Gaurav Narang

Design Engineer II, Synopsys

Applying for PhD position in Efficient Architectures for AI/Deep learning

gaurav13125@iiitd.ac.in

+91 7838175600

New Delhi, India

linkedin.com/in/gaurav-narang-272b3546

WORK EXPERIENCE

Design Engineer II
Synopsys

03/2018 – Present *Noida, India*

Responsibilities

- Independent ownership of serdes testchip frontend design
- Worked on HDMI/USB testchips in latest technology nodes
- Specification documentation, coordinating between IP teams and design reviews

Design Engineer
STMicroelectronics

08/2015 – 03/2018 *Noida, India*

Responsibilities

- RTL design of memory repair IP and ECC for SRAM
- Deployed a fully automated environment for RTL generation using Python

RESEARCH PUBLICATIONS

Heterogeneous Memory Assembly Exploration Using a Floorplan and Interconnect Aware Framework
- 29th IEEE International System-on- Chip Conference, 2016 in Seattle, USA

Floorplan Aware And Congestion Aware Framework For Optimal SRAM Selection For Memory Subsystems
- 28th IEEE International System-on-Chip Conference, 2015 in Beijing, China

Statistical Analysis of 64Mb SRAM for Optimizing Yield and Write Performance
- 28th International Conference on VLSI Design, 2015 in Bengaluru, India

EDUCATION

Mtech (VLSI & Embedded systems)
IIIT DELHI (CGPA 8.88/10)

2013 – 2015 *New Delhi*

Thesis

- Developed a framework for architectural analysis to select the optimal memory instances for larger memory designs : In collaboration with STMicroelectronics, India

Btech (ECE)
GGSIPU (Percentage 79.86%)

2009 – 2013 *New Delhi*

Projects

- Digital design & comparative analysis of Affine cipher architecture
- Density based traffic light controller : responsible for hardware, soldering, ICs understanding

SKILLS

Digital Hardware Design | Verilog | C | Tcl | Python | RTL simulations (vcs) | Synthesis (Design Compiler) | Spyglass (CDC, LINT)

ACHIEVEMENTS

Distinguished Alumni Award (MSIT, GGSIPU) (04/2016)

Awarded Student Fellowship for 28th International VLSI Design Conference (2015)

test scores - GRE - 319

MOOC/CERTIFICATES

Neural Networks and Deep Learning
deeplearning.ai on Coursera.org

Programming for everybody
University of Michigan, on Coursera.org

Python Data Structures
University of Michigan, on Coursera.org

VLSI CAD: Logic to Layout
University of Illinois at Urbana-Champaign, on Coursera.org

RESEARCH PROJECTS

Multivariate Statistical Analysis of 64Mb SRAM
Yield vs performance analysis for different capacities of 6T SRAM cell using Design of Experiment (DoE) approach and nonlinear regression

Energy Efficient NoC Architecture using EVCs
Implemented a parameterized router node with Express Virtual Channels (EVCs) and token based flow control to virtually bypass intermediate nodes in multicore architecture.

INTERESTS

Edge computing | Deep learning | Efficient VLSI architectures | Processing in memory