

**FINAL PROJECT REPORT**

**EENG – 5540**

**DIGITAL IC DESIGN**

**(FALL 2023)**

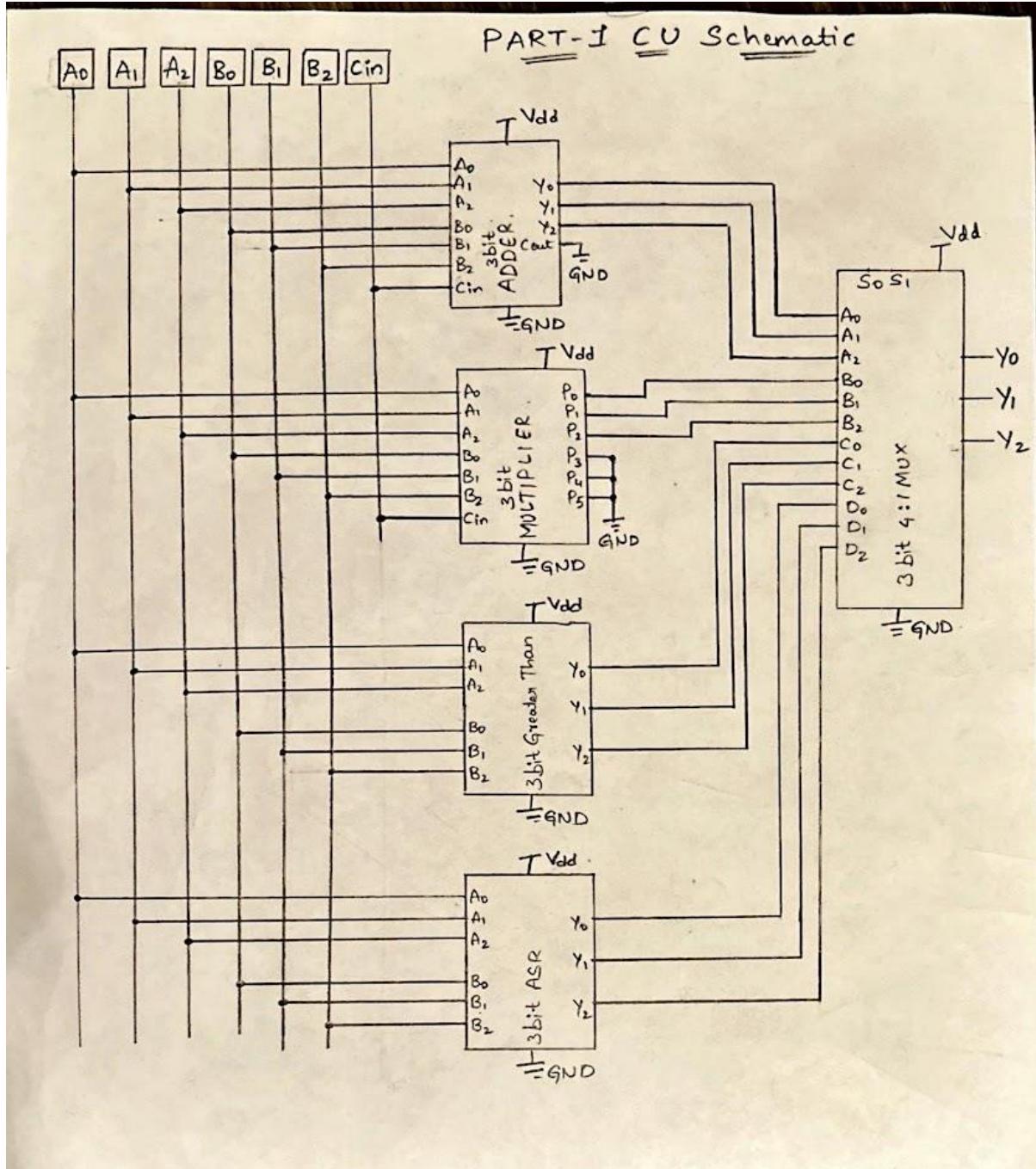
**Submitted By**

**NARAYANA REDDY SANDRU**

**11558422**

## PART 1 CU

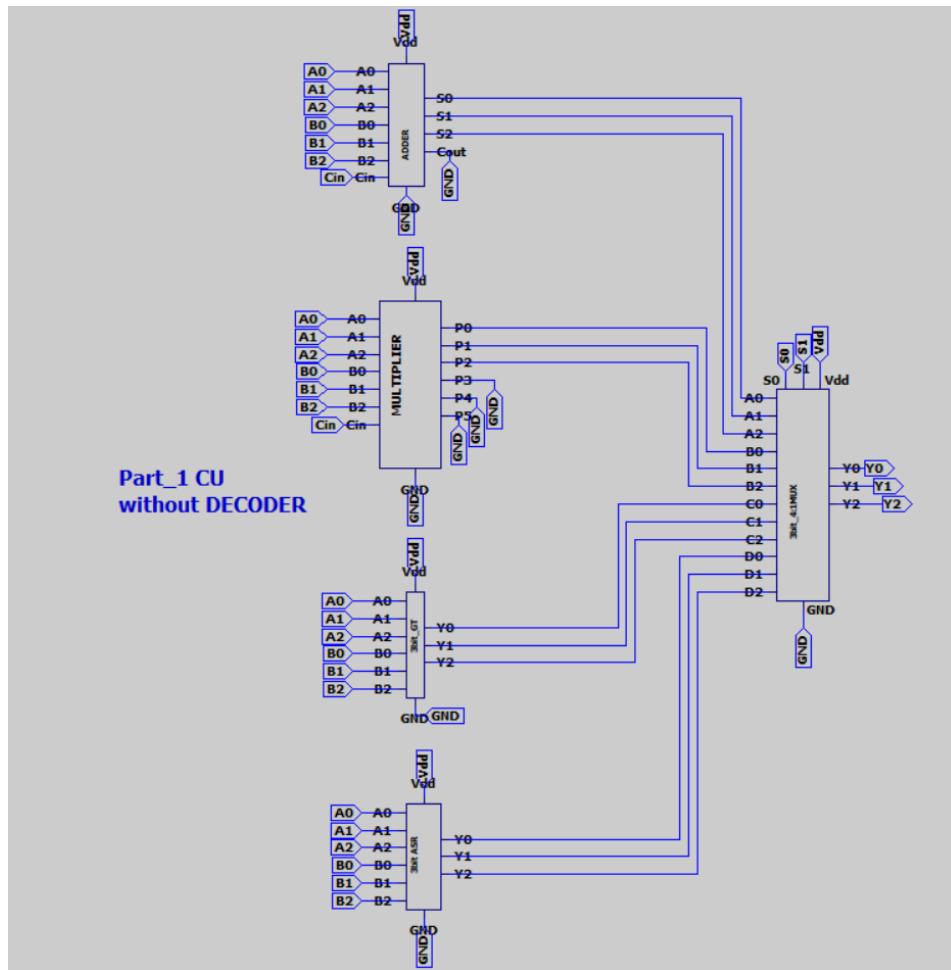
CU Circuit Diagram



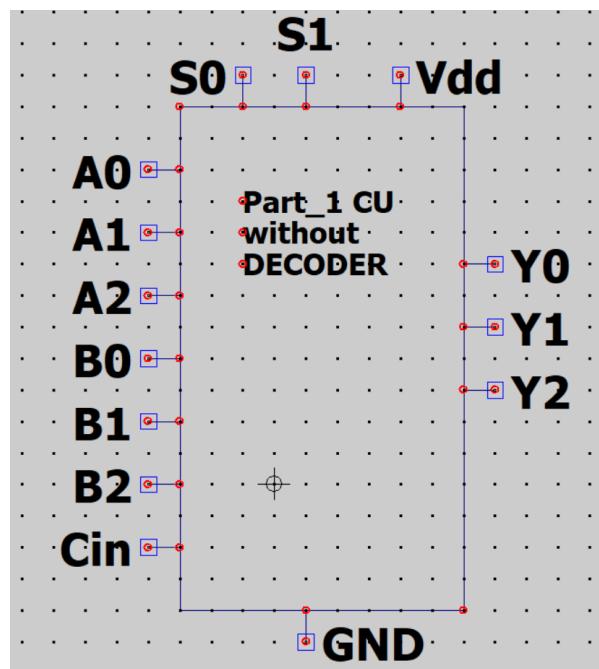
In the circuit CU-1, we have taken input's as A<sub>2</sub> , A<sub>1</sub>, A<sub>0</sub> , B<sub>2</sub> , B<sub>1</sub> , B<sub>0</sub>

These inputs are given to the CU. The CU calculates all the given four operations (ADD , MULTIPLY , GREATER THAN , ASR). The selector lines of the MUX S<sub>0</sub> , S<sub>1</sub> decide the overall CU output.

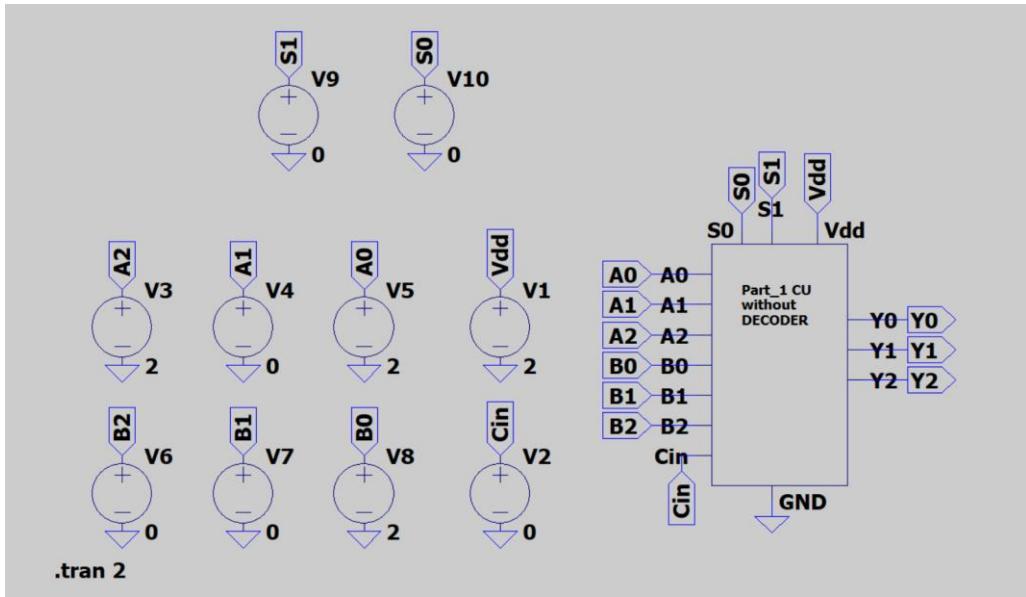
## CU Schematic



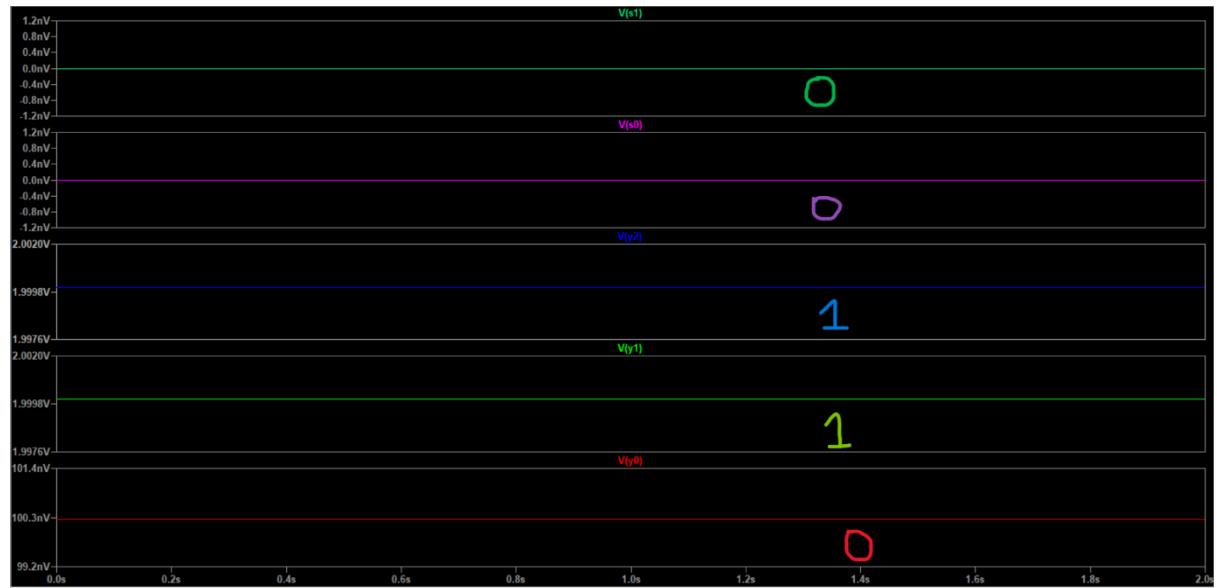
## CU Symbol



### CU Test Circuit-1(for ADD)



### CU Test Circuit-1 Waveform



A2 , A1 , A0 = 1 0 1

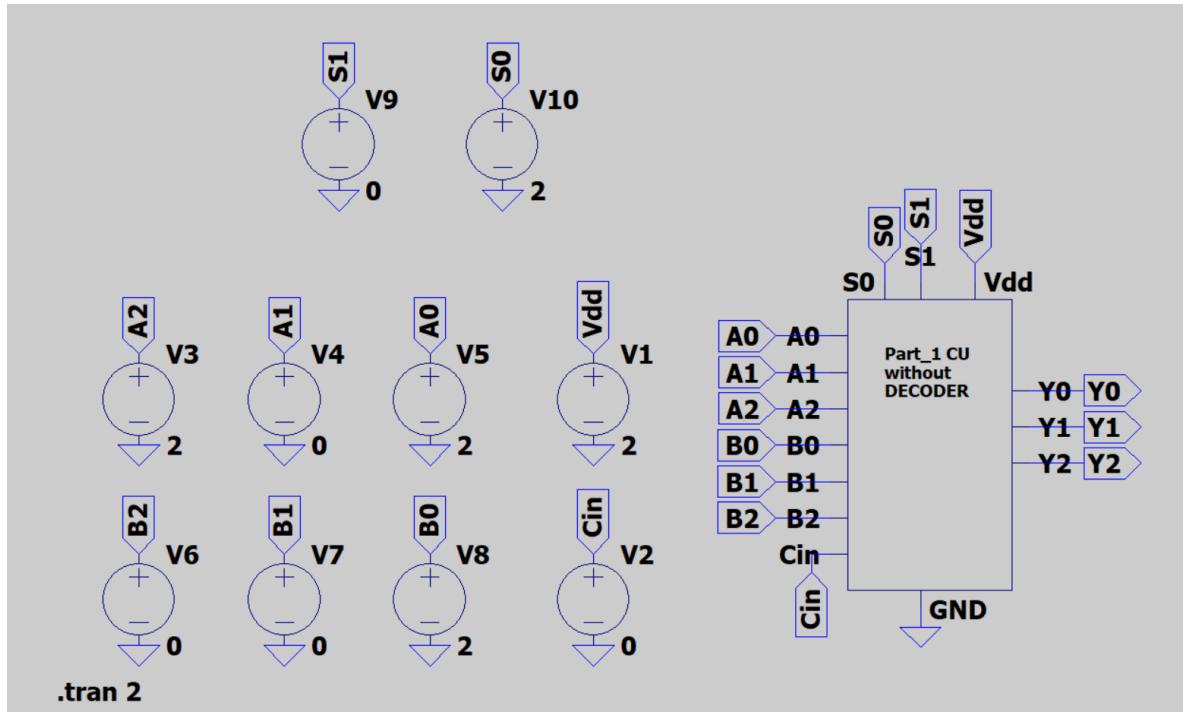
B2 , B1 , B0 = 0 0 1.

Selector lines S1 , S0 = 0 0. i.e., the 3-bit 4:1 MUX chooses output from Addition unit and reflects the same as CU's output. Y2 , Y1 , Y0 = 1 1 0.

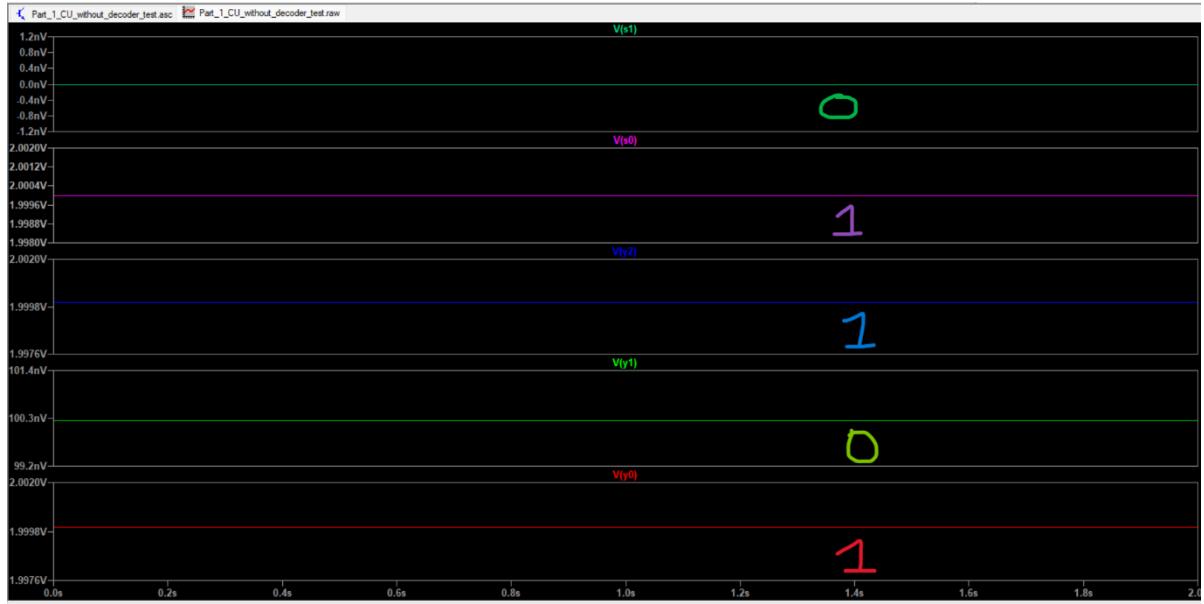
#### Verification Statement:

The generated output waveform values for the Test circuit-1 match with the above calculated output values. And the CU device works properly.

## CU Test Circuit-2(for MULTIPLY)



## CU Test Circuit-2 Waveform



A2 , A1 , A0 = 1 0 1

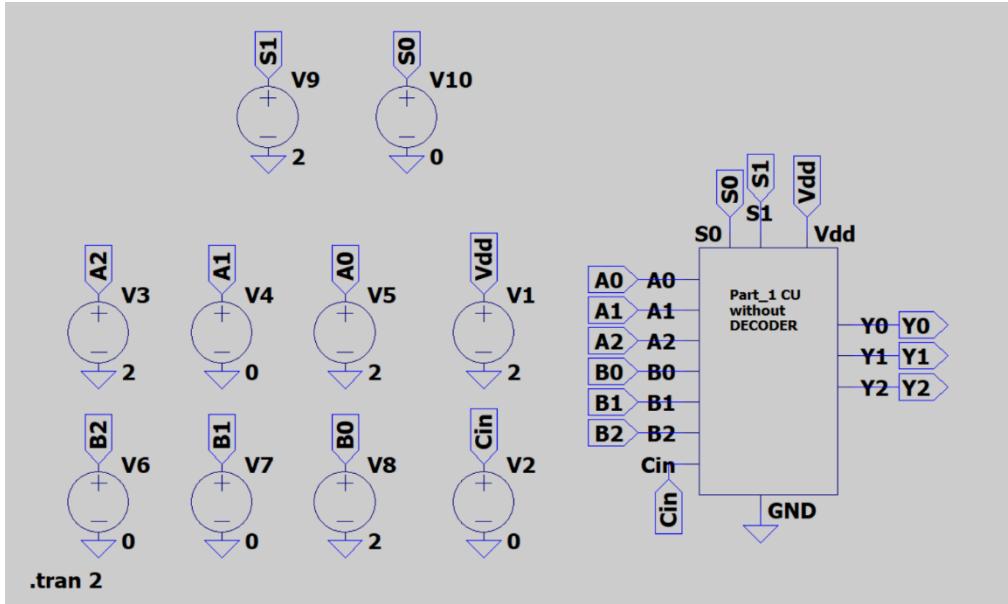
B2 , B1 , B0 = 0 0 1.

Selector lines S1 , S0 = 0 1. i.e., the 3-bit 4:1 MUX chooses output from Multiplication unit and reflects the same as CU's output. Y2 , Y1 , Y0 = 1 0 1.

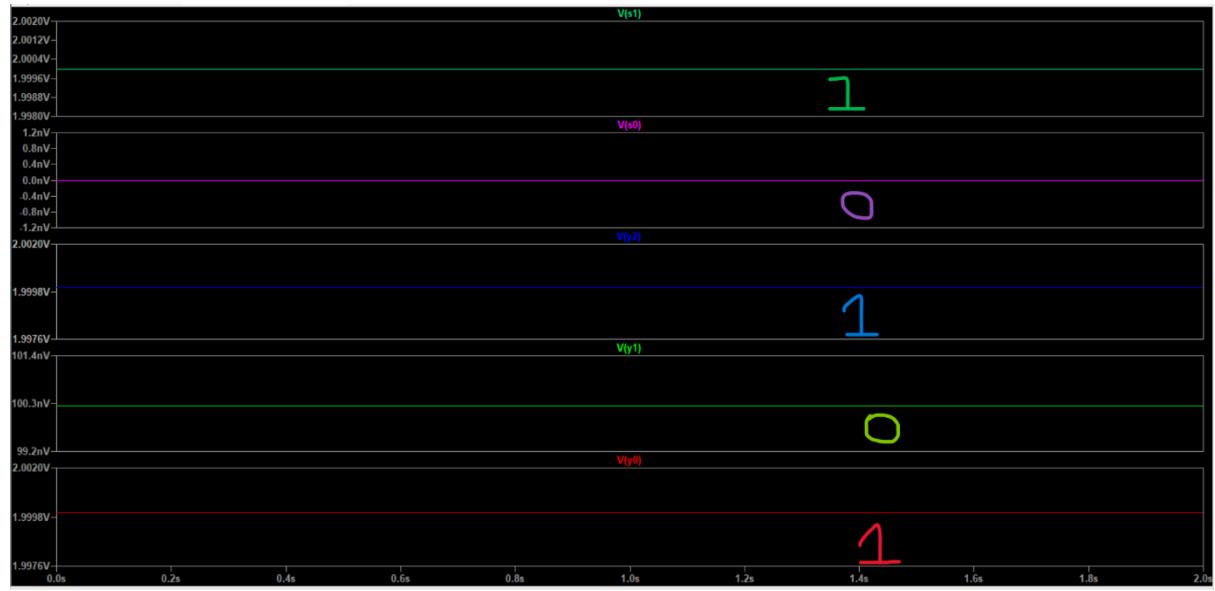
### Verification Statement:

The simulated test case outputs and the calculated output values, both are same and are verified.

### CU Test Circuit – 3(for GT)



### CU Test Circuit-3 Waveform



A2 , A1 , A0 = 1 0 1

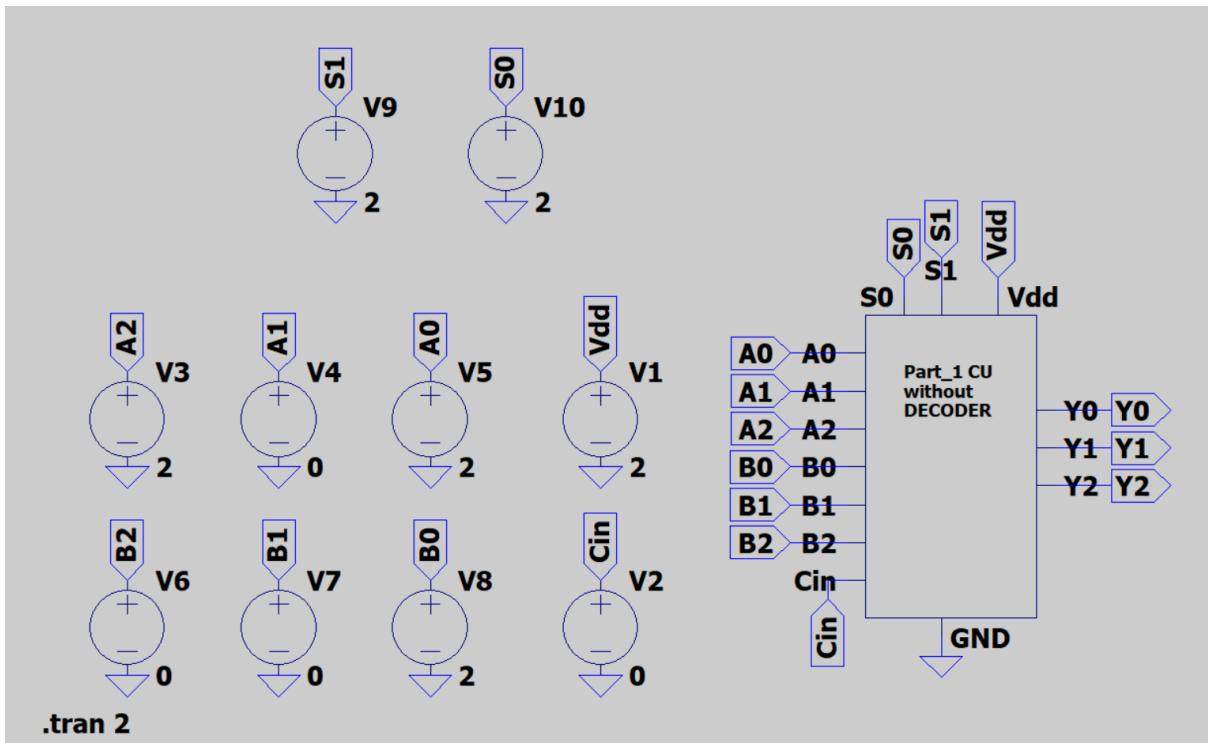
B2 , B1 , B0 = 0 0 1. Selector lines S1 , S0 = 1 0. i.e., the 3-bit 4:1 MUX chooses output from Greater Than unit and reflects the same as CU's output. Y2 , Y1 , Y0 = 1 0 1.

#### Verification Statement:

The waveform values generated for the Test circuit-2 match with the above calculated values for the GT operation.

This verifies that the CU unit works properly.

### CU Test Circuit-4(for ASR)



### CU Test Circuit-4 Waveform



A2 , A1 , A0 = 1 0 1

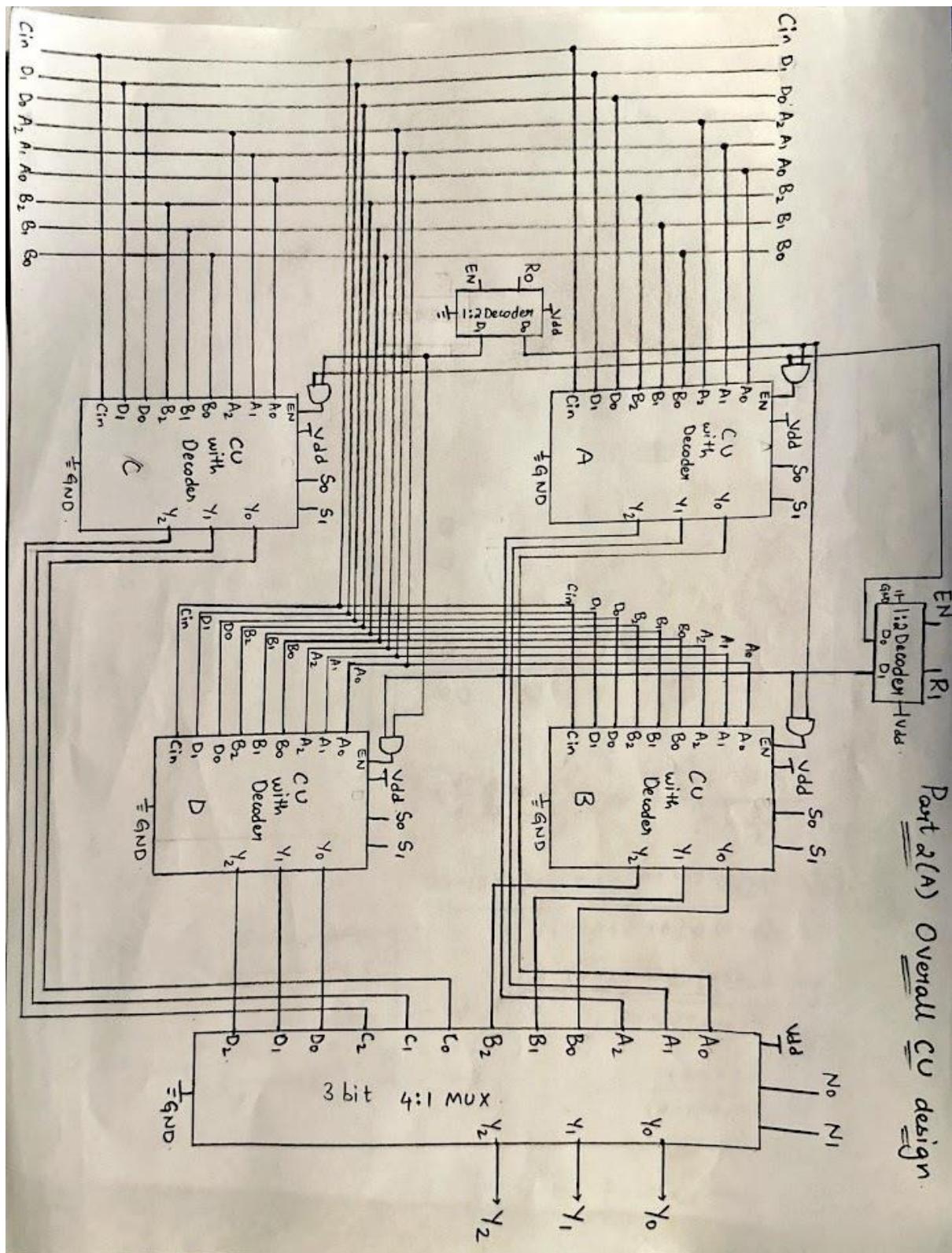
B2 , B1 , B0 = 0 0 1. Selector lines S1 , S0 = 1 1. i.e., the 3-bit 4:1 MUX chooses output from ASR unit and reflects the same as CU's output. Y2 , Y1 , Y0 = 1 1 0.

#### Verification Statement:

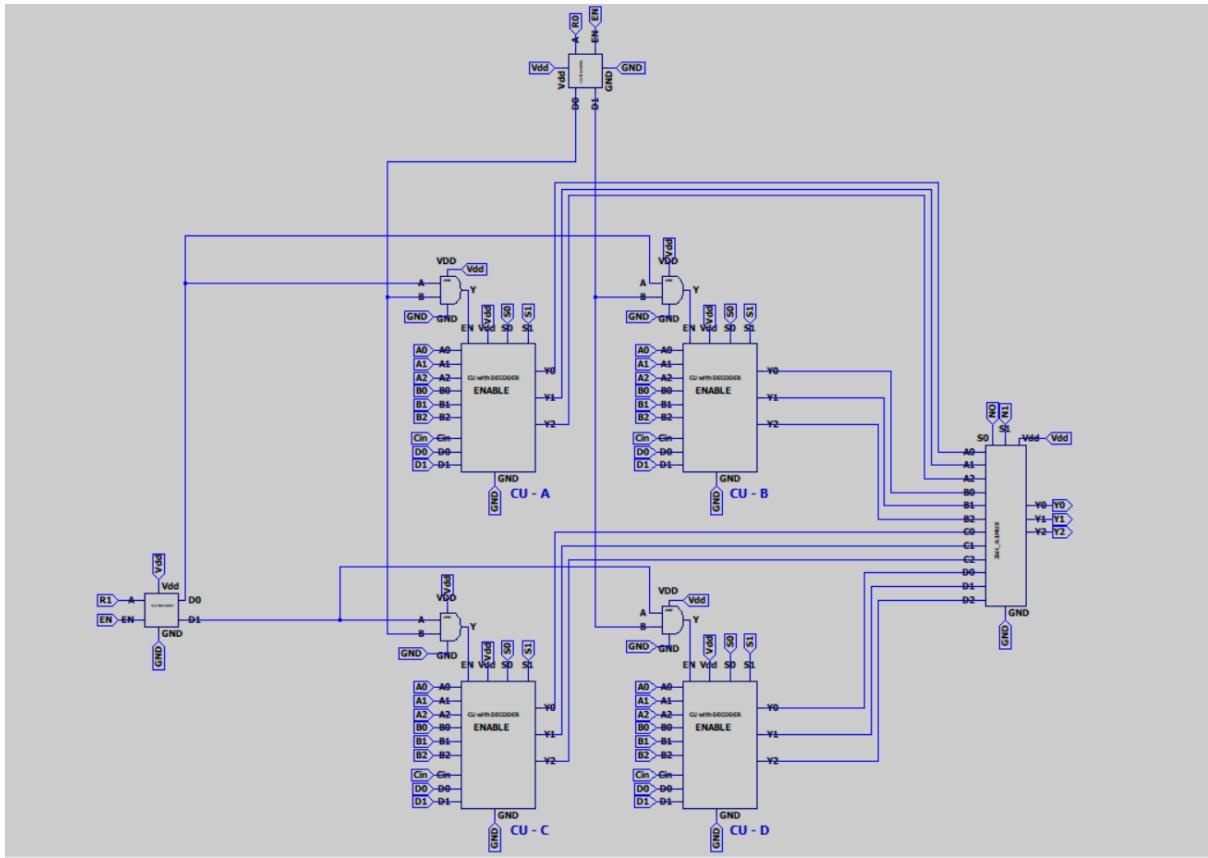
Waveform values generated by test circuit for ASR and the above calculated values both are same and are verified.

## Part 2(a) OVERALL CU Design

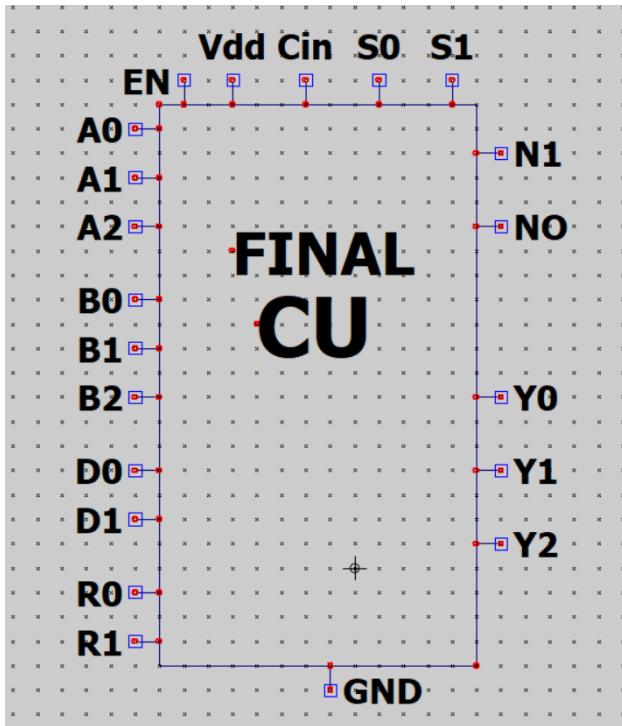
Overall device circuit drawing



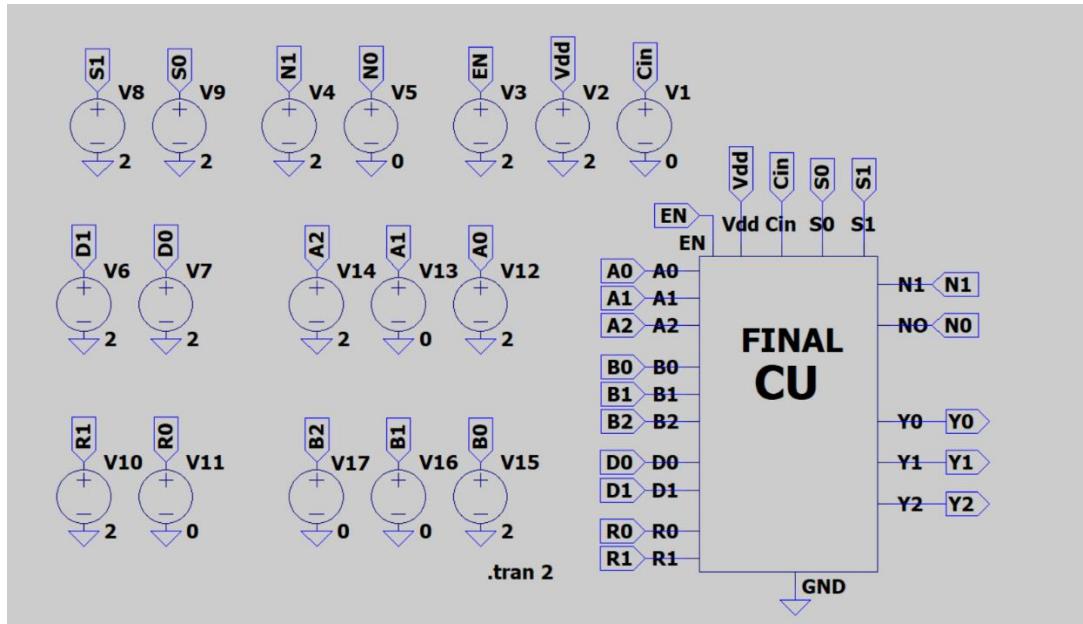
## Overall device circuit Schematic



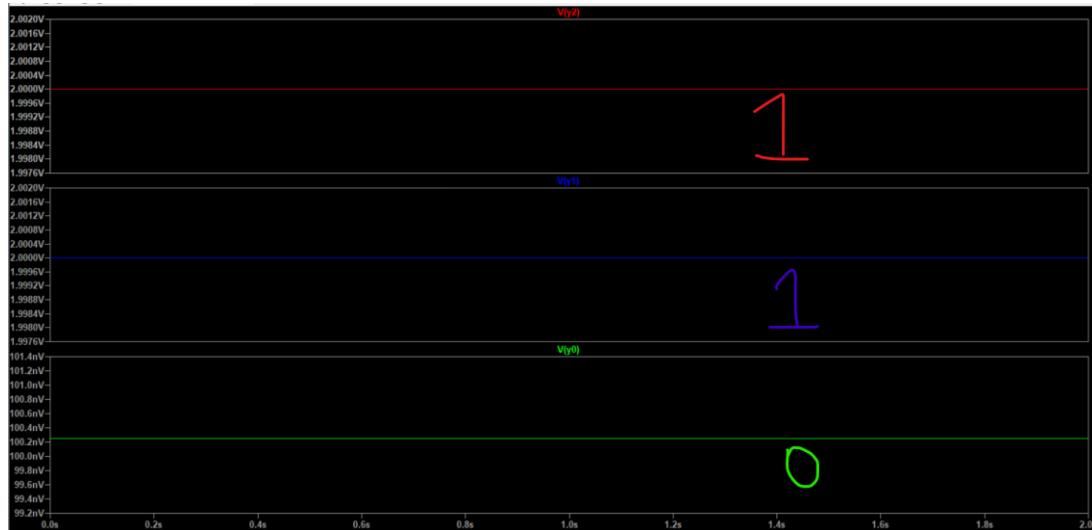
## Overall device circuit symbol drawing/shape



## Overall device test circuit



## Test circuit waveform



A2 , A1 , A0 ; B2 , B1 , B0 are the inputs for the CU

R1 , R0 are inputs from 1:2 decoders. Based on the values of these two decoders the CU's to operate are chosen

R1	R0	CU operated
0	0	CU - A
0	1	CU - B
1	0	CU - C
1	1	CU - D

D1 , D0 are the inputs for the 2:4 decoder. The output from this decoder enables the particular operational unit to get functional.

D1	D0	Operation
0	0	ADD
0	1	MULTIPLY
1	0	GREATER THAN
1	1	ASR

S1 , S0 are the 3bit 4:1 MUX selector lines, which choose the operation output from the CU.

S1	S0	Operation
0	0	ADD
0	1	MULTIPLY
1	0	GREATER THAN
1	1	ASR

N1 , N0 are the selector lines for the overall blocks. This 3-bit 4:1 MUX chooses the output from which CU block to be taken as Y2 , Y1 , Y0

N1	N0	CU operated
0	0	CU – A
0	1	CU – B
1	0	CU – C
1	1	CU – D

## Calculation

inputs are A2 , A1 , A0 – 1 0 1 ; B2 , B1 , B0 – 0 0 1

R1 , R0 = 1 0 . CU – 3 is enabled and the operations are performed.

D1 , D0 = 1 1 . ASR operation is performed in the CU.

S1 , S0 = 1 1. O/p from the CU is taken from ASR.

N1 , N0 = 1 0. The overall CU o/p is taken from CU – 3 (ASR operation).

Output is -      Y2 , Y1 , Y0 = 1 1 0.

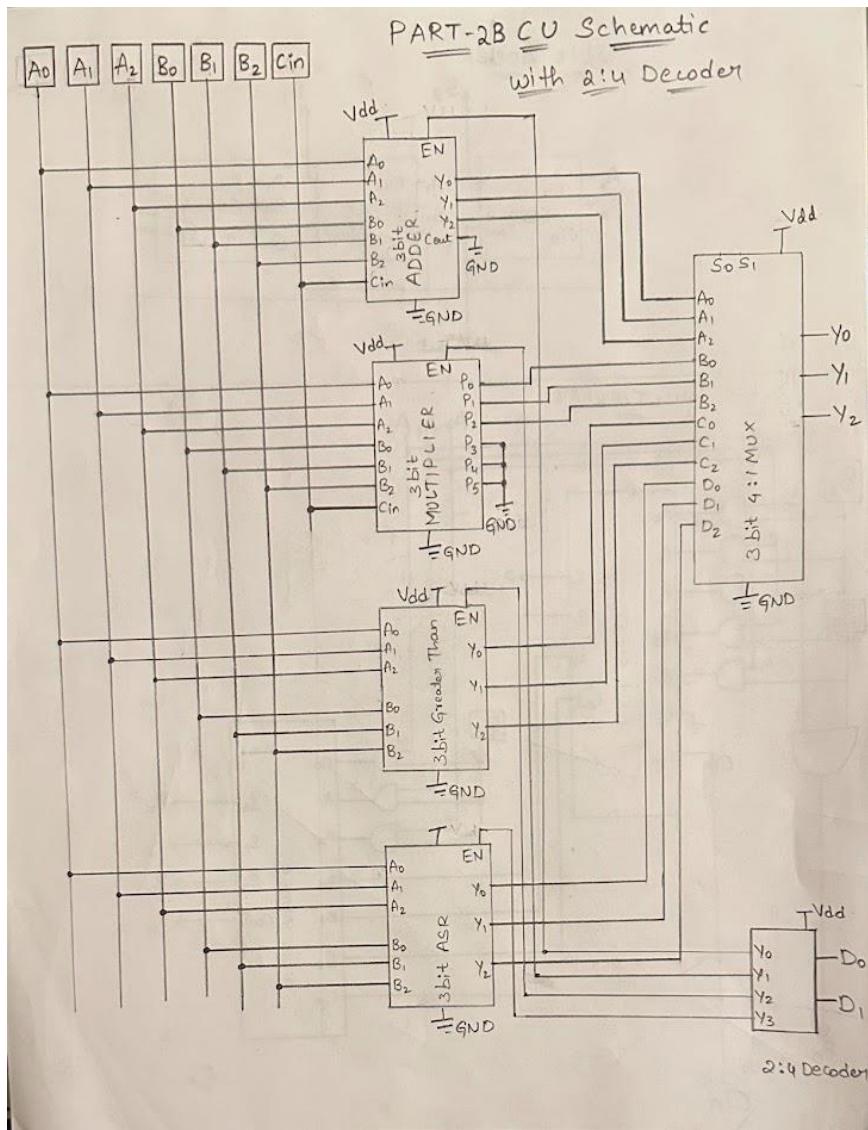
## Verification Statement

The calculated output matches with the waveform o/p generated by test circuit.

The Overall CU device works properly and is verified by the above result.

## PART 2(b) CU with DECODER

Overall device circuit drawing



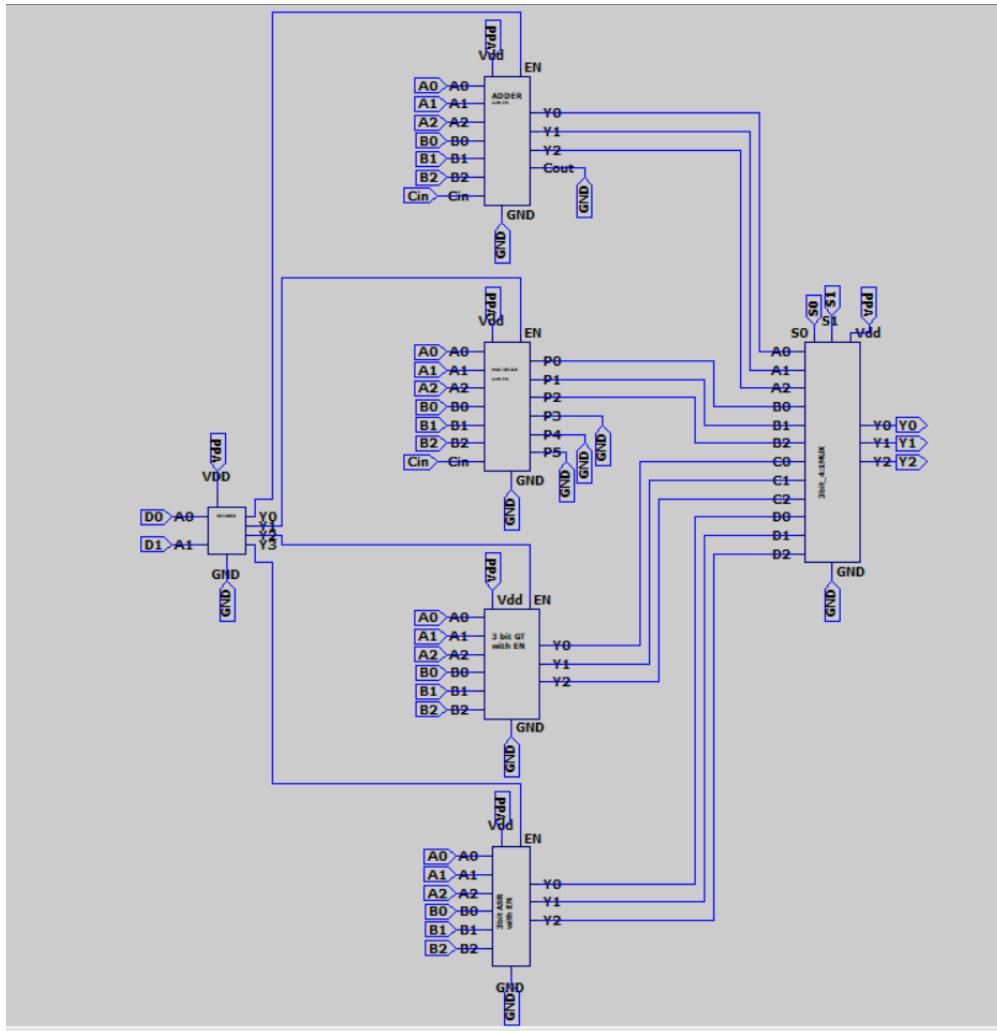
In the circuit the 4 operations ADD, MULTIPLY, GT, ASR devices are given an enable pin.

The enable pin is operated through a 2:4 DECODER. The 4 output's from the decoder are given as enables to each of the 4 devices. The value of the EN pin decides weather the device to function or not. If the EN is 0 then the devices don't run. If the EN is 1 then the device operates.

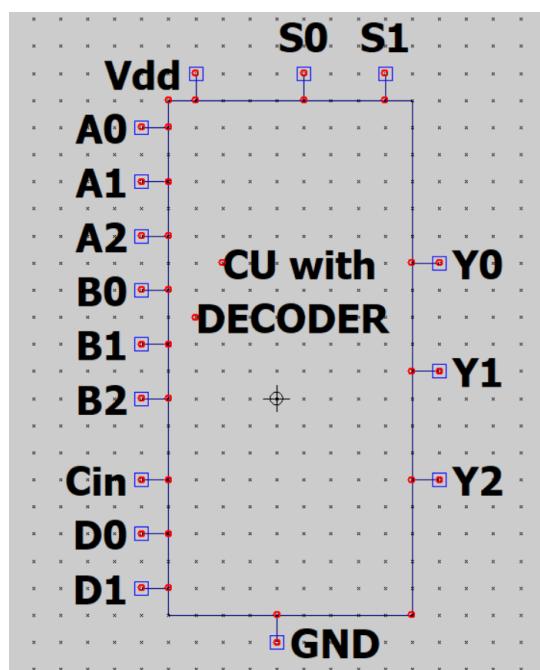
The 3-bit input's A2,A1,A0 ; B2,B1,B0 are given to the CU. The CU calculates the given four operations (ADD , MULTIPLY , GT , ASR) based on decoder o/p values.

The selector lines of the 3-bit 4:1 MUX S0 , S1 control the overall output's (Y2 , Y1 , Y0) of CU.

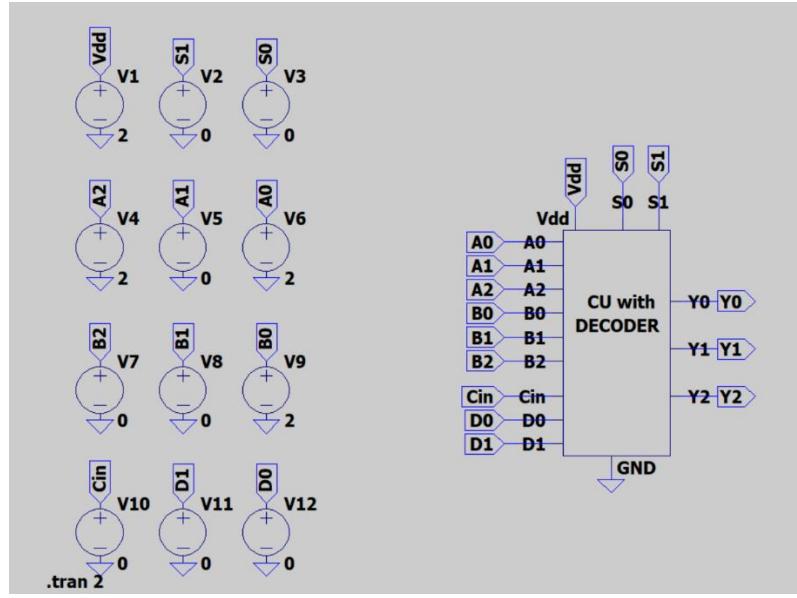
## Overall device symbol schematic



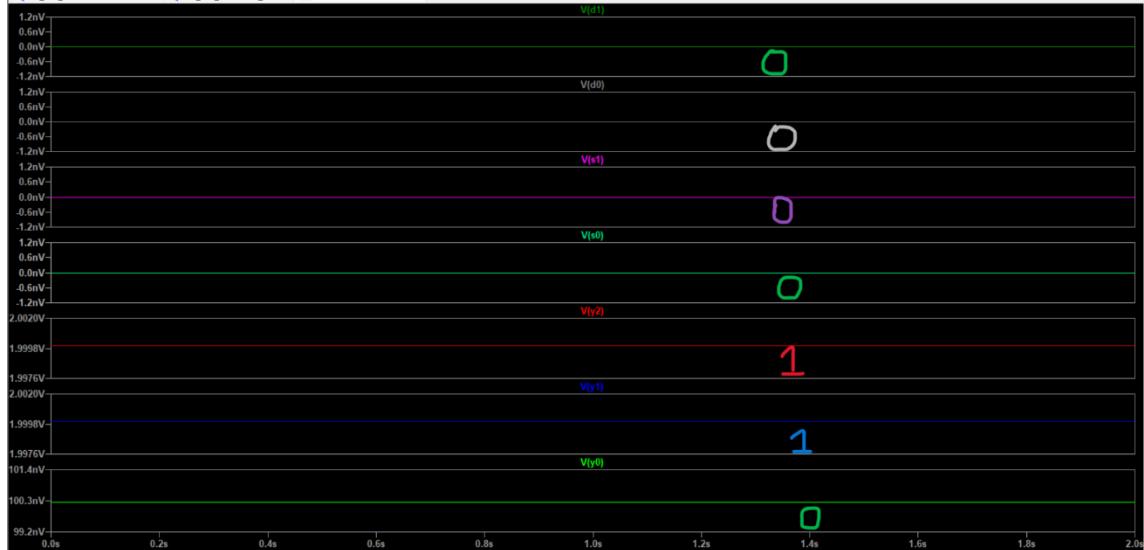
## Overall device symbol drawing/shape



## Overall device test circuit (for ADD)



## Test circuit Waveforms



Inputs for the CU are - A2 , A1 , A0 = 1 0 1 ; B2 , B1 , B0 = 0 0 1 .

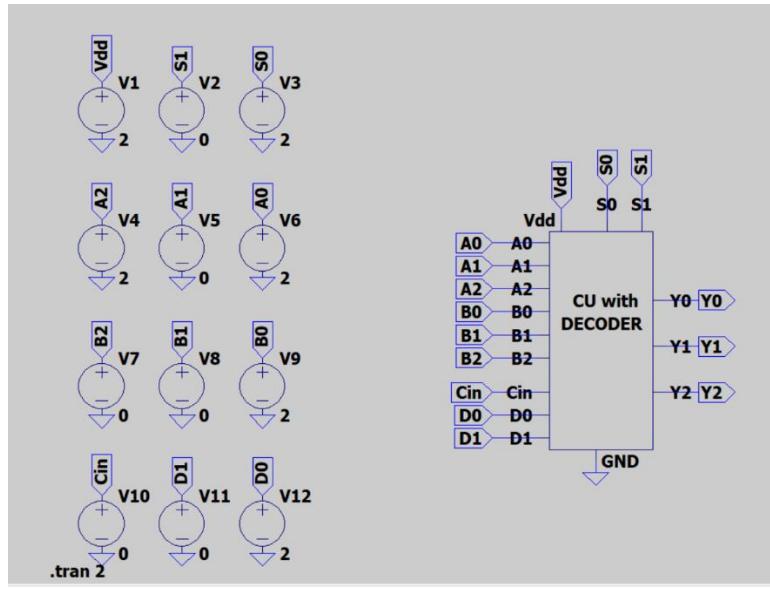
Decoder inputs D1 , D0 = 0 0 ; then the o/p pin Y0 from decoder is high(1) and it enables the operation of Adder unit in CU.

Selector lines S1 , S0 = 0 0. i.e., the 3-bit 4:1 MUX chooses output from Addition unit and reflects the same as CU's output. Y2 , Y1 , Y0 = 1 1 0 .

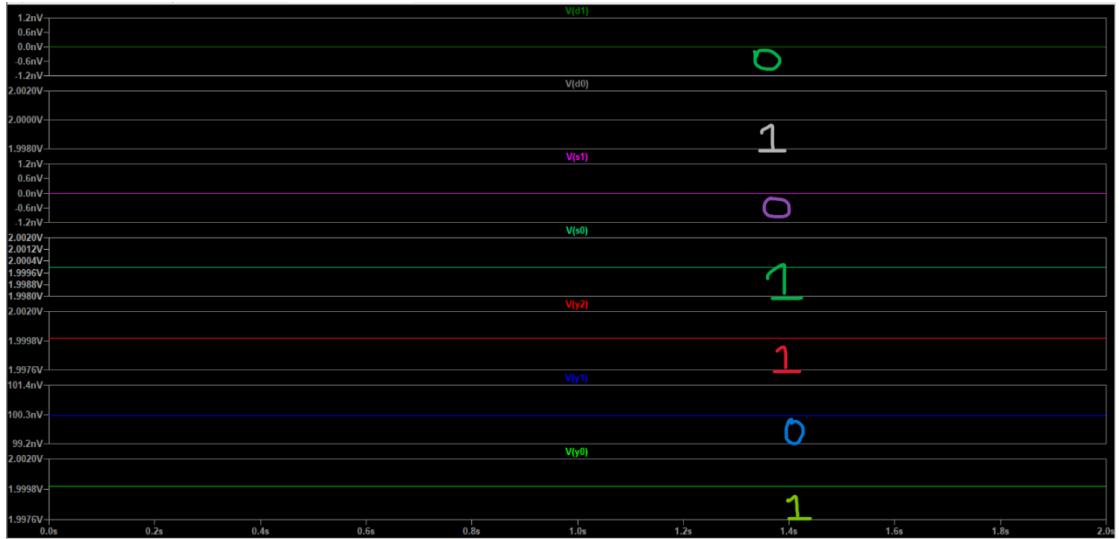
## Verification Statement:

Waveform values generated by test circuit and the above calculated values both are same and are verified.

## Overall device test circuit (for Multiply)



## Test circuit Waveforms



## Verification Statement

Inputs for the CU are - A2 , A1 , A0 = 1 0 1 ; B2 , B1 , B0 = 0 0 1 .

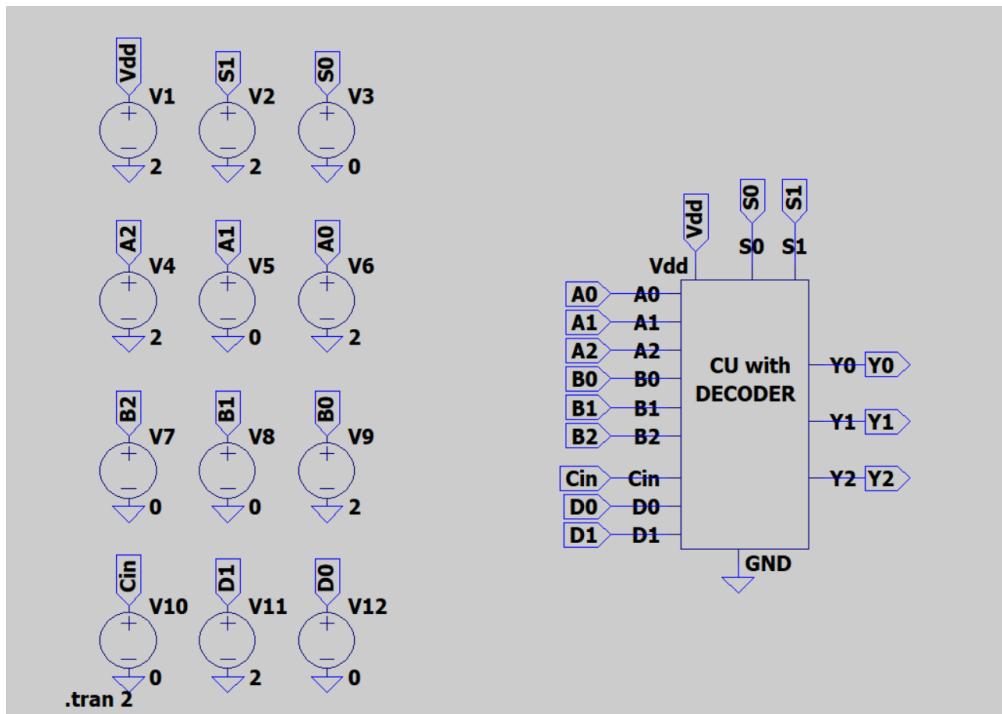
Decoder inputs D1 , D0 = 0 1 ; then the o/p pin Y1 from decoder is high(1) and it enables the operation of Multiplier unit in CU.

Selector lines S1 , S0 = 0 1. i.e., the 3-bit 4:1 MUX chooses output from Multiplier unit and reflects the same as CU's output. Y2 , Y1 , Y0 = 1 0 1 .

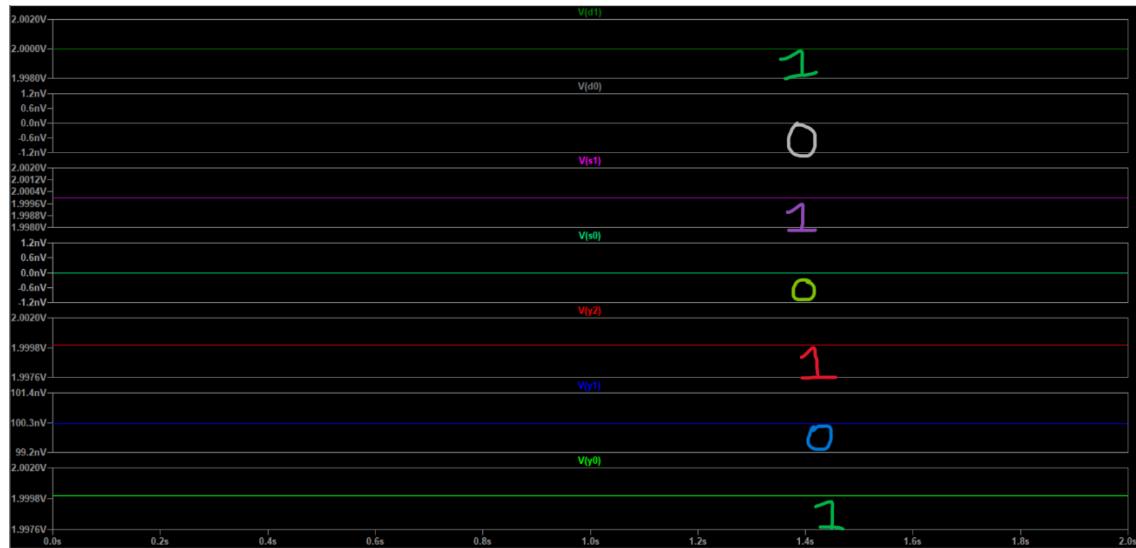
## Verification Statement:

The waveform values obtained from the test circuit and the computed values mentioned above are exactly the same and have been validated.

## Overall device test circuit (for GT)



## Test circuit Waveforms



## Verification Statement

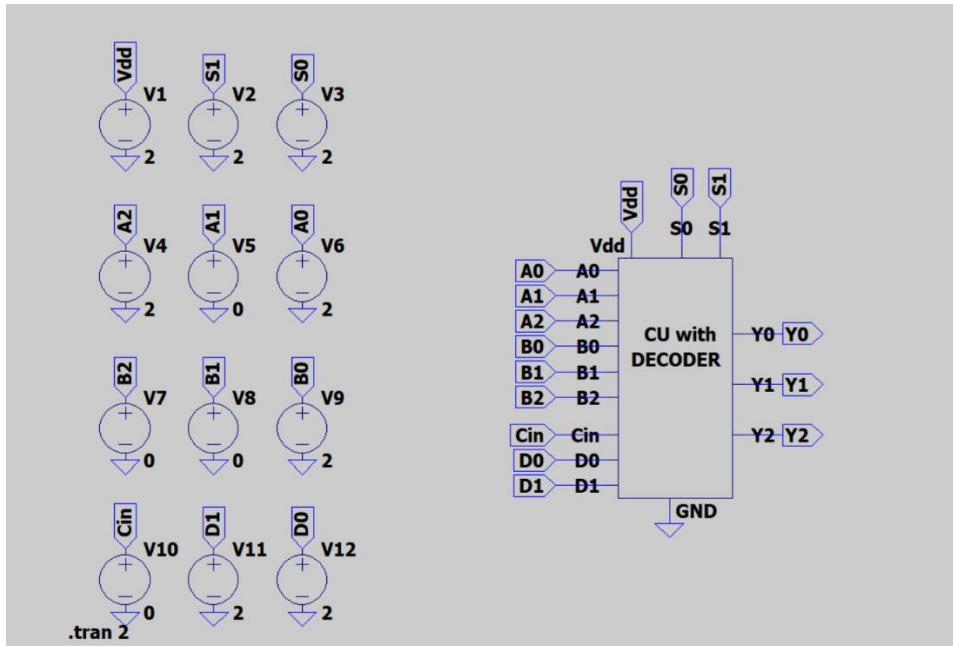
Inputs for the CU are - A2 , A1 , A0 = 1 0 1 ; B2 , B1 , B0 = 0 0 1.

Decoder inputs D1 , D0 = 1 0 ; then the o/p pin Y2 from decoder is high(1) and it enables the operation of Greater Than unit in CU.

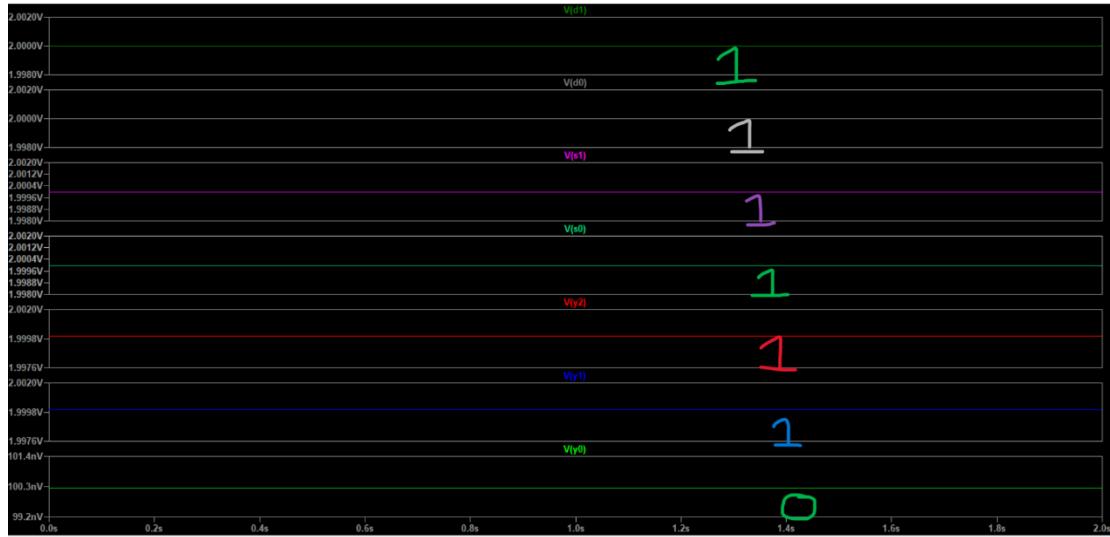
Selecter lines S1 , S0 = 1 0. i.e., the 3-bit 4:1 MUX chooses output from Multiplier unit and reflects the same as CU's output. Y2 , Y1 , Y0 = 1 0 1.

The generated output waveform values from the Test circuit and the above calculated output values are same and are verified. Overall CU device works properly.

## Overall device test circuit (for ASR)



## Test circuit Waveforms



## Verification Statement

Inputs for the CU are - A2 , A1 , A0 = 1 0 1 ; B2 , B1 , B0 = 0 0 1.

Decoder inputs D1 , D0 = 1 1 ; then the o/p pin Y3 from decoder is high(1) and it enables the operation of ASR unit in CU.

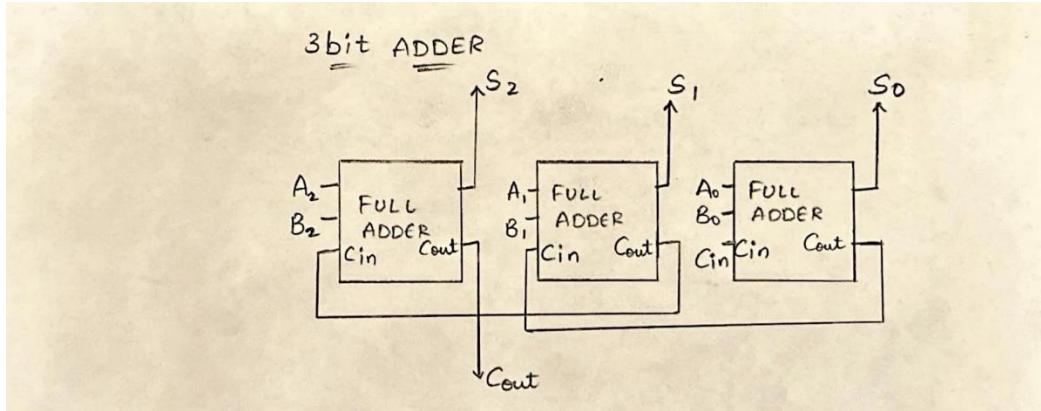
Selector lines S1 , S0 = 1 1. i.e., the 3-bit 4:1 MUX chooses output from ASR unit and reflects the same as CU's output. Y2 , Y1 , Y0 = 1 1 0.

The simulated test case outputs and the calculated output values, both are same and are verified.

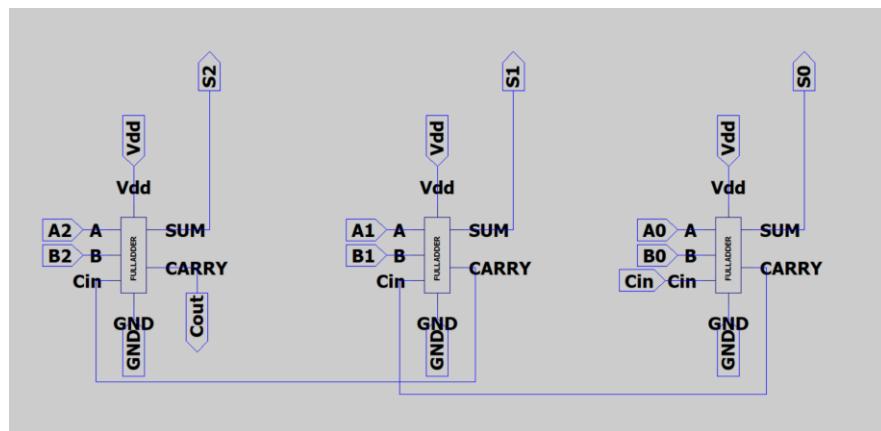
## OPERATION COMPONENTS

### ADDITION

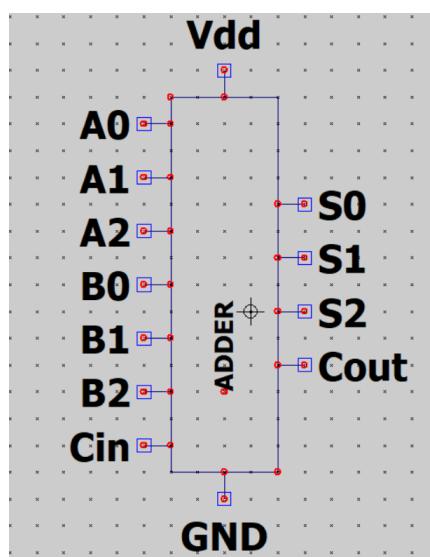
Separate gate-level drawing:



Symbol Schematic:



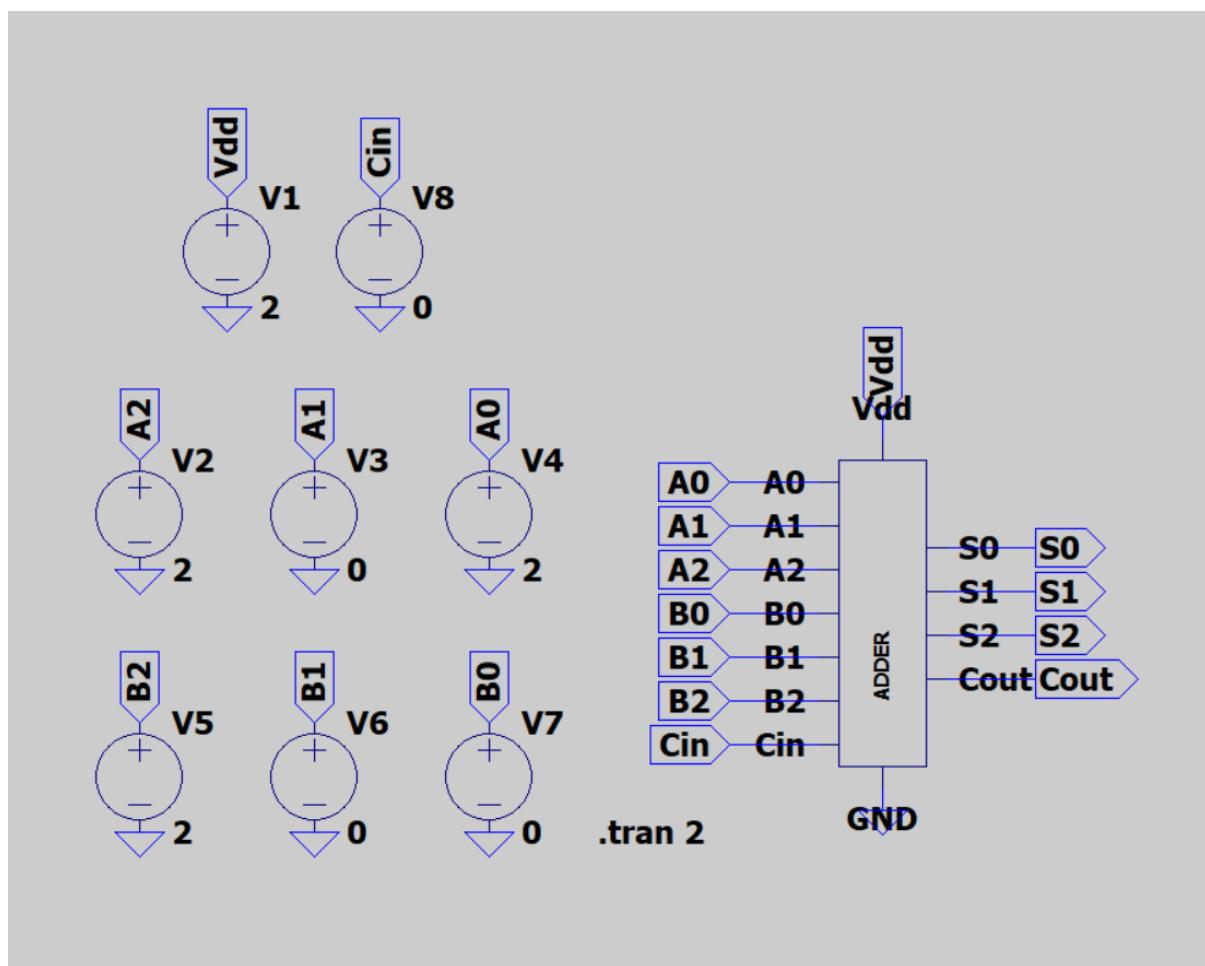
Symbol drawing/shape:



### Test case calculation

$$\begin{array}{r}
 \begin{array}{ccccccc}
 & 1 & 0 & & 1 & - & A_2 \ A_1 \ A_0 \\
 & (+) & 1 & 0 & 0 & - & B_2 \ B_1 \ B_0 \\
 \hline
 & 1 & 0 & 0 & 1 & & \\
 \text{Cout} & Y_2 & Y_1 & Y_0 & & &
 \end{array}
 \end{array}$$

### Test Circuit



## Test Circuit Waveforms



### Verification Statement:

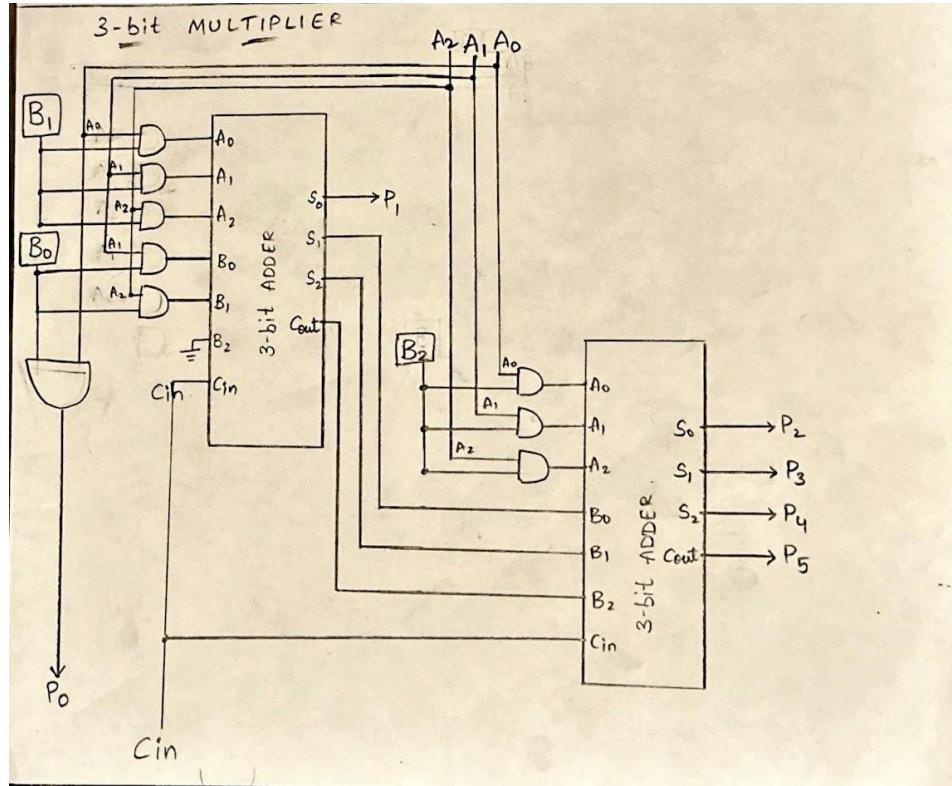
Inputs are A2,A1,A0 – 1 0 1 ; B2,B1,B0 – 1 0 0 . Cin = 0. The adder unit performs addition operation for the two 3 bit inputs. The output is Y2,Y1,Y0 – 0 0 1. Cout = 1.

The waveform values generated from the test case circuit for the ADDITION operation match with the calculated test case output values.

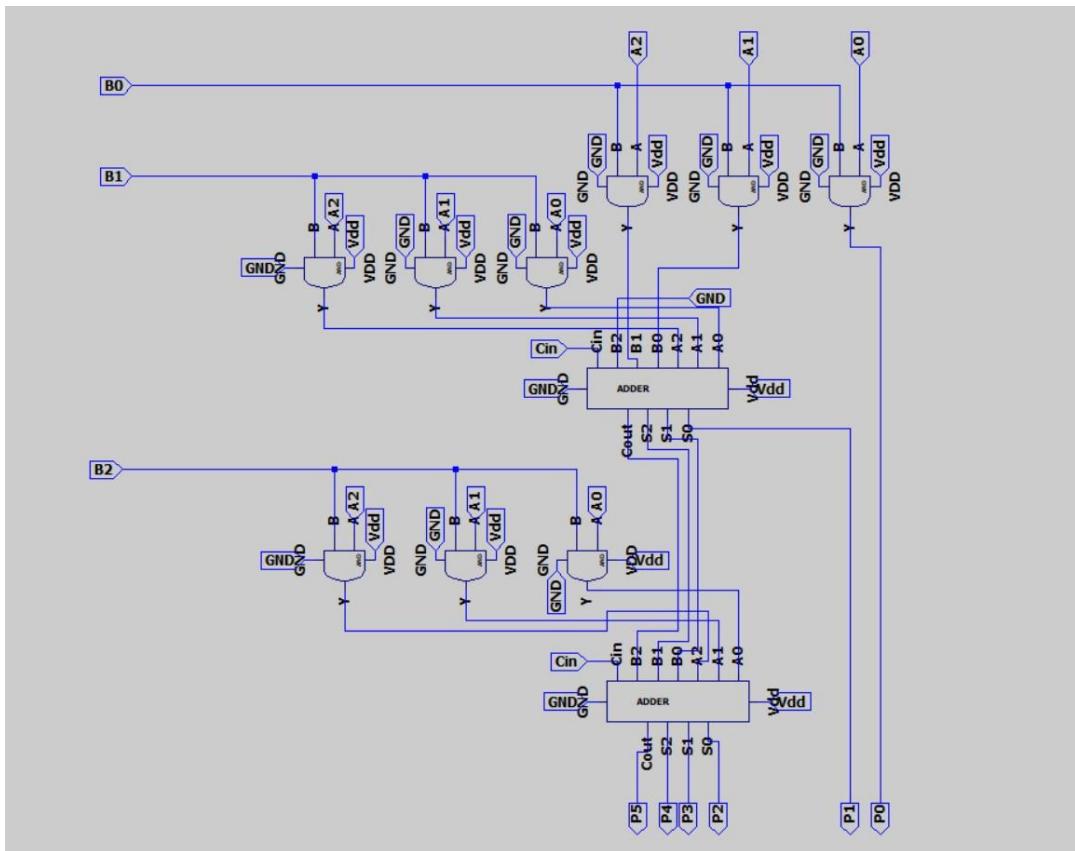
It is verified that the ADDITION unit works properly.

## MULTIPLICATION

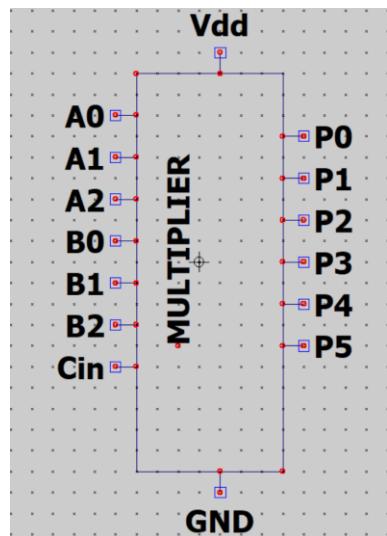
Separate gate level drawing



Symbol Schematic



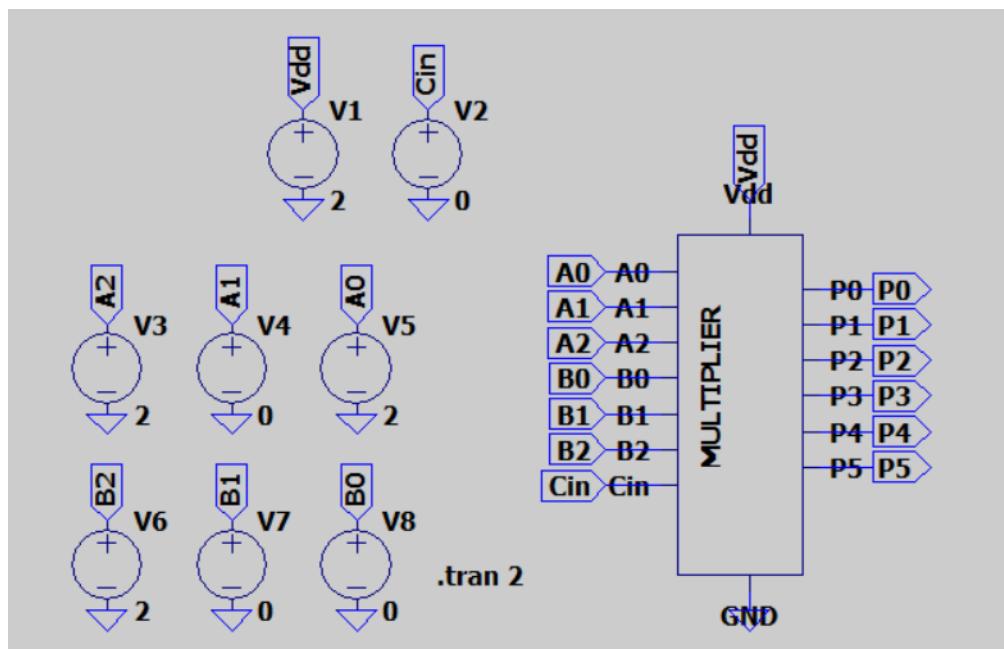
## Symbol drawing/shape



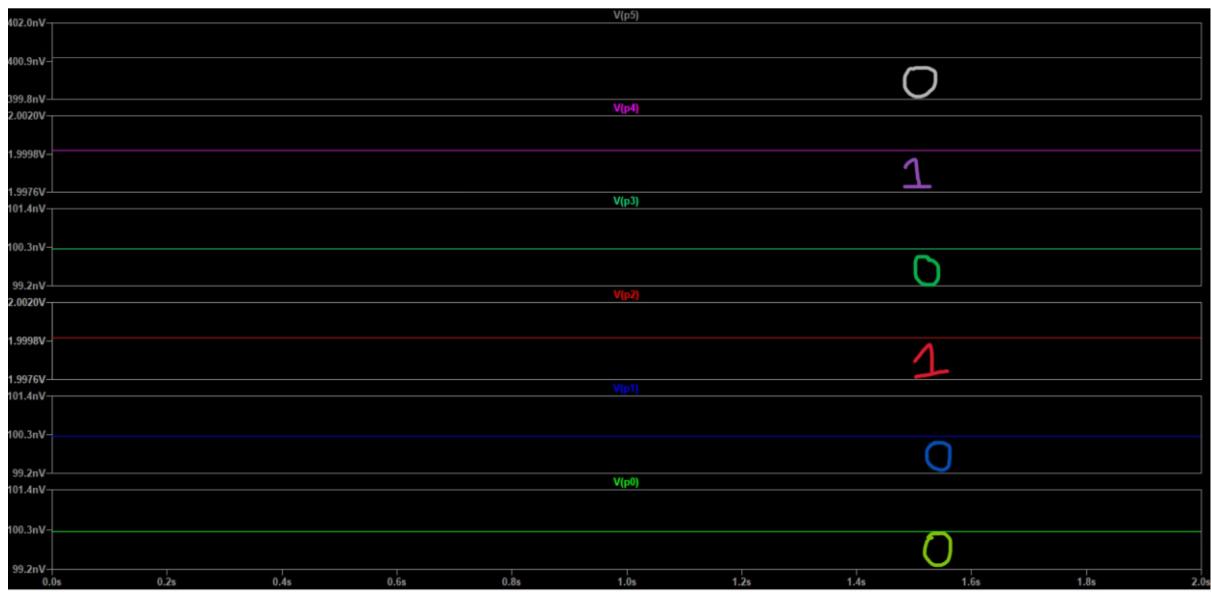
## Test case calculation

$$\begin{array}{r}
 101 - A_2 \ A_1 \ A_0 \\
 \times 100 - B_2 \ B_1 \ B_0 \\
 \hline
 000 \\
 000 \\
 \hline
 \text{(+) } 101 \\
 \hline
 010100 - P_5 \ P_4 \ P_3 \ P_2 \ P_1 \ P_0
 \end{array}$$

## Test Circuit



## Test Circuit Waveforms



### Verification Statement:

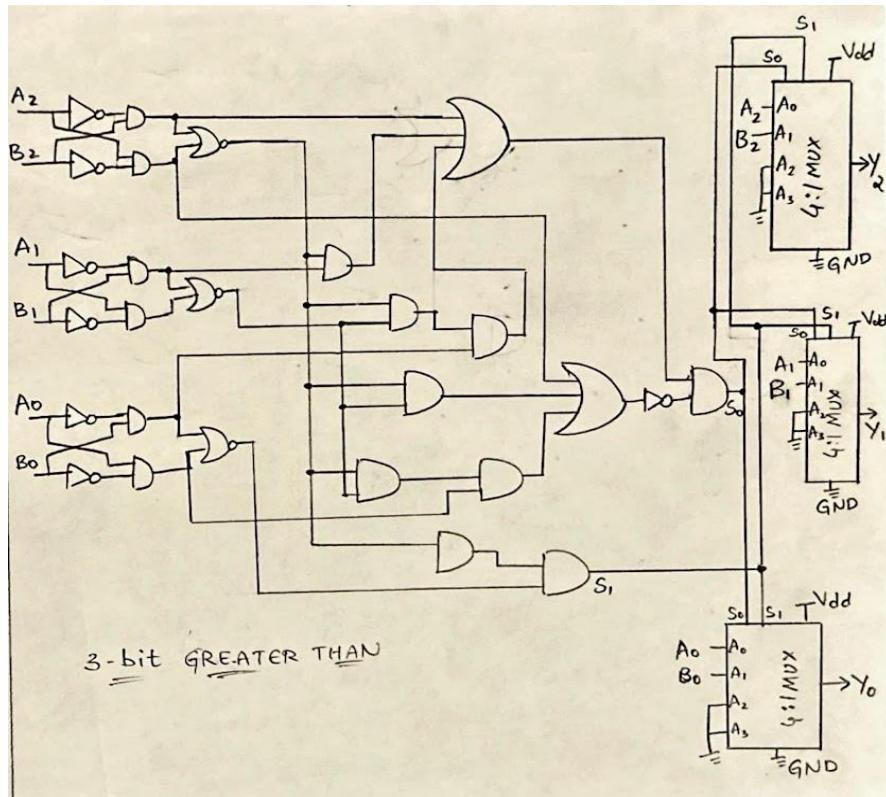
Inputs are A2,A1,A0 – 1 0 1 ; B2,B1,B0 – 1 0 0 . Cin = 0. Multiplication operation is performed between the two 3-bit inputs. The output for the operation is of 6bits.

P5 , P4 , P3 , P2 , P1 , P0 – 0 1 0 1 0 0 .

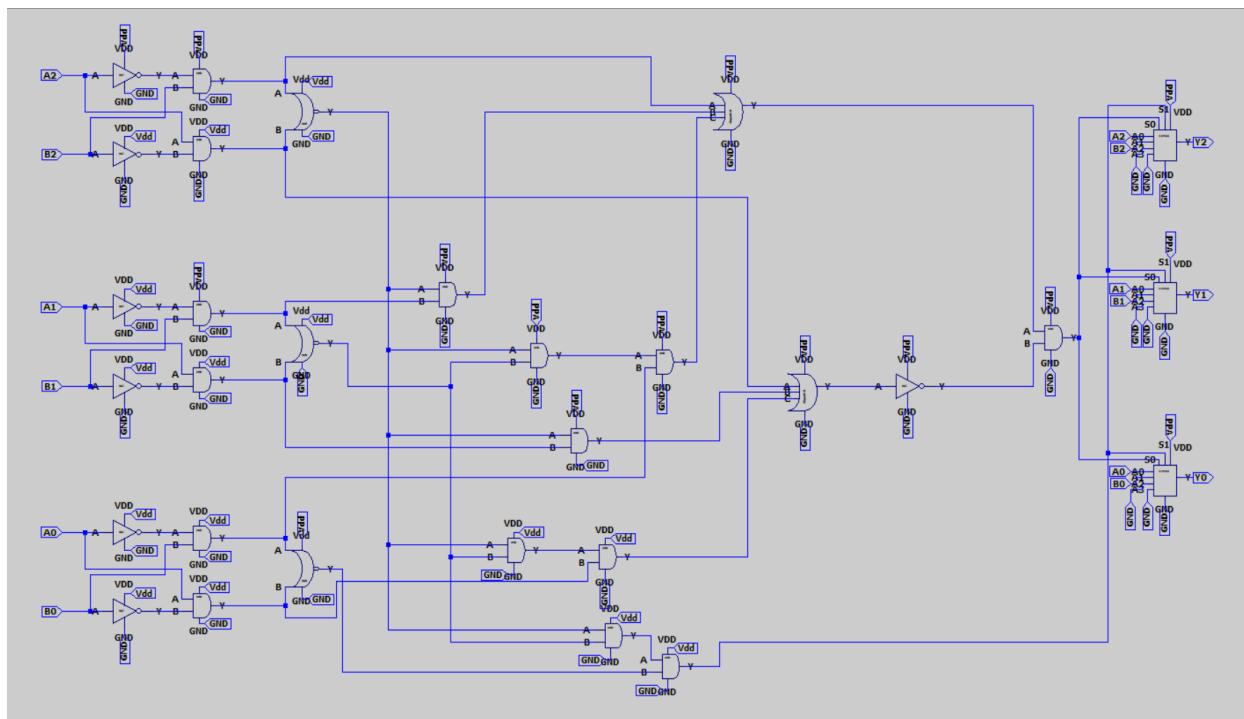
The calculated test case output values match with the waveform values generated by the test case circuit for the MULTIPLICATION operation. This verifies that the MULTIPLICATION unit works properly.

## GREATER THAN

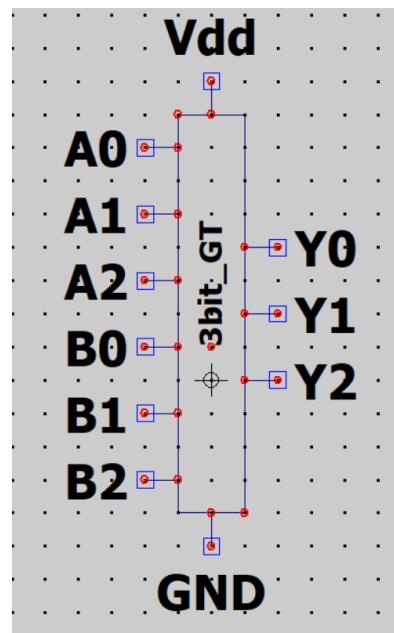
Separate gate level circuit diagram



Symbol Schematic



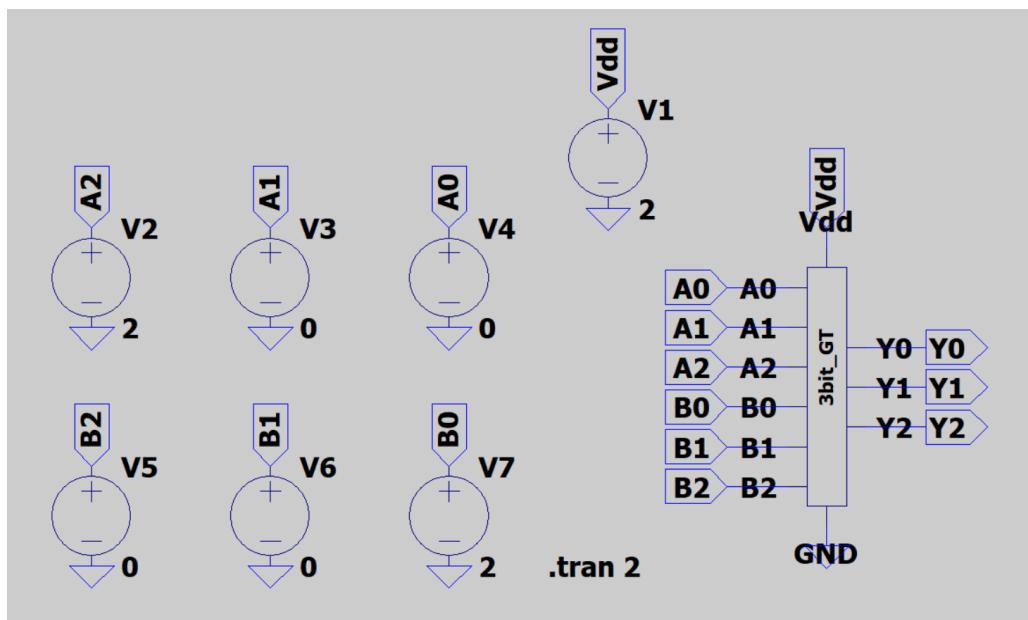
## Symbol drawing/shape



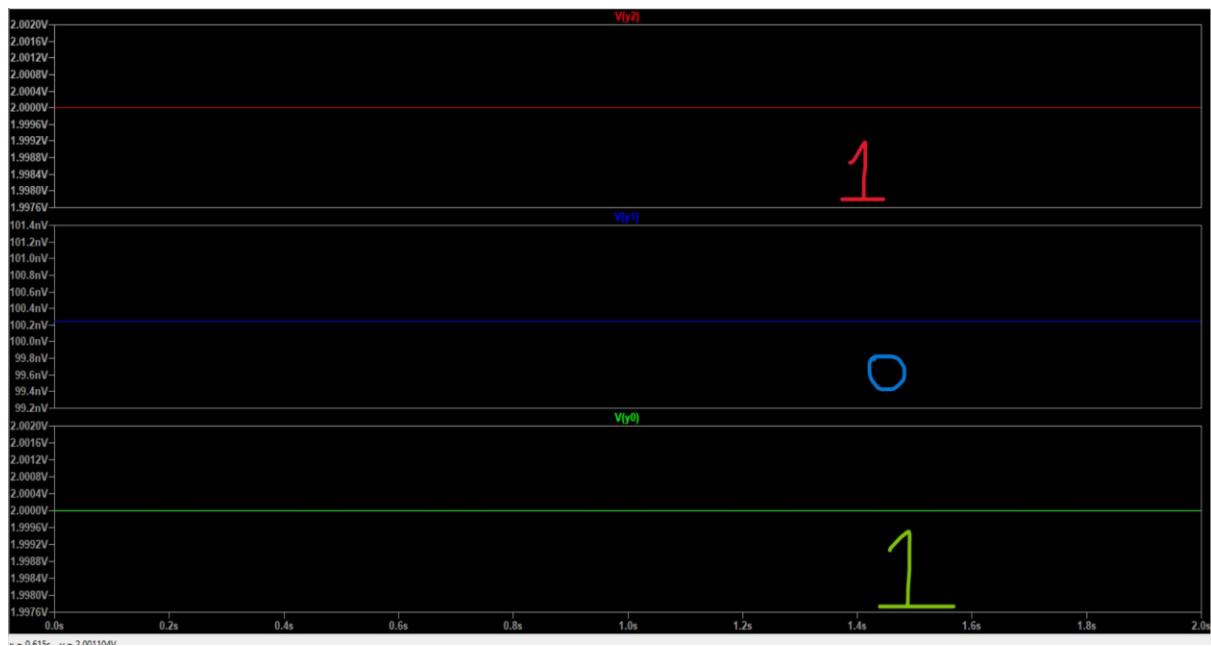
## Test case calculations

$$\begin{array}{r}
 101 - A_2\ A_1\ A_0 \\
 001 - B_2\ B_1\ B_0 \\
 \hline
 (A - B) = 101 - Y_2\ Y_1\ Y_0
 \end{array}$$

## Test circuit



## Test circuit waveform



## Verification Statement

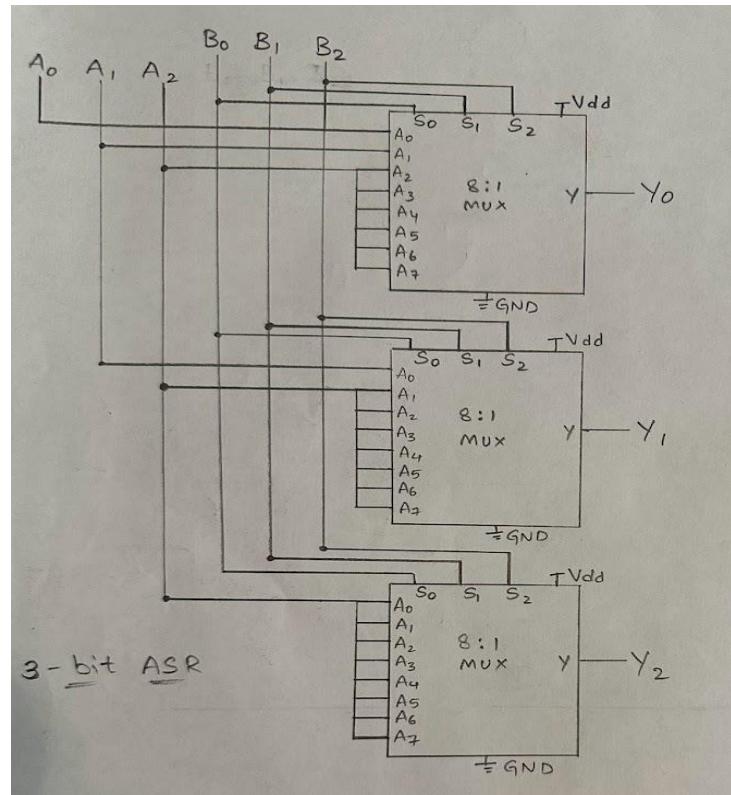
The generated waveform outputs for the 3-bit inputs  $A_2, A_1, A_0 = 1\ 0\ 1$ ;  $B_2, B_1, B_0 = 0\ 0\ 1$  for GT operation are  $Y_2, Y_1, Y_0 = 1\ 0\ 1$ . And our calculated output is also  $1\ 0\ 1$ .

Waveform values for the GREATER THAN operation match the expected output values from the calculations.

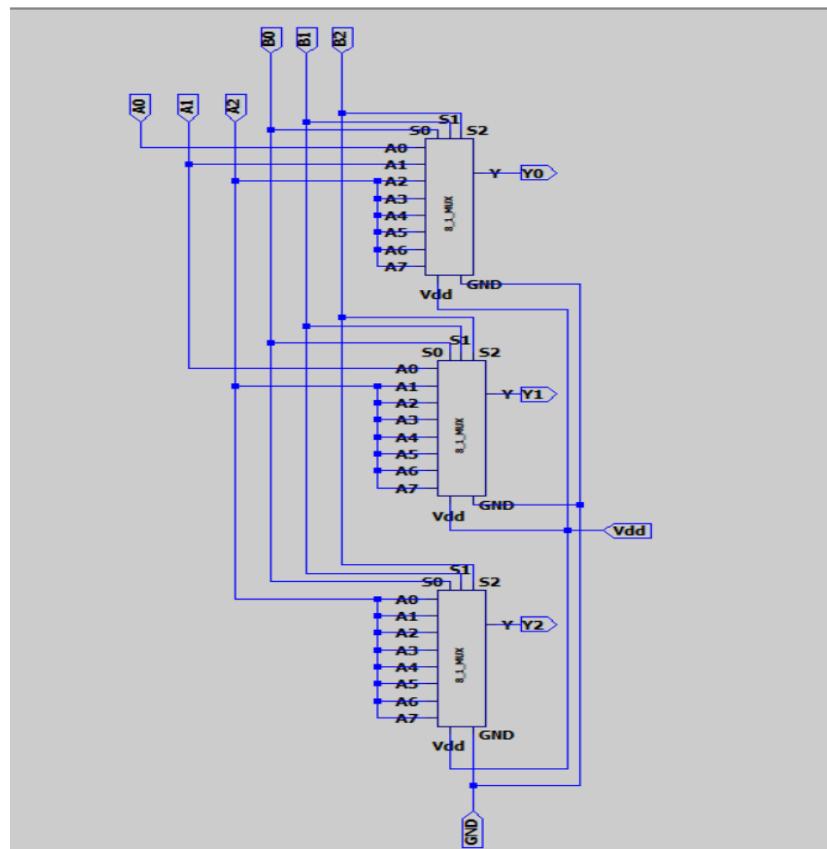
This verifies that the GT unit device works properly.

## ARITHMETIC SHIFT RIGHT

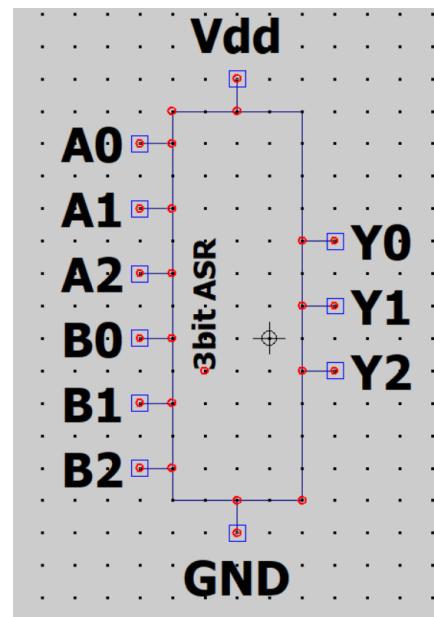
Separate gate level circuit diagram



Symbol schematic



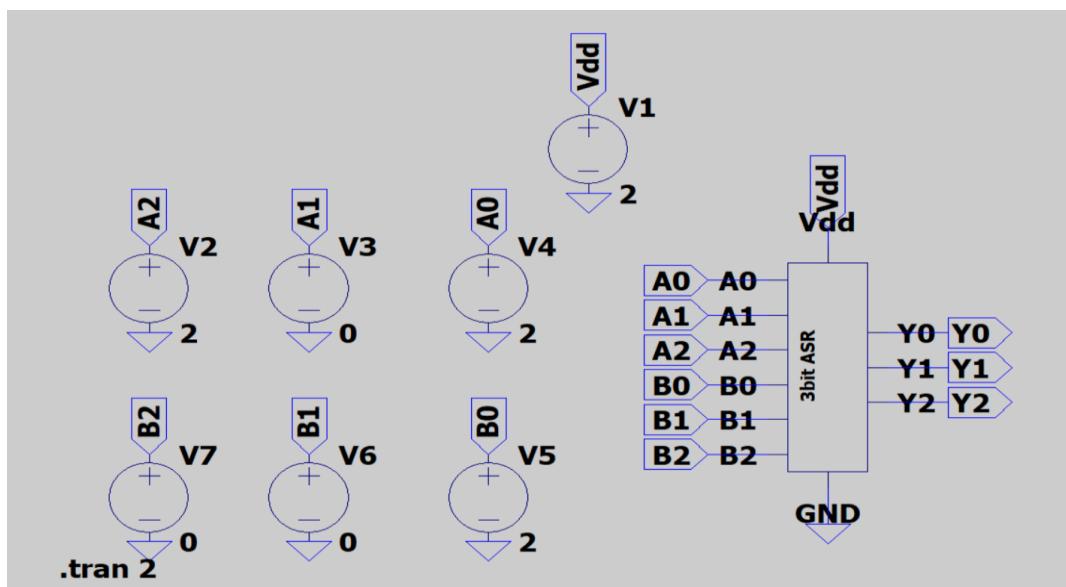
## Symbol drawing/shape



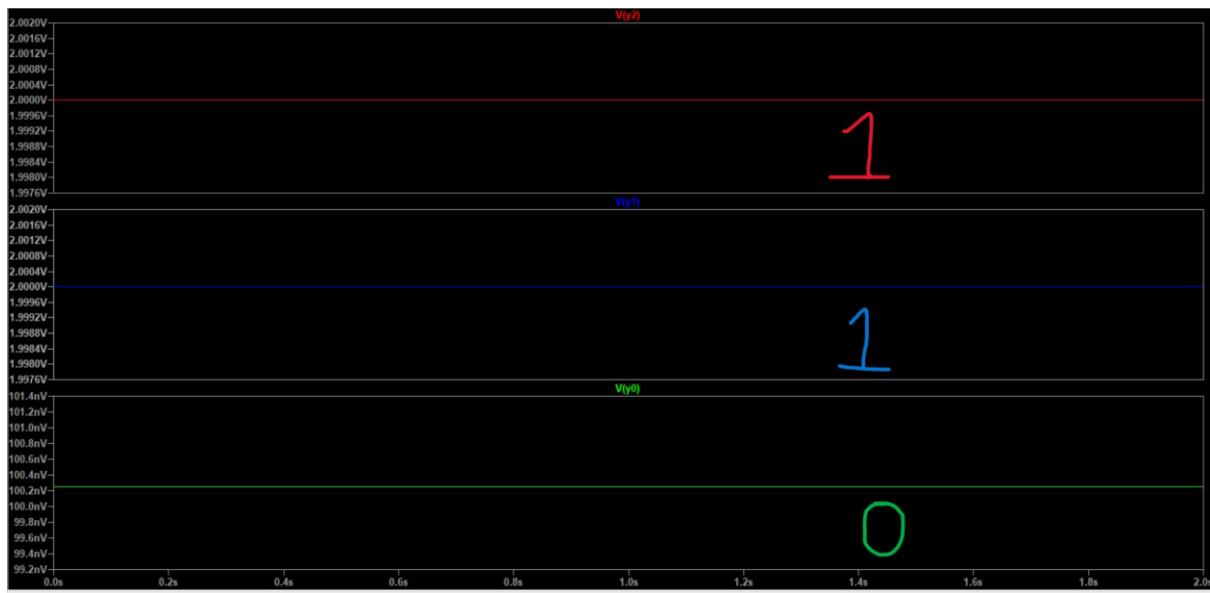
## Test case calculations

$1 \ 0 \ 1 - A_2 \ A_1 \ A_0$   
 $0 \ 0 \ 1 - B_2 \ B_1 \ B_0$   
 ASR, shifting 1 bit to right  
 $\Rightarrow \ 1 \ 1 \ 0 - Y_2 \ Y_1 \ Y_0$

## Test circuit



## Test circuit waveforms



## Verification Statement

3 bit Input A2,A1,A0 – 1 0 1 is arithmetically shifted to right side by one bit. (i.e., values of B2,B1,B0 – 0 0 1).

The calculated output values for the ASR operation match with the generated output waveforms of the test circuit used. Hence the operation unit ASR works properly and is verified.

## NOTE

For all the CU's operated above and the operational units

The inputs are:

A2 , A1 , A0 (**A2** is considered as the **MSB** ; and **A0** is considered as the **LSB**)

B2 , B1 , B0 (**B2** is considered as the **MSB** ; and **B0** is considered as the **LSB**)

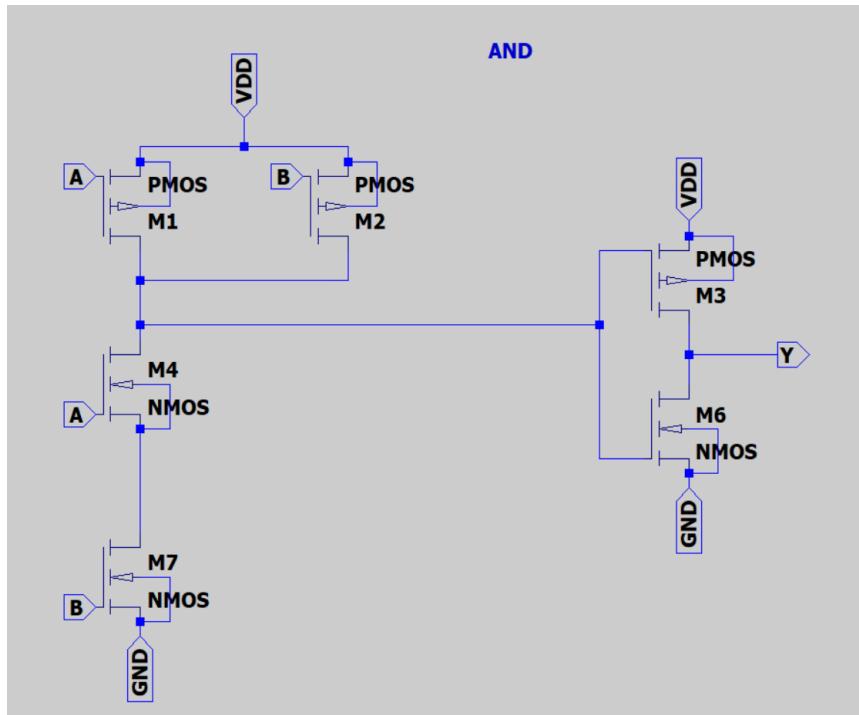
The output's are:

Y2 , Y1 , Y0 (**Y2** is considered as the **MSB** ; and **Y0** is considered as the **LSB**)

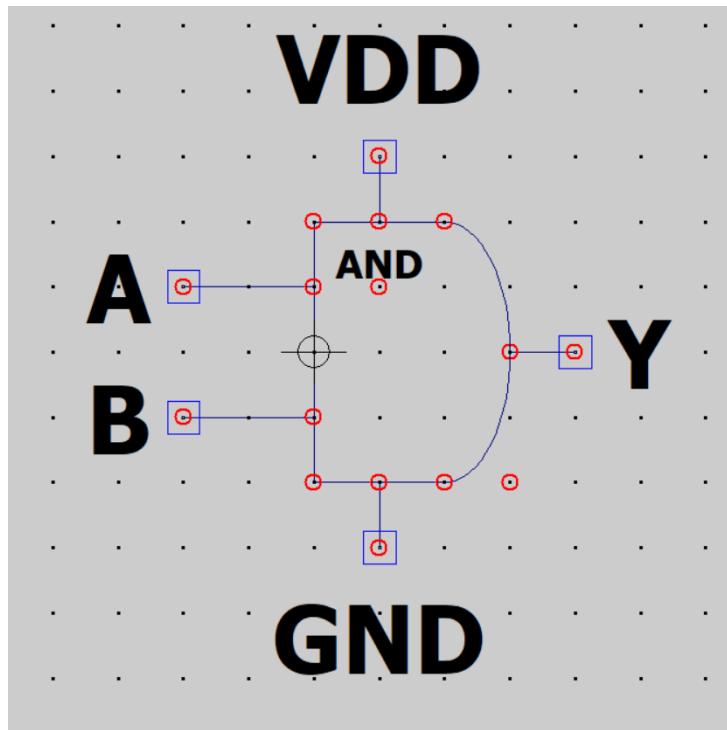
## APPENDIX

### AND

Schematic

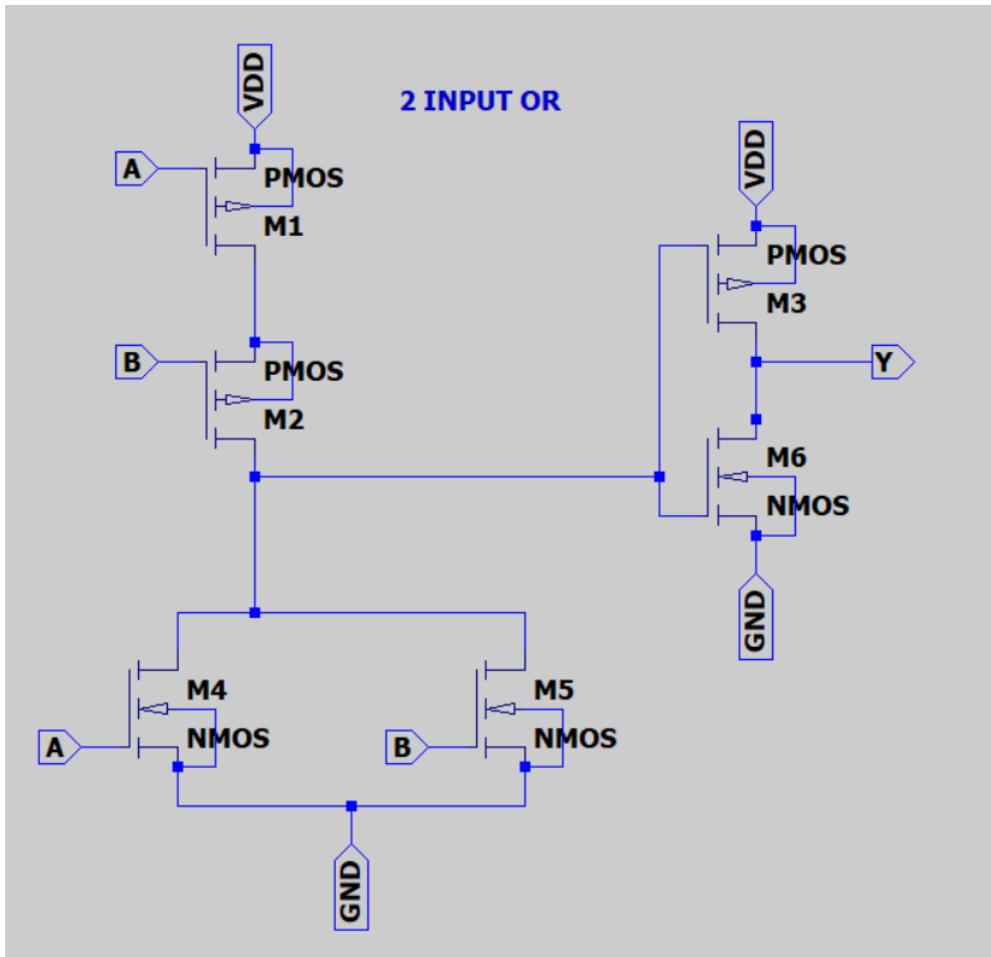


Symbol

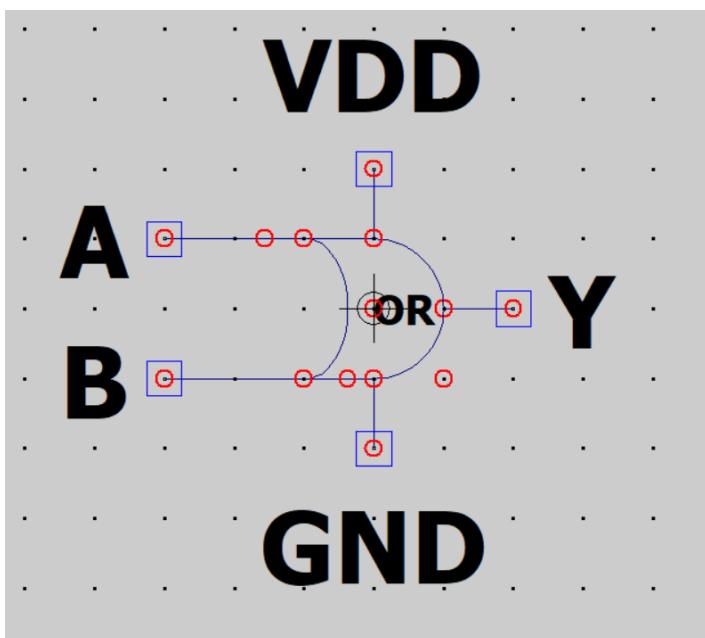


## OR

Schematic

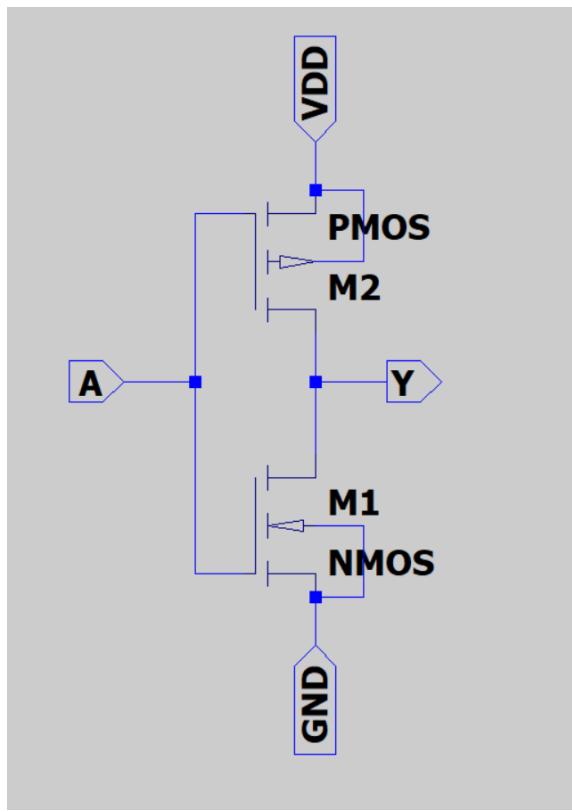


Symbol

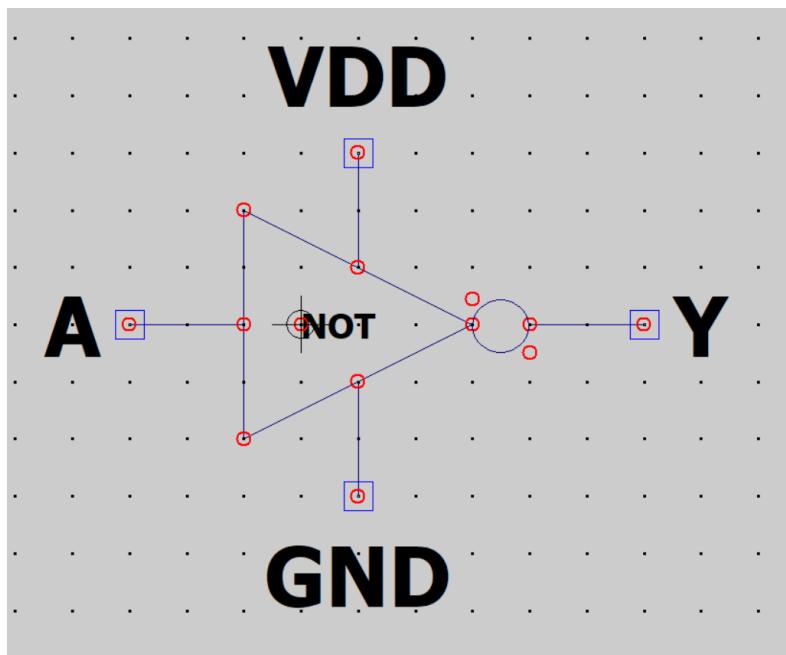


**NOT**

Schematic

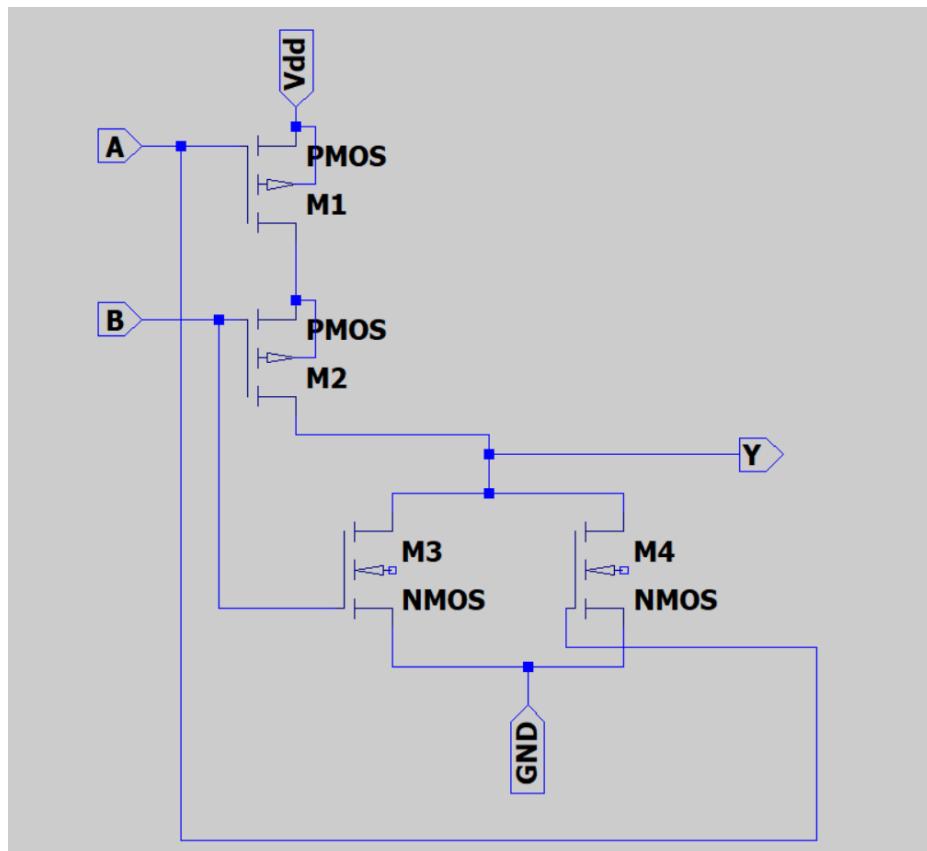


Symbol

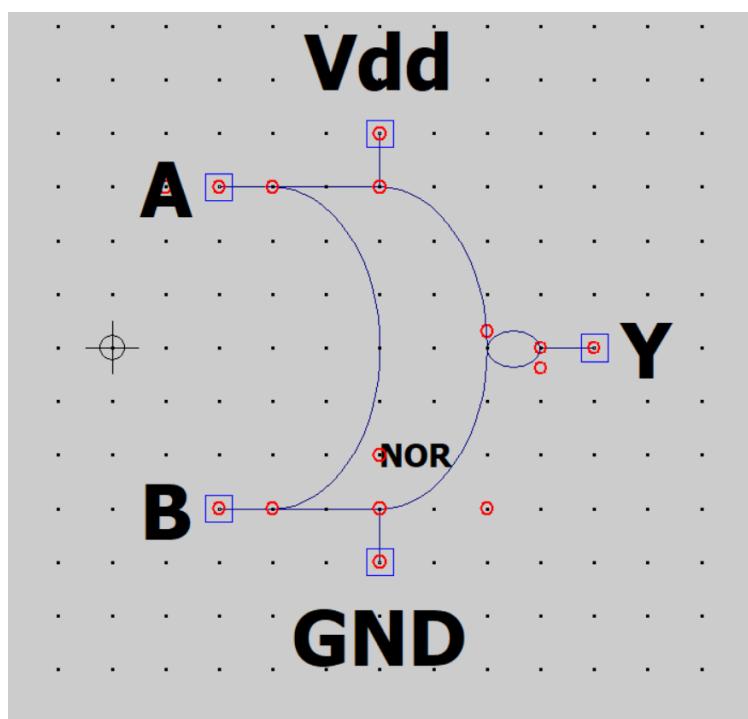


## NOR

Schematic

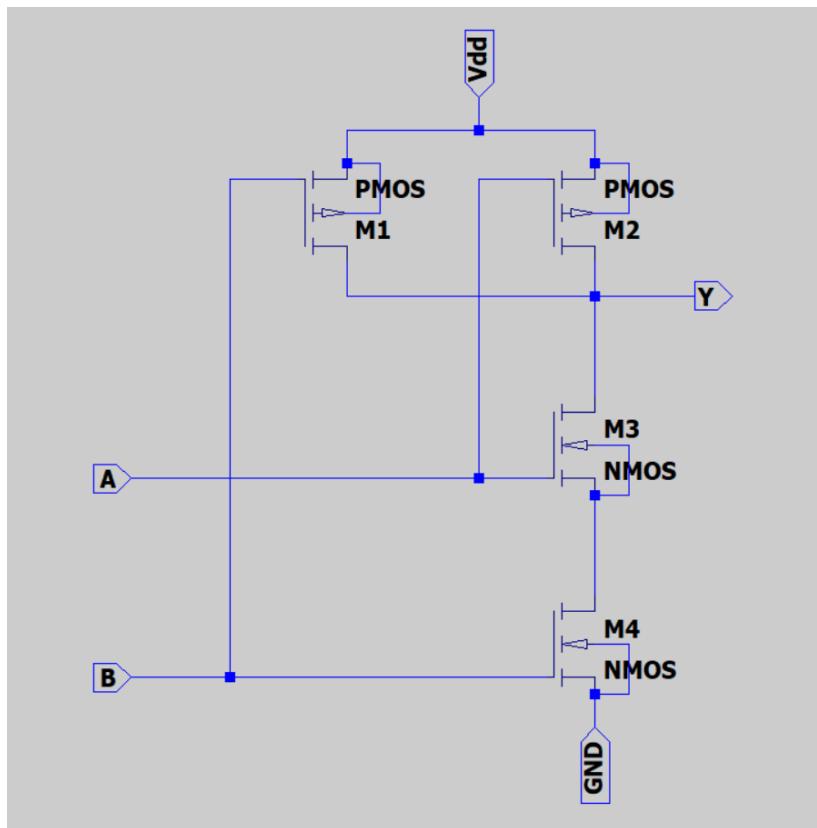


Symbol

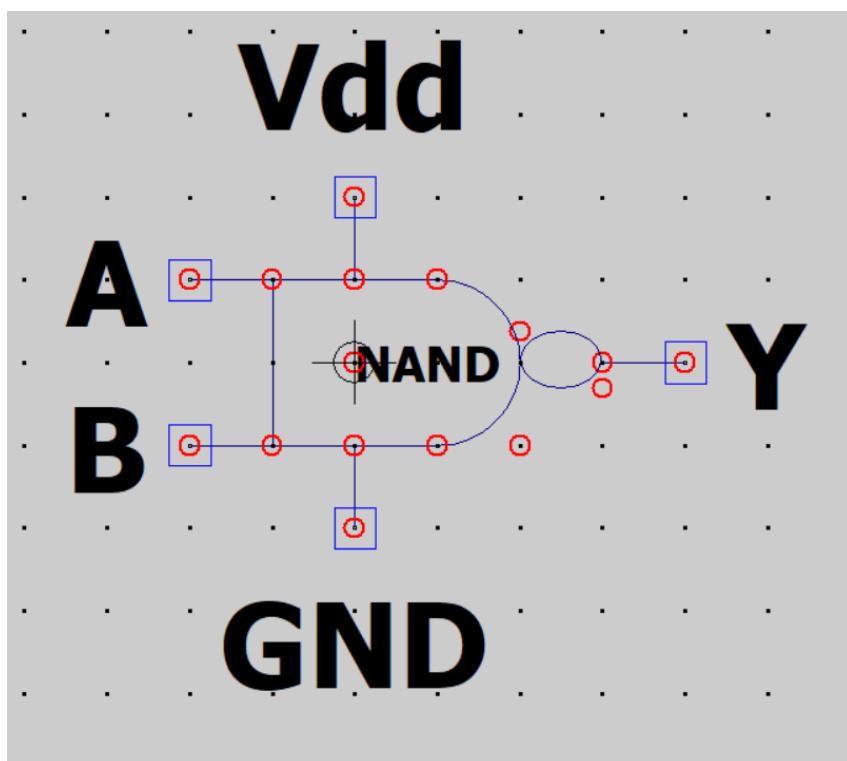


## NAND

Schematic

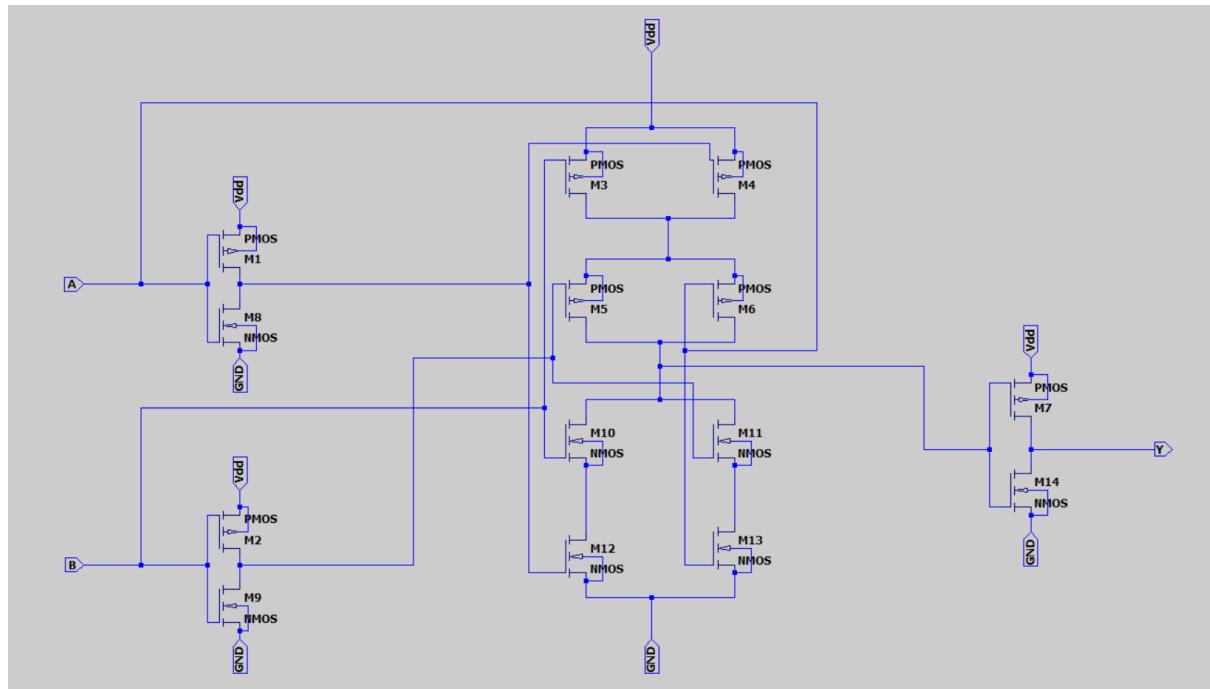


Symbol

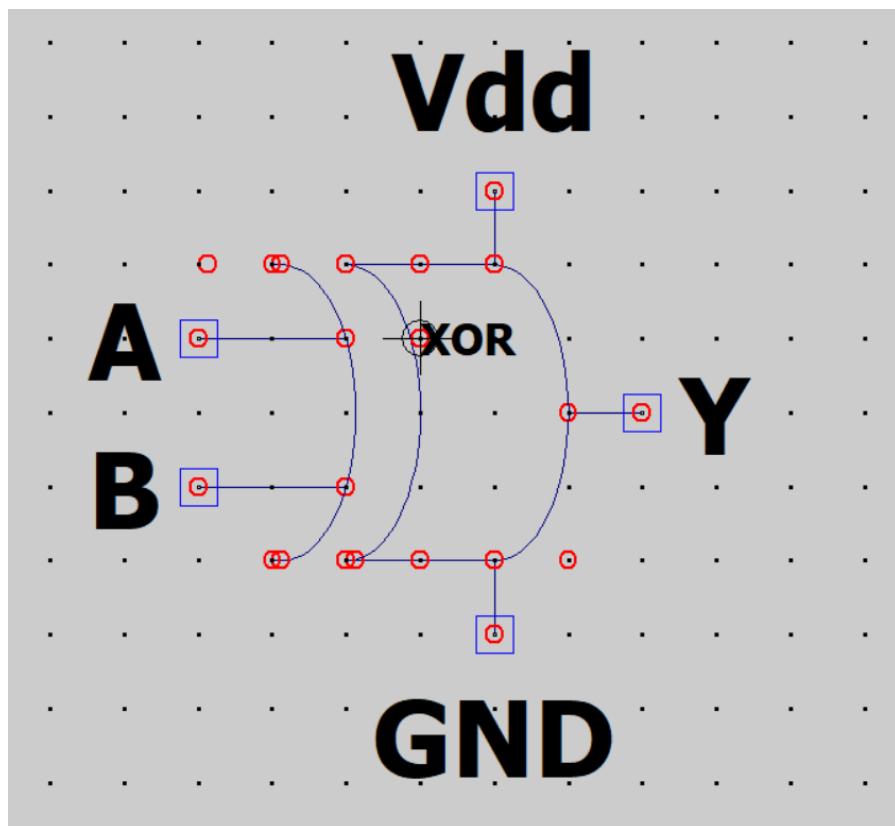


## XOR

Schematic

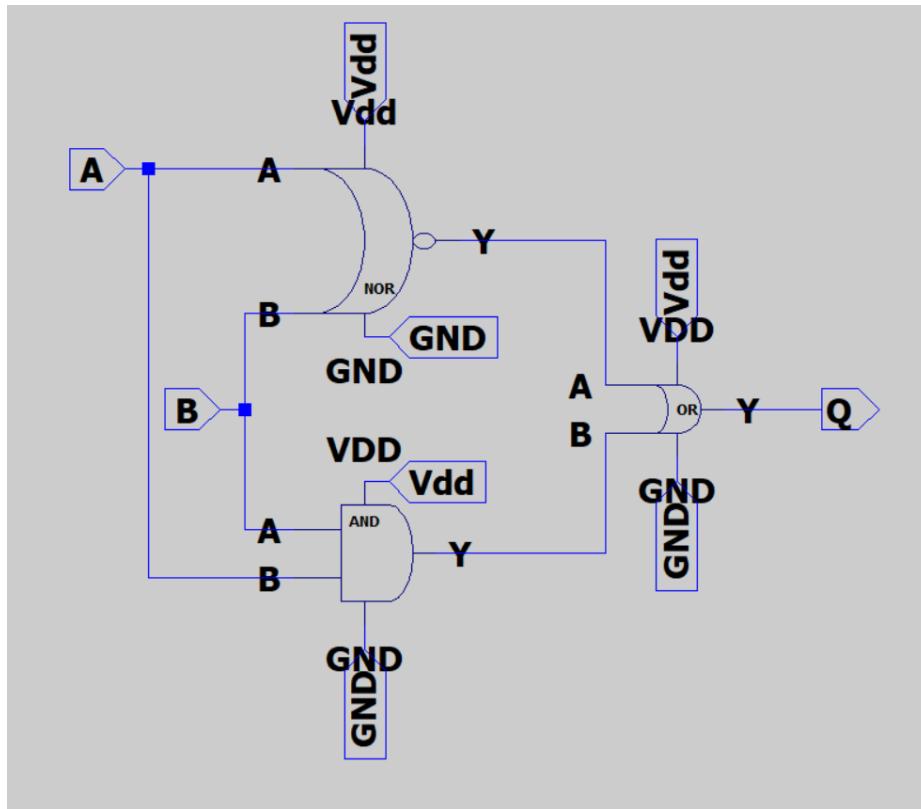


Symbol

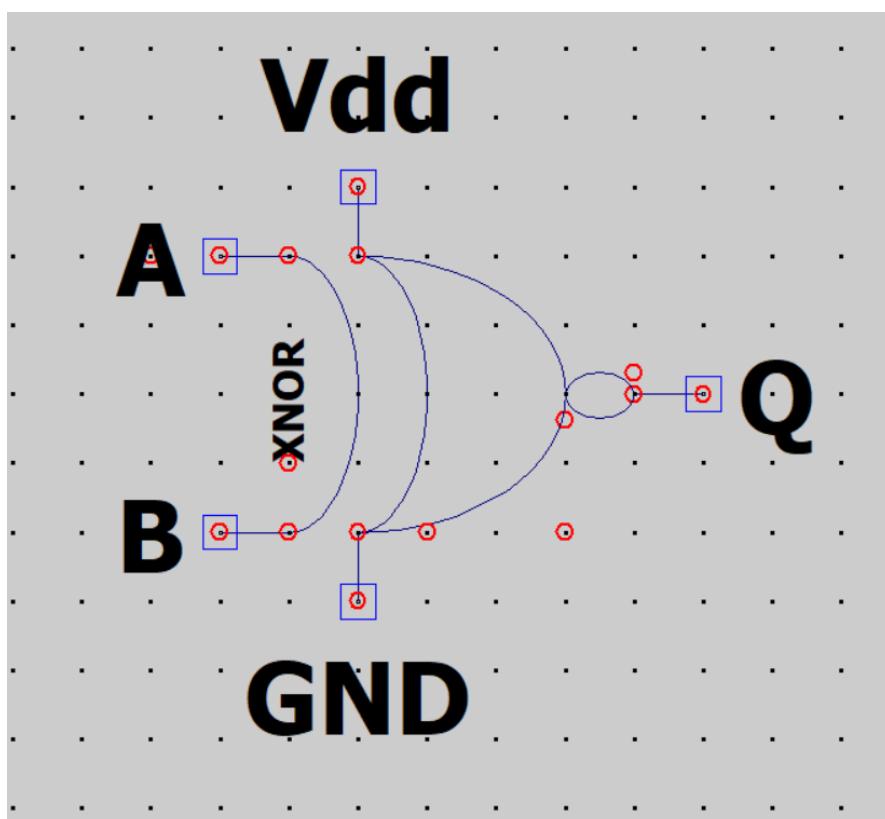


## XNOR

Schematic

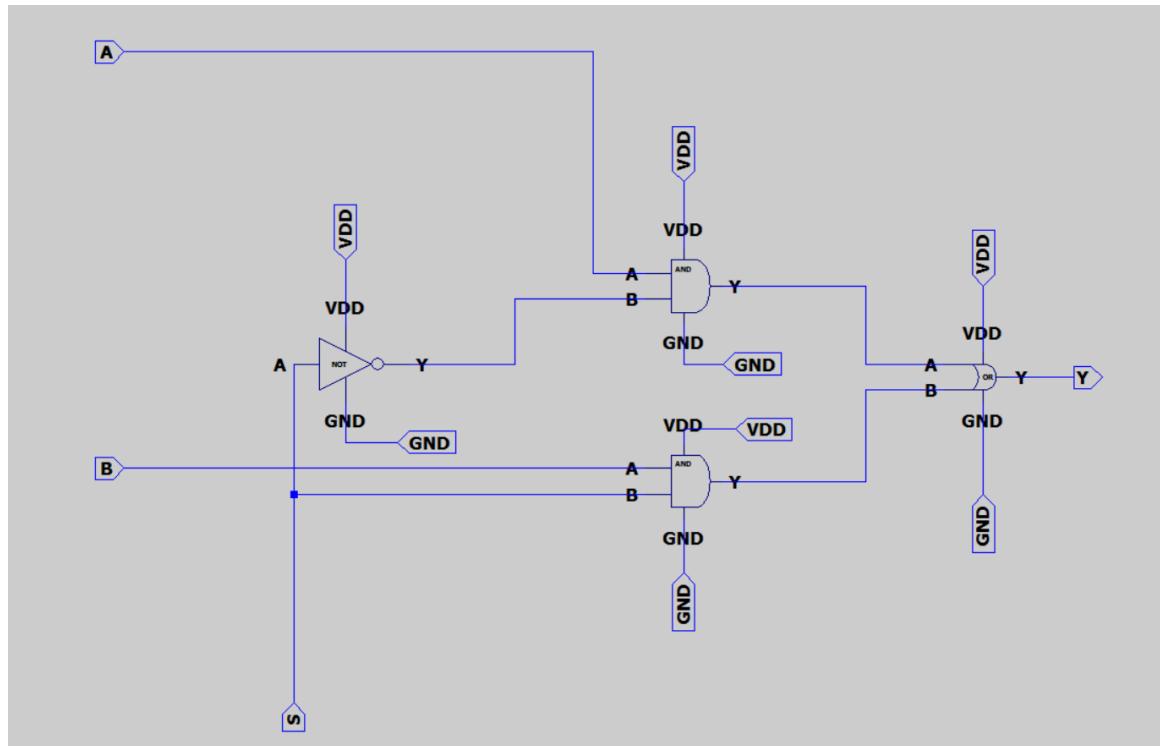


Symbol

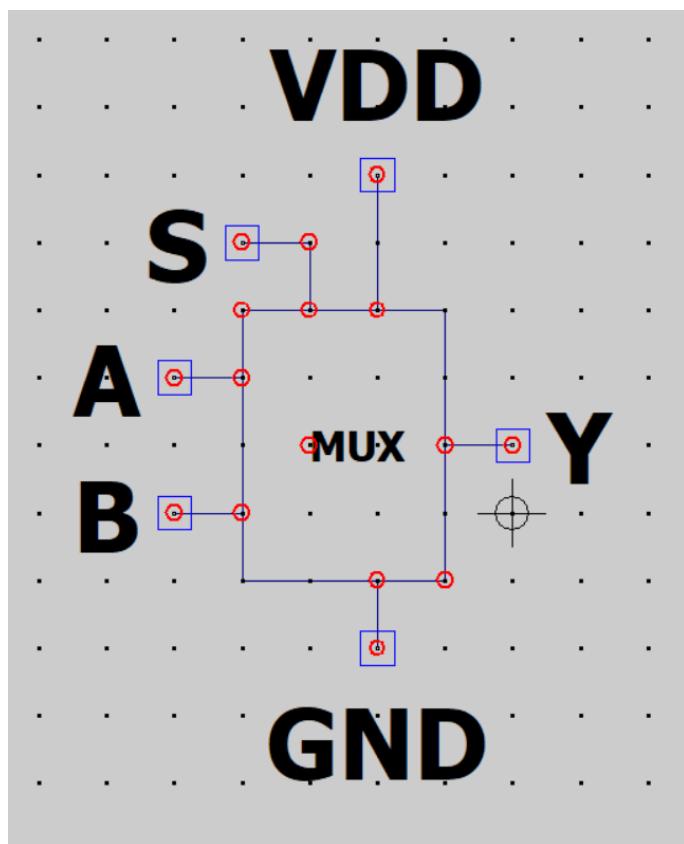


## 2:1 MUX

Schematic

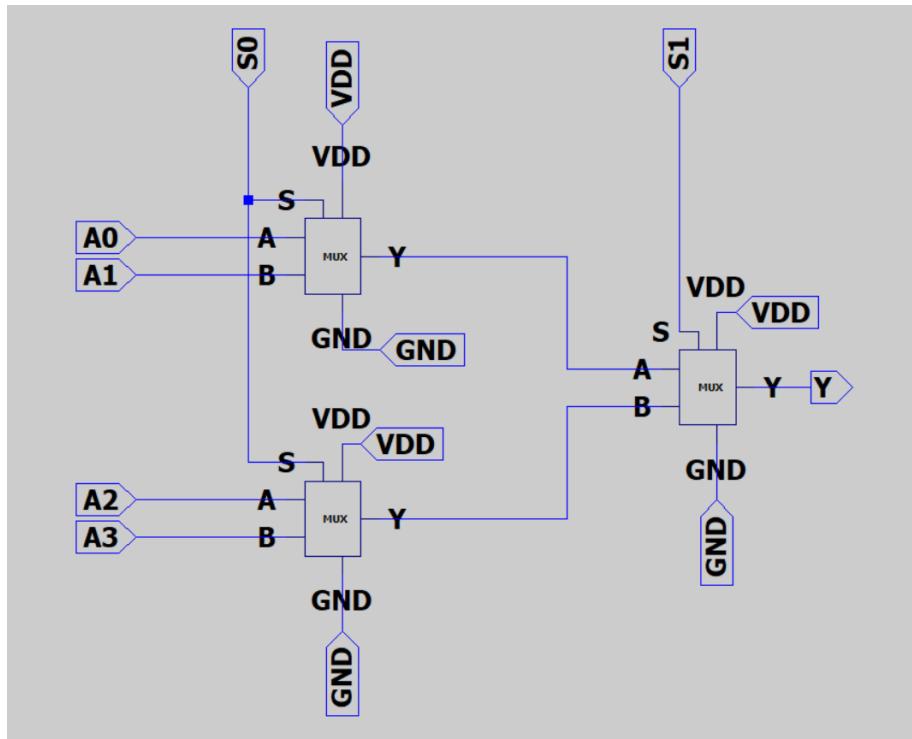


Symbol

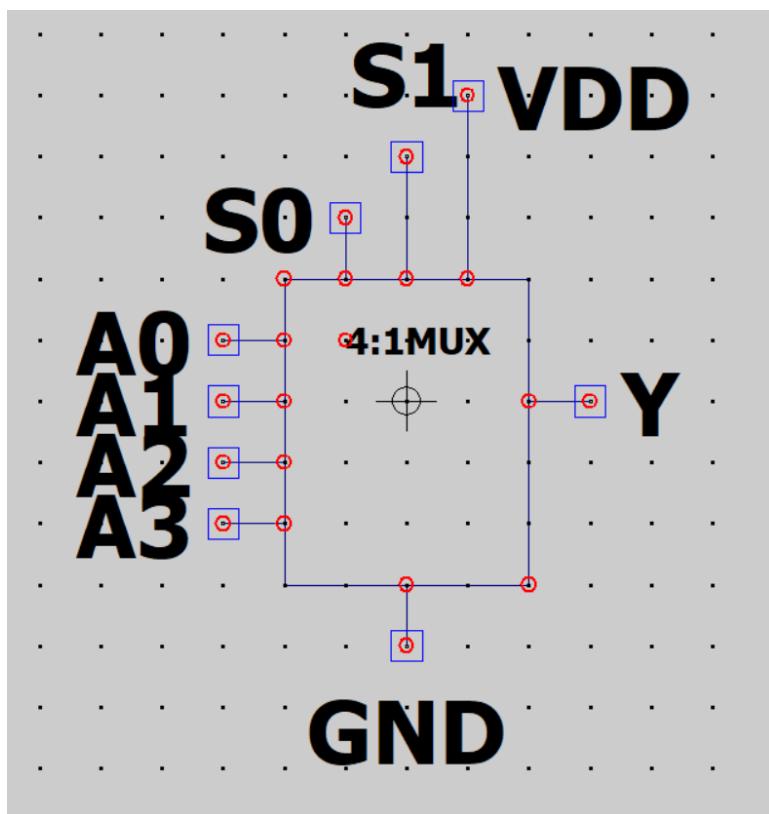


## 4:1 MUX

Schematic

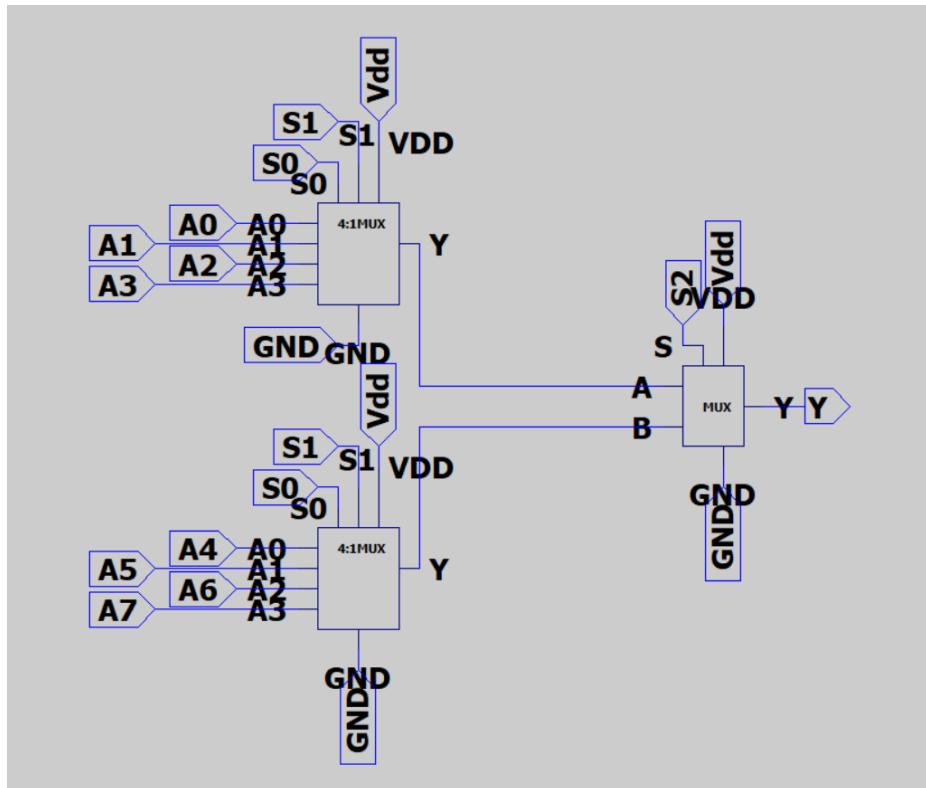


Symbol

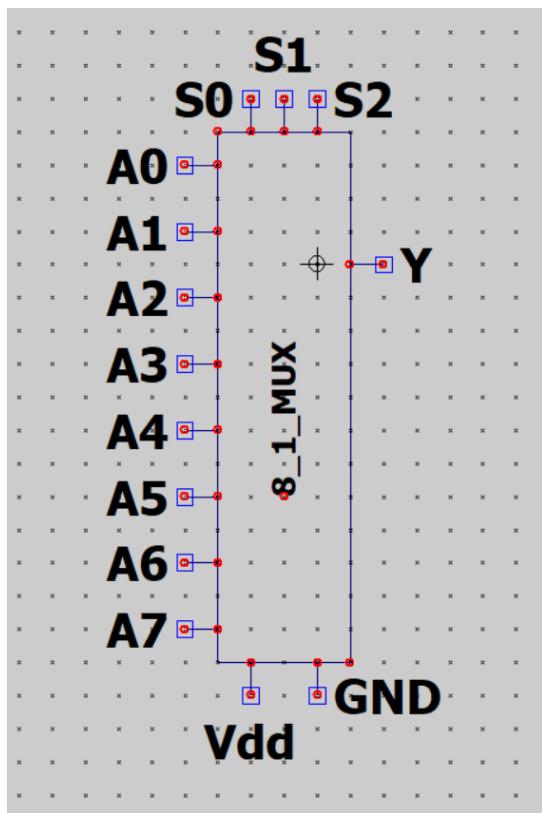


## 8:1 MUX

Schematic

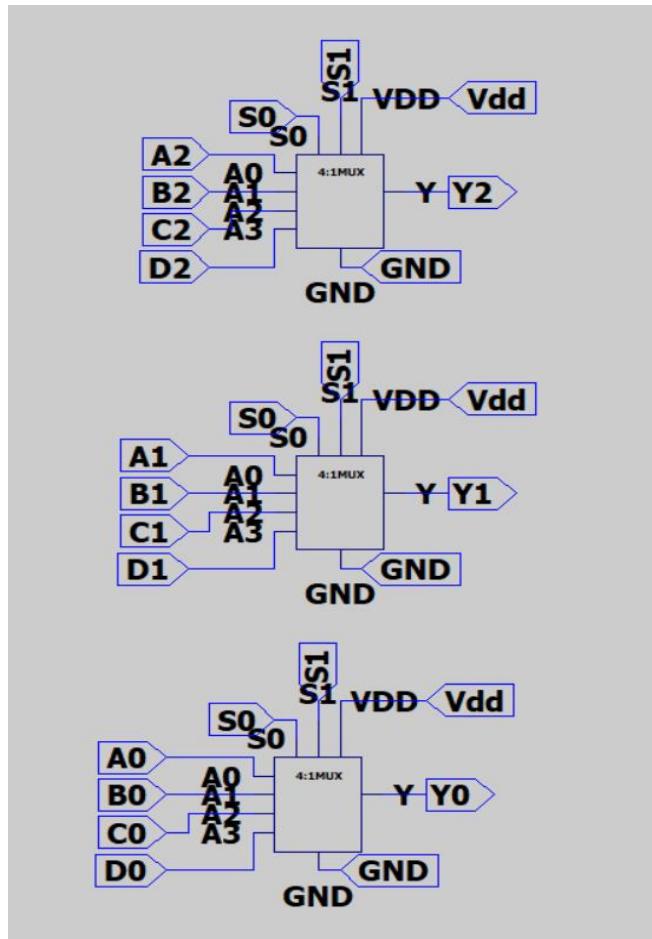


Symbol

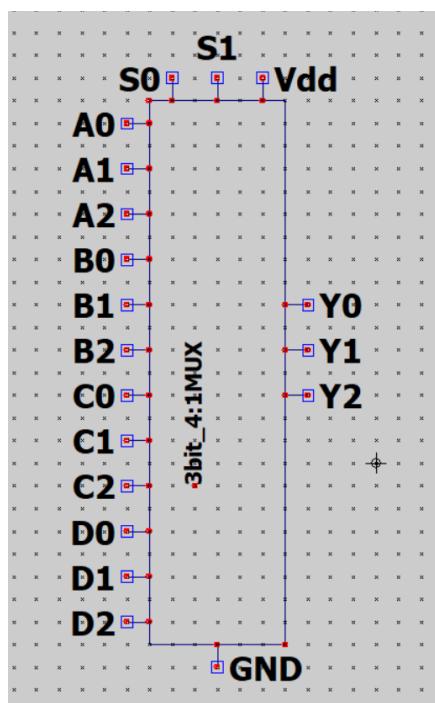


## 3-bit 4:1 MUX

Schematic

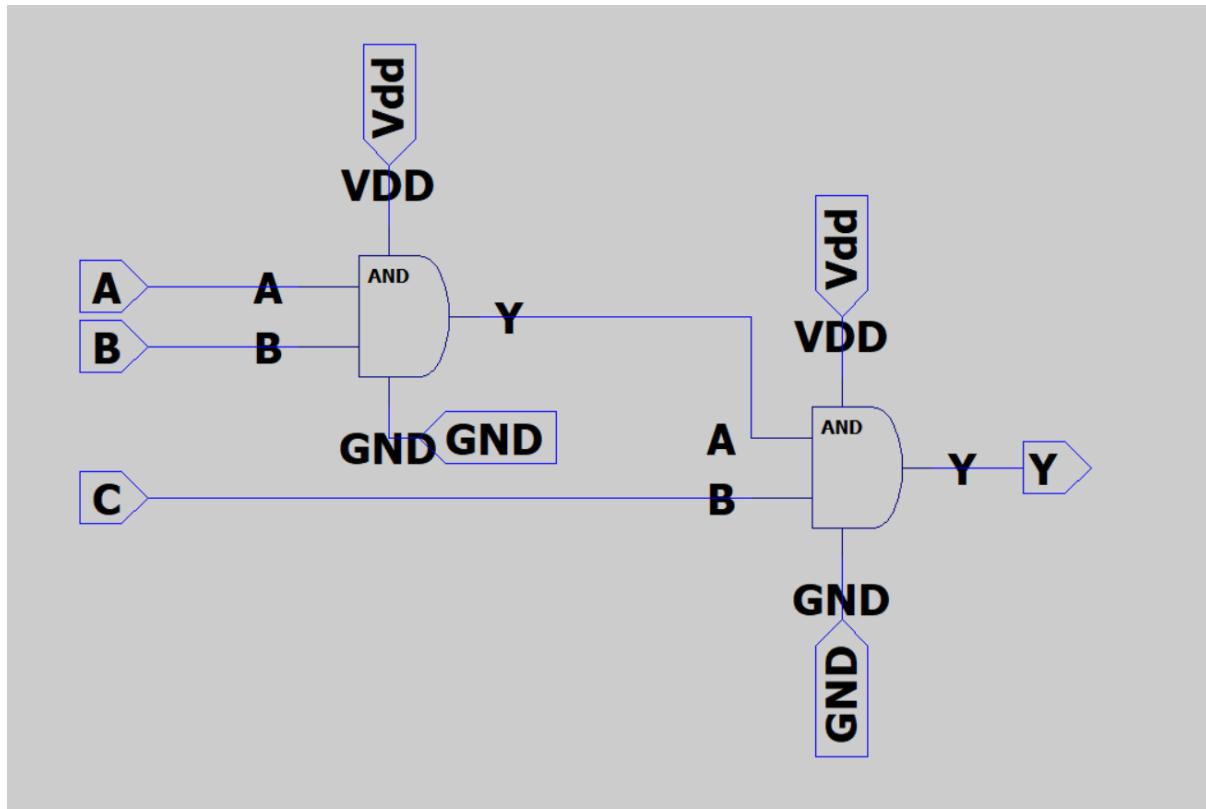


Symbol

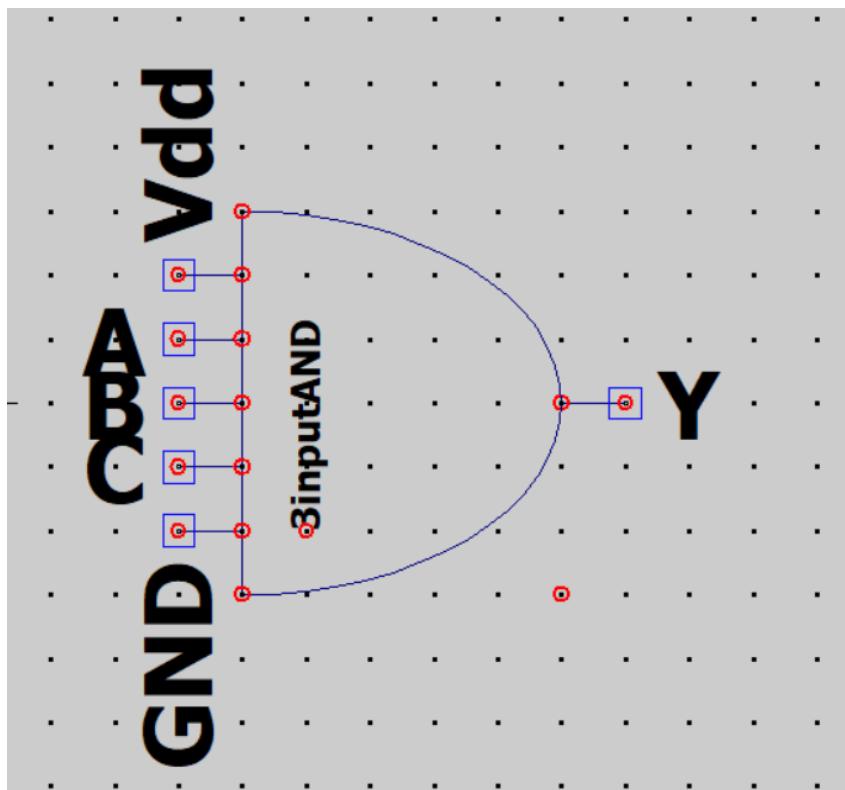


### 3 input AND

Schematic

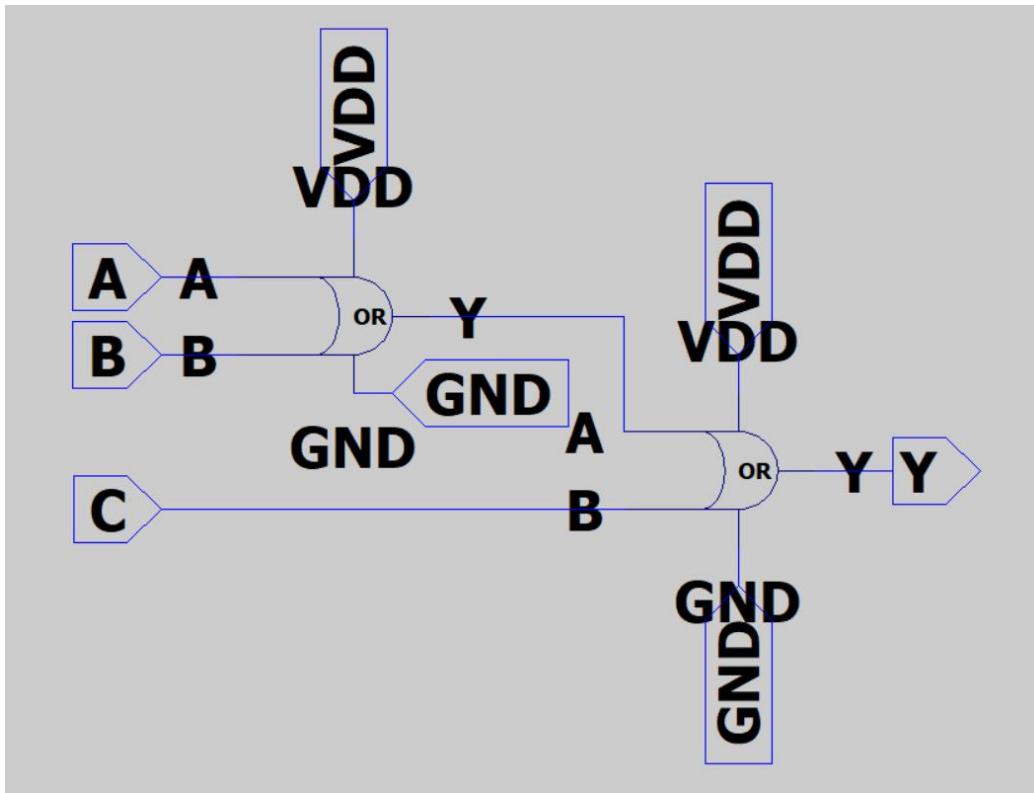


Symbol

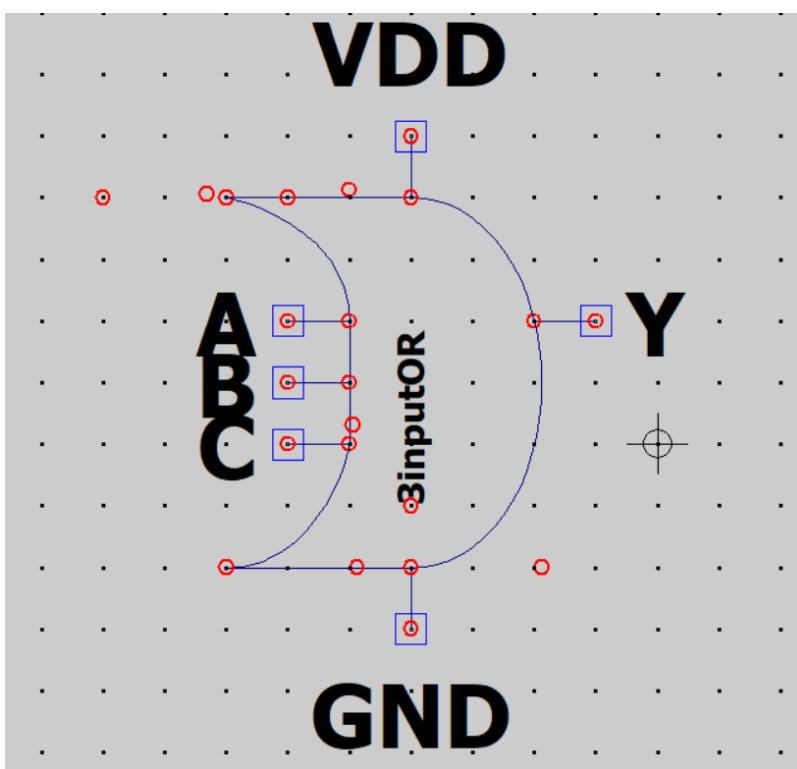


### 3 input OR

Schematic

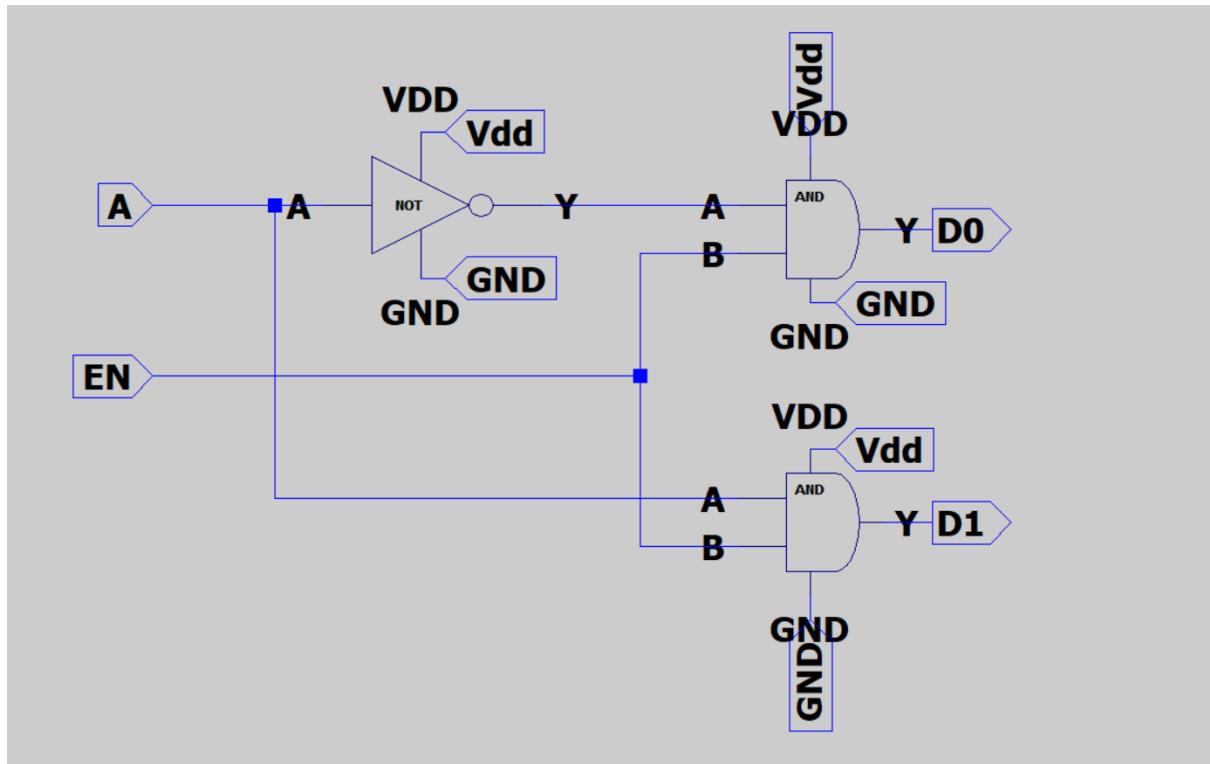


Symbol

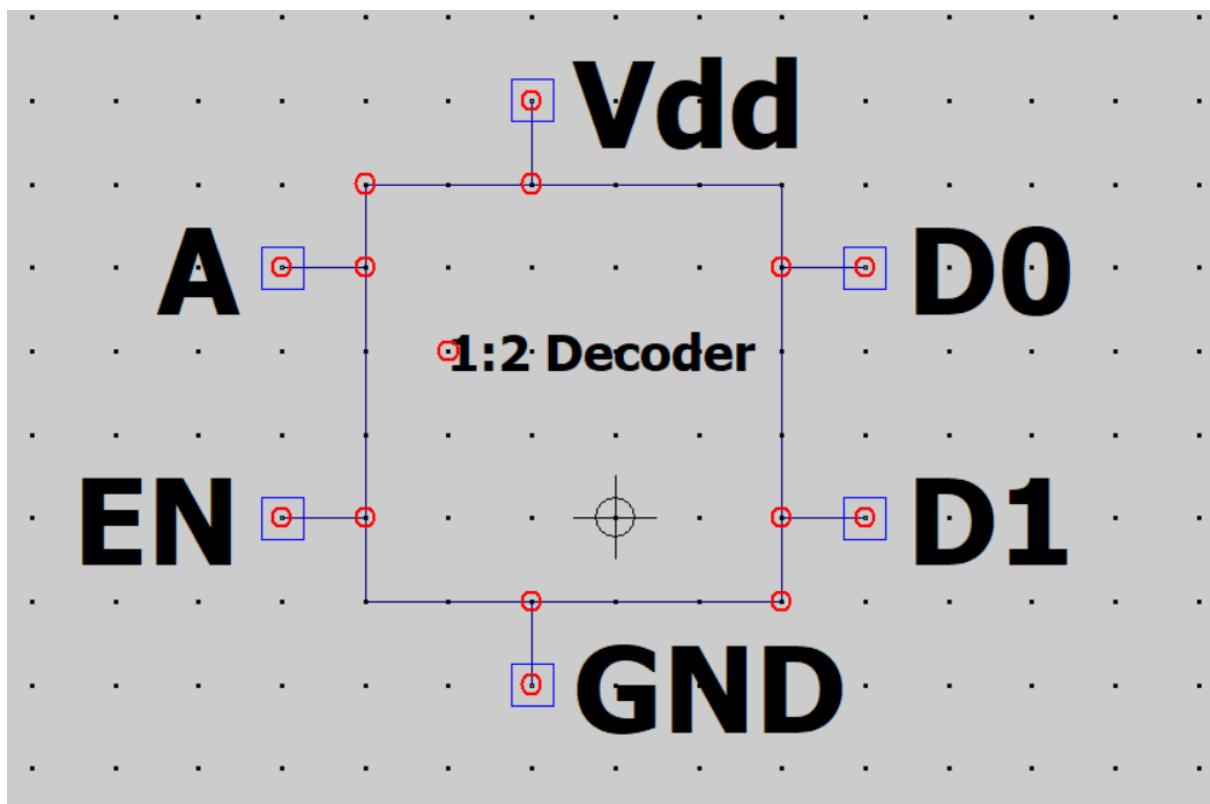


## 1:2 DECODER

Schematic

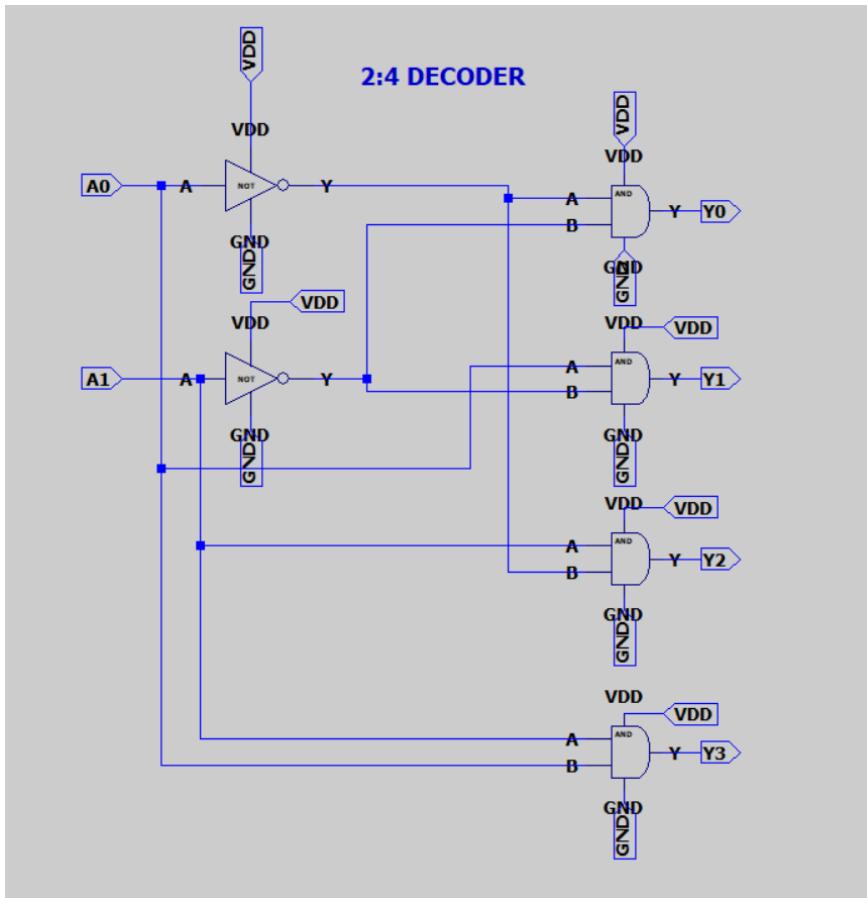


Symbol

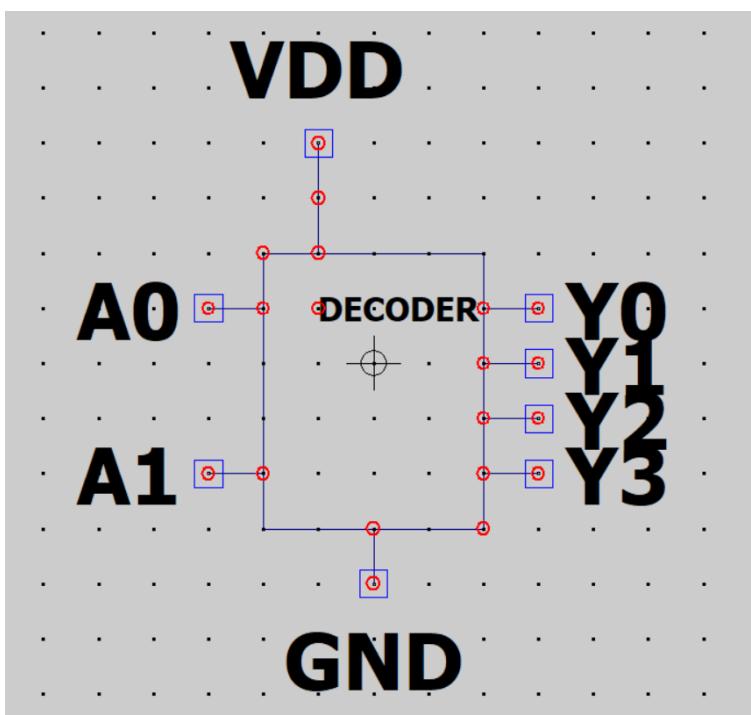


## 2:4 DECODER

Schematic

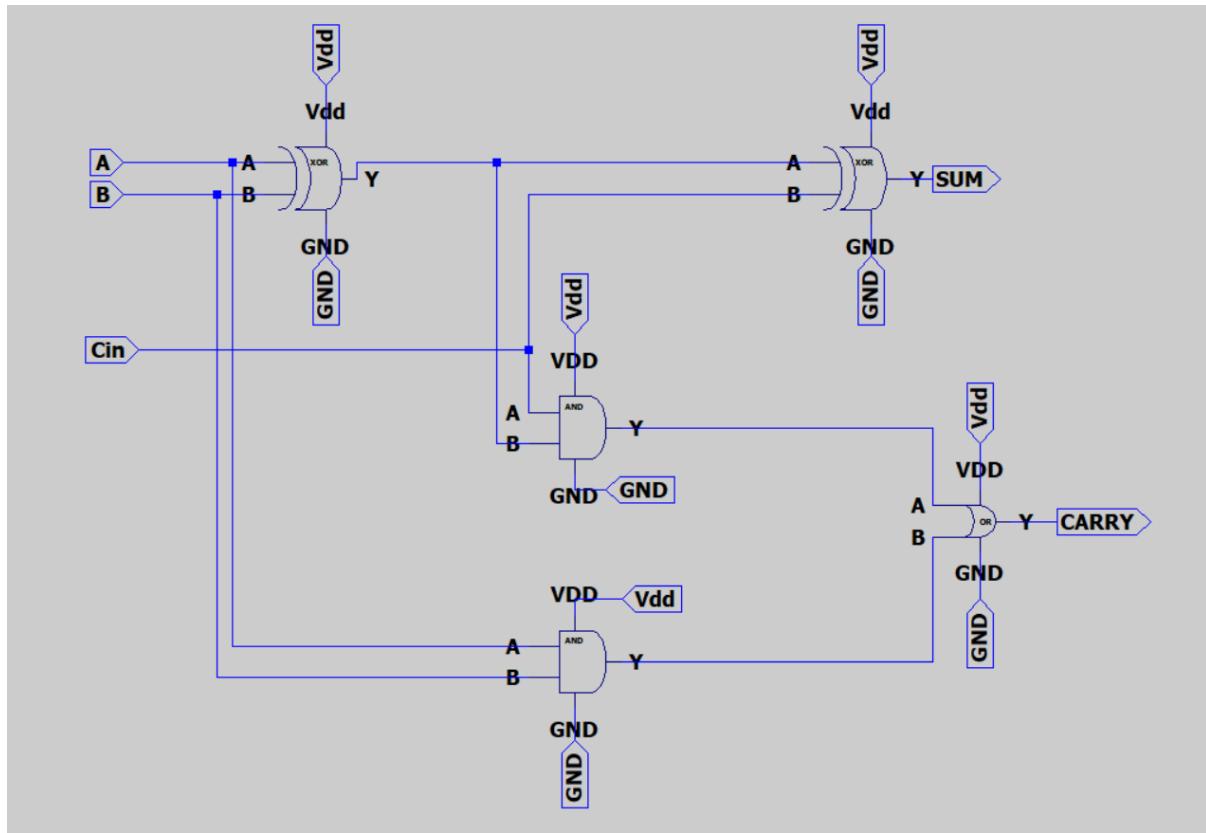


Symbol

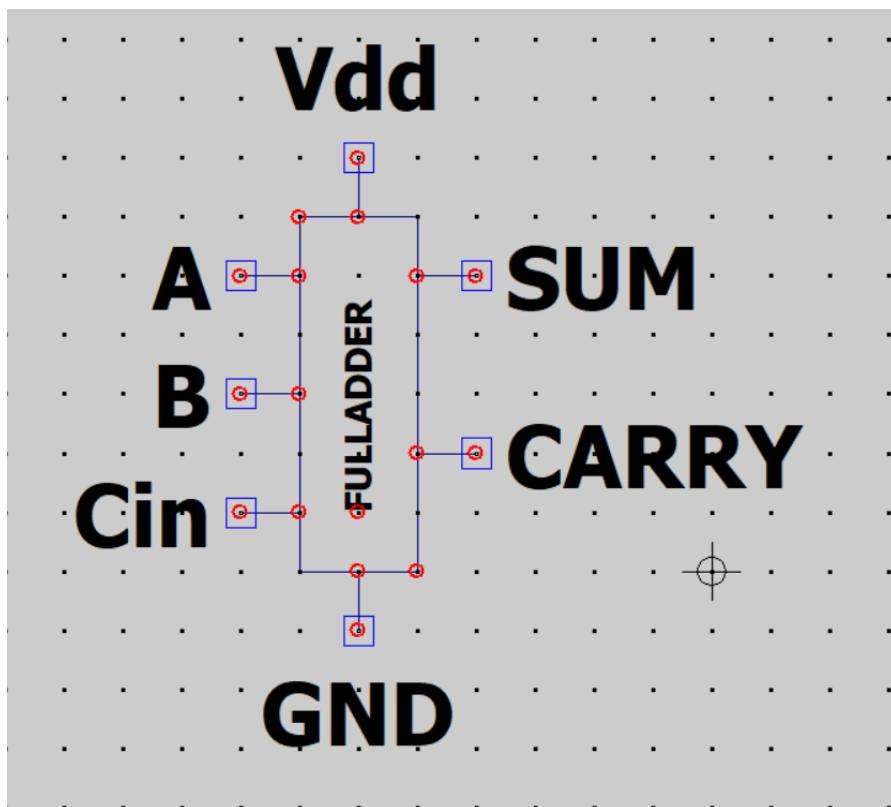


## FULL ADDER

Schematic



Symbol



## NOTE's from the DEMO Session

For the Second Test case Prof. Mehta asked me to show o/p from the Part – 1 CU for the Multiplication Operation for  $2 \times 2$ .

But due to a excited confusion, I have operated for the Greater than Operation value and presented the o/p waveforms before Prof. and TA.

The correct operation has been made and I hope the grader consider this while evaluating.

For ref, I am adding a screenshot of the same.

