```
----------------------------------------------------------------------
--------------
-- Company:
-- Engineer:
--
-- Create Date: 17.04.2023 22:48:37
-- Design Name:
-- Module Name: Mux4to1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------
--------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.NUMERIC_STD.ALL;
use ieee.std_logic_unsigned.all;

ENTITY Mux4to1 IS
    PORT (
          J0,J1,J2,J3:IN STD_LOGIC_VECTOR(3 DOWNTO 0);  --mux
inputs
          J: OUT STD_LOGIC_VECTOR(3 DOWNTO 0);          --mux
output
          MSL4:IN STD_LOGIC_vector(1 downto 0)          --mux
selector
             );
```

```
END ENTITY;

ARCHITECTURE BEHAVIORAL OF Mux4to1 IS
BEGIN
    PROCESS(J0,J1,J2,J3,MSL4)
    BEGIN
        CASE (MSL4) IS
            WHEN "00" =>  J<= J0;
            WHEN "01" =>  J<= J1;
            WHEN "10" =>  J<= J2;
            WHEN "11" =>  J<= J3;
           WHEN OTHERS =>
           J<= "0000";
        END CASE;
    END PROCESS;
END BEHAVIORAL;
```