```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.NUMERIC_STD.all;

entity FINAL is

port(
N1,N2,N3,N4,N5,R1,R2,R3,R4,R5:in std_logic_vector(3 downto 0);
--input's for fabric
Sel1,Sel2,Sel3,Sel4,Sel5,Sel6,Sel7,Sel8,Sel9,Sel10,Sel11,Sel12,Sel1
3,Sel14,Sel15,Sel16,Sel17,Sel18,Sel19,Sel20,Sel21,Sel22,Sel23,Sel24
,Sel25: in std_logic_vector(4 DOWNTO 0); --Selector's of CU_1 to
CU_25
MSL8_1,MSL8_2,MSL8_3,MSL8_4: in std_logic_vector(2 DOWNTO 0); --
Selector's for 8:1 muxes
MSL4_1,MSL4_2,MSL4_3,MSL4_4,MSL4_5,MSL4_6,MSL4_7,MSL4_8,MSL4_9,MSL4
_10,MSL4_11,MSL4_12: in std_logic_vector(1 DOWNTO 0); -- Selector's
for 4:1 muxes
MSL2_3,MSL2_4,MSL2_5,MSL2_6,MSL2_7,MSL2_8,MSL2_9,MSL2_10,MSL2_11,MS
L2_12,MSL2_13,MSL2_14,MSL2_15,MSL2_16,MSL2_17,MSL2_18,MSL2_19,MSL2_
20,MSL2_21,MSL2_22,MSL2_23,MSL2_24,MSL2_25,MSL2_26: in std_logic;
-- Selector's for 2:1 muxes
S21,S22,S23,S24,S25:out std_logic_vector(3 downto 0) --output's of
fabric
);
end FINAL;

architecture behavioral of FINAL is
SIGNAL
S1,S2,S3,S4,S5,S6,S7,S8,S9,S10,S11,S12,S13,S14,S15,S16,S17,S18,S19,
S20: std_logic_vector(3 DOWNTO 0); --output's of CU-1 to CU-20
respectively
SIGNAL
N6,R6,N7,R7,N8,R8,N9,R9,N10,R10,N11,R11,N12,R12,N13,R13,N14,R14,N15
,R15,N16,R16,N17,R17,N18,R18,N19,R19,N20,R20,N21,R21,N22,R22,N23,R2
3,N24,R24,N25,R25: std_logic_vector(3 DOWNTO 0); --inputs for CU's
```

```
6 to 25
begin

ALU1:entity work.ALU
    port map(N=>N1,R=>R1,Sel=>Sel1,S=>S1);

ALU2:entity work.ALU
    port map(N=>N2,R=>R2,Sel=>Sel2,S=>S2);

ALU3:entity work.ALU
    port map(N=>N3,R=>R3,Sel=>Sel3,S=>S3);

ALU4:entity work.ALU
    port map(N=>N4,R=>R4,Sel=>Sel4,S=>S4);

ALU5:entity work.ALU
    port map(N=>N5,R=>R5,Sel=>Sel5,S=>S5);

Mux1: entity work.Mux4to1
    port
map(J0=>"0000",J1=>"0000",J2=>S1,J3=>S2,MSL4=>MSL4_1,J=>N6);

Mux2: entity work.Mux4to1
    port map(J0=>"0000",J1=>S1,J2=>S2,J3=>S3,MSL4=>MSL4_2,J=>R6);

Mux3: entity work.Mux8to1
    port
map(I0=>"0000",I1=>"0000",I2=>"0000",I3=>S1,I4=>S2,I5=>S3,I6=>S4,I7
=>S5,MSL8=>MSL8_1,I=>N7);

Mux4: entity work.mux8to1
    port
map(I0=>"0000",I1=>"0000",I2=>S1,I3=>S2,I4=>S3,I5=>S4,I6=>S5,I7=>"0
000",MSL8=>MSL8_2,I=>R7);

Mux5: entity work.Mux4to1
    port map(J0=>S1,J1=>S2,J2=>S3,J3=>S4,MSL4=>MSL4_3,J=>N8);
```

```
Mux6: entity work.Mux4to1
    port map(J0=>S2,J1=>S3,J2=>S4,J3=>S5,MSL4=>MSL4_4,J=>R8);

Mux7: entity work.Mux4to1
    port map(J0=>S2,J1=>S3,J2=>S4,J3=>S5,MSL4=>MSL4_5,J=>N9);

Mux8: entity work.Mux4to1
    port map(J0=>S3,J1=>S4,J2=>S5,J3=>"0000",MSL4=>MSL4_6,J=>R9);

Mux9: entity work.mux2to1
    port map(K0=>S4,K1=>S5,MSL2=>MSL2_3,K=>N10);

Mux10: entity work.mux2to1
    port map(K0=>S5,K1=>"0000",MSL2=>MSL2_4,K=>R10);


ALU6:entity work.ALU
    port map(N=>N6,R=>R6,Sel=>Sel6,S=>S6);

ALU7:entity work.ALU
    port map(N=>N7,R=>R7,Sel=>Sel7,S=>S7);

ALU8:entity work.ALU
    port map(N=>N8,R=>R8,Sel=>Sel8,S=>S8);

ALU9:entity work.ALU
    port map(N=>N9,R=>R9,Sel=>Sel9,S=>S9);

ALU10:entity work.ALU
    port map(N=>N10,R=>R10,Sel=>Sel10,S=>S10);


Mux11: entity work.Mux8to1
    port
map(I0=>"0000",I1=>"0000",I2=>"0000",I3=>"0000",I4=>S6,I5=>S7,I6=>S
8,I7=>S9,MSL8=>MSL8_3,I=>N11);
```

```
Mux12: entity work.mux8to1
    port
map(I0=>"0000",I1=>"0000",I2=>"0000",I3=>S6,I4=>S7,I5=>S8,I6=>S9,I7
=>S10,MSL8=>MSL8_4,I=>R11);

Mux13: entity work.Mux4to1
    port map(J0=>"0000",J1=>S6,J2=>S7,J3=>S8,MSL4=>MSL4_7,J=>N12);

Mux14: entity work.Mux4to1
    port map(J0=>S6,J1=>S7,J2=>S8,J3=>S9,MSL4=>MSL4_8,J=>R12);

Mux15: entity work.Mux4to1
    port map(J0=>S6,J1=>S7,J2=>S8,J3=>S9,MSL4=>MSL4_9,J=>N13);

Mux16: entity work.Mux4to1
    port map(J0=>S7,J1=>S8,J2=>S9,J3=>S10,MSL4=>MSL4_10,J=>R13);

Mux17: entity work.mux2to1
    port map(K0=>S8,K1=>S9,MSL2=>MSL2_5,K=>N14);

Mux18: entity work.mux2to1
    port map(K0=>S9,K1=>S10,MSL2=>MSL2_6,K=>R14);

Mux19: entity work.mux2to1
    port map(K0=>S9,K1=>S10,MSL2=>MSL2_7,K=>N15);

Mux20: entity work.mux2to1
    port map(K0=>S10,K1=>"0000",MSL2=>MSL2_8,K=>R15);


ALU11:entity work.ALU
    port map(N=>N11,R=>R11,Sel=>Sel11,S=>S11);

ALU12:entity work.ALU
    port map(N=>N12,R=>R12,Sel=>Sel12,S=>S12);
```

```
ALU13:entity work.ALU
    port map(N=>N13,R=>R13,Sel=>Sel13,S=>S13);

ALU14:entity work.ALU
    port map(N=>N14,R=>R14,Sel=>Sel14,S=>S14);

ALU15:entity work.ALU
    port map(N=>N15,R=>R15,Sel=>Sel15,S=>S15);


Mux21: entity work.Mux4to1
    port
map(J0=>"0000",J1=>"0000",J2=>S11,J3=>S12,MSL4=>MSL4_11,J=>N16);

Mux22: entity work.Mux4to1
    port
map(J0=>"0000",J1=>S11,J2=>S12,J3=>S13,MSL4=>MSL4_12,J=>R16);


Mux23: entity work.mux2to1
    port map(K0=>S11,K1=>S12,MSL2=>MSL2_9,K=>N17);

Mux24: entity work.mux2to1
    port map(K0=>S12,K1=>S13,MSL2=>MSL2_10,K=>R17);

Mux25: entity work.mux2to1
    port map(K0=>S12,K1=>S13,MSL2=>MSL2_11,K=>N18);

Mux26: entity work.mux2to1
    port map(K0=>S13,K1=>S14,MSL2=>MSL2_12,K=>R18);

Mux27: entity work.mux2to1
    port map(K0=>S13,K1=>S14,MSL2=>MSL2_13,K=>N19);

Mux28: entity work.mux2to1
    port map(K0=>S14,K1=>S15,MSL2=>MSL2_14,K=>R19);
```

```
Mux29: entity work.mux2to1
    port map(K0=>S14,K1=>S15,MSL2=>MSL2_15,K=>N20);

Mux30: entity work.mux2to1
    port map(K0=>S15,K1=>"0000",MSL2=>MSL2_16,K=>R20);


ALU16:entity work.ALU
    port map(N=>N16,R=>R16,Sel=>Sel16,S=>S16);

ALU17:entity work.ALU
    port map(N=>N17,R=>R17,Sel=>Sel17,S=>S17);

ALU18:entity work.ALU
    port map(N=>N18,R=>R18,Sel=>Sel18,S=>S18);

ALU19:entity work.ALU
    port map(N=>N19,R=>R19,Sel=>Sel19,S=>S19);

ALU20:entity work.ALU
    port map(N=>N20,R=>R20,Sel=>Sel20,S=>S20);


Mux31: entity work.mux2to1
    port map(K0=>"0000",K1=>S16,MSL2=>MSL2_17,K=>N21);

Mux32: entity work.mux2to1
    port map(K0=>S16,K1=>S17,MSL2=>MSL2_18,K=>R21);

Mux33: entity work.mux2to1
    port map(K0=>S16,K1=>S17,MSL2=>MSL2_19,K=>N22);

Mux34: entity work.mux2to1
    port map(K0=>S17,K1=>S18,MSL2=>MSL2_20,K=>R22);

Mux35: entity work.mux2to1
    port map(K0=>S17,K1=>S18,MSL2=>MSL2_21,K=>N23);
```

```
Mux36: entity work.mux2to1
    port map(K0=>S18,K1=>S19,MSL2=>MSL2_22,K=>R23);

Mux37: entity work.mux2to1
    port map(K0=>S18,K1=>S19,MSL2=>MSL2_23,K=>N24);

Mux38: entity work.mux2to1
    port map(K0=>S19,K1=>S20,MSL2=>MSL2_24,K=>R24);

Mux39: entity work.mux2to1
    port map(K0=>S19,K1=>S20,MSL2=>MSL2_25,K=>N25);

Mux40: entity work.mux2to1
    port map(K0=>S20,K1=>"0000",MSL2=>MSL2_26,K=>R25);


ALU21:entity work.ALU
    port map(N=>N21,R=>R21,Sel=>Sel21,S=>S21);

ALU22:entity work.ALU
    port map(N=>N22,R=>R22,Sel=>Sel22,S=>S22);

ALU23:entity work.ALU
    port map(N=>N23,R=>R23,Sel=>Sel23,S=>S23);

ALU24:entity work.ALU
    port map(N=>N24,R=>R24,Sel=>Sel24,S=>S24);

ALU25:entity work.ALU
    port map(N=>N25,R=>R25,Sel=>Sel25,S=>S25);

end behavioral;
```