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-- Company:
-- Engineer:
-- Create Date: 22.04.2023 20:22:27
-- Design Name:
-- Module Name: FINAL TB - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
-- Dependencies:
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
entity FINAL TB is
end FINAL TB;
architecture Behavioral of FINAL TB is
signal N1, N2, N3, N4, N5, R1, R2, R3, R4, R5: std logic vector (3 downto 0);
signal Sel1, Sel2, Sel3, Sel4, Sel5, Sel6, Sel7, Sel8, Sel9, Sel10,
Sel11, Sel12, Sel13, Sel14, Sel15, Sel16, Sel17, Sel18, Sel19,
Sel20, Sel21, Sel22, Sel23, Sel24, Sel25: std logic vector(4 DOWNTO
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MSL2 3, MSL2 4, MSL2 5, MSL2 6, MSL2 7, MSL2 8, MSL2 9, MSL2 10, MSL2 11, MS
L2_12,MSL2_13,MSL2_14,MSL2_15,MSL2_16,MSL2_17,MSL2_18,MSL2_19,MSL2_
20, MSL2 21, MSL2 22, MSL2 23, MSL2 24, MSL2 25, MSL2 26: std logic;
signal
MSL4 1, MSL4 2, MSL4 3, MSL4 4, MSL4 5, MSL4 6, MSL4 7, MSL4 8, MSL4 9, MSL4
_10,MSL4_11,MSL4_12: std_logic_vector(1 DOWNTO 0);
signal MSL8 1, MSL8 2, MSL8 3, MSL8 4: std logic vector(2 DOWNTO 0);
signal S21,S22,S23,S24,S25: std_logic_vector(3 downto 0);
begin
uut: entity work.FINAL
port map(
N1=>N1, N2=>N2, N3=>N3, N4=>N4, N5=>N5,
R1 = > R1, R2 = > R2, R3 = > R3, R4 = > R4, R5 = > R5,
Sel1=>Sel1, Sel2=>Sel2, Sel3=>Sel3, Sel4=>Sel4, Sel5=>Sel5,
Sel6=>Sel6, Sel7=>Sel7, Sel8=>Sel8, Sel9=>Sel9, Sel10=>Sel10,
Sel11=>Sel11, Sel12=>Sel12, Sel13=>Sel13, Sel14=>Sel14,
Sel15=>Sel15,
Sel16=>Sel16, Sel17=>Sel17, Sel18=>Sel18, Sel19=>Sel19,
Sel20=>Sel20,
Sel21=>Sel21, Sel22=>Sel22, Sel23=>Sel23, Sel24=>Sel24,
Se125=>Se125,
MSL2 3=>MSL2 3,MSL2 4=>MSL2 4,MSL2 5=>MSL2 5,MSL2 6=>MSL2 6,MSL2 7=
>MSL2 7, MSL2 8=>MSL2 8, MSL2 9=>MSL2 9, MSL2 10=>MSL2 10,
MSL2 11=>MSL2 11, MSL2 12=>MSL2 12, MSL2 13=>MSL2 13, MSL2 14=>MSL2 14
,MSL2 15=>MSL2_15,MSL2_16=>MSL2_16,MSL2_17=>MSL2_17,MSL2_18=>MSL2_1
8,MSL2 19=>MSL2 19,
MSL2_20=>MSL2_20,MSL2_21=>MSL2_21,MSL2_22=>MSL2_22,MSL2_23=>MSL2_23
,MSL2 24=>MSL2 24,MSL2 25=>MSL2 25,MSL2 26=>MSL2 26,
MSL4 1=>MSL4 1,MSL4 2=>MSL4 2,MSL4 3=>MSL4 3,MSL4 4=>MSL4 4,MSL4 5=
>MSL4 5, MSL4 6=>MSL4 6,
MSL4 7=>MSL4 7,MSL4 8=>MSL4 8,MSL4 9=>MSL4 9,MSL4 10=>MSL4 10,MSL4
11=>MSL4 11, MSL4 12=>MSL4 12,
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0);

signal

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MSL8 1=>MSL8 1,MSL8 2=>MSL8 2,MSL8 3=>MSL8 3,MSL8 4=>MSL8 4,
S21=>S21, S22=>S22, S23=>S23, S24=>S24, S25=>S25);
process
begin
--TB FOR DFG-1
--INPUT'S
N1<="1001";N2<="0100";N3<="0010";N4<="1111";N5<="0001";
R1<="0110";R2<="0011";R3<="0111";R4<="1101";R5<="0001";
--ALU SEL'S
Sel1<="00000"; Sel2<="00010"; Sel3<="00000"; Sel4<="00001";
Sel5<="00010";
Sel6<="00001"; Sel7<="00000"; Sel8<="00001"; Sel9<="10010";
Sel10<="10011";
Sel11<="00110"; Sel12<="01001"; Sel13<="01000"; Sel14<="10011"
; Sel15<="10011" ;
Sel16<="01010"; Sel17<="00111"; Sel18<="10011"; Sel19<="10011";
Sel20<="10011";
Sel21<="10001"; Sel22<="10010"; Sel23<="10011"; Sel24<="10011";
Sel25<="10011";
--MUX SEL'S
MSL4\ 1 \le "10"; MSL4\ 2 \le "11"; MSL8\ 1 \le "101"; MSL8\ 2 \le "110"; MSL4\ 3 \le "01";
MSL4 4<="10"; MSL4 5<="00"; MSL4 6<="10"; MSL2 3<='1'; MSL2 4<='0';
MSL8 3 \le "100"; MSL8 4 \le "101"; MSL4 7 \le "10"; MSL4 8 \le "10"; MSL4 9 \le "00";
MSL4_10<="10";MSL2_5<='0';MSL2_6<='0';MSL2_7<='0';MSL2_8<='0';
MSL4 11<="10"; MSL4 12<="10"; MSL2 9<='1'; MSL2 10<='1'; MSL2 11<='0'; M
SL2 12<='1'; MSL2 13<='0'; MSL2 14<='0'; MSL2 15<='0'; MSL2 16<='0';
MSL2 17<='1'; MSL2 18<='1'; MSL2 19<='0'; MSL2 20<='0'; MSL2 21<='0'; MS
L2 22<='1'; MSL2 23<='0'; MSL2 24<='0'; MSL2 25<='0'; MSL2 26<='0';
WAIT FOR 20 NS;
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--TB FOR DFG-2

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N1<="1101";N2<="0010";N3<="0001";N4<="0010";N5<="0001";
R1<="0110";R2<="0011";R3<="0001";R4<="0010";R5<="0001";
--ALU SEL'S
Sel1<="00001"; Sel2<="00010"; Sel3<="10011"; Sel4<="00000";
Sel5<="00010";
Sel6<="10001" ; Sel7<="00000" ; Sel8<="00001" ; Sel9<="00000" ;
Sel10<="10001";
Sel11<="01100"; Sel12<="10010"; Sel13<="10000"; Sel14<="10011"
; Sel15<="10011" ;
Sel16<="00100"; Sel17<="00011"; Sel18<="10011"; Sel19<="10011";
Sel20<="10011";
Sel21<="10001"; Sel22<="10010"; Sel23<="10011"; Sel24<="10011";
Sel25<="10011";
--MUX SEL'S
MSL4_1<="10";MSL4_2<="10";MSL8_1<="011";MSL8_2<="101";MSL4_3<="00";
MSL4 4<="11";MSL4 5<="00";MSL4 6<="10";MSL2 3<='0';MSL2 4<='0';
MSL8 3 \le "100"; MSL8 4 \le "110"; MSL4 7 \le "10"; MSL4 8 \le "10"; MSL4 9 \le "01";
MSL4\ 10 <= "11"; MSL2\ 5 <= '0'; MSL2\ 6 <= '0'; MSL2\ 7 <= '0'; MSL2\ 8 <= '0';
MSL4 11<="10"; MSL4 12<="11"; MSL2 9<='0'; MSL2 10<='0'; MSL2 11<='0'; M
SL2 12<='1'; MSL2 13<='0'; MSL2 14<='0'; MSL2 15<='0'; MSL2 16<='0';
MSL2 17<='1'; MSL2 18<='0'; MSL2 19<='0'; MSL2 20<='0'; MSL2 21<='0'; MS
L2 22<='1'; MSL2 23<='0'; MSL2 24<='0'; MSL2 25<='0'; MSL2 26<='0';
WAIT FOR 20 NS;
--TB FOR DFG-3
--INPUT'S
N1<="1000"; N2<="1110"; N3<="0001"; N4<="0011"; N5<="0001";
R1<="0101";R2<="1000";R3<="0100";R4<="0010";R5<="0001";
--ALU SEL'S
Sel1<="00000" ; Sel2<="00001" ; Sel3<="00010" ; Sel4<="00010" ;
Sel5<="10011";
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--INPUT'S

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Sel6<="00001"; Sel7<="10010"; Sel8<="00000"; Sel9<="00001";
Sel10<="10011";
Sel11<="00111"; Sel12<="01000"; Sel13<="10011"; Sel14<="10011"
; Sel15<="10011" ;
Sel16<="10001"; Sel17<="10010"; Sel18<="10011"; Sel19<="10011";
Sel20<="10011"
Sel21<="10001"; Sel22<="10010"; Sel23<="10011"; Sel24<="10011";
Se125<="10011";
--MUX SEL'S
MSL4_1 \le "10"; MSL4_2 \le "10"; MSL8_1 \le "011"; MSL8_2 \le "100"; MSL4_3 \le "01";
MSL4 4 <= "10"; MSL4 5 <= "00"; MSL4 6 <= "01"; MSL2 3 <= '1'; MSL2 4 <= '0';
MSL8 \ 3 \le "100"; MSL8 \ 4 \le "100"; MSL4 \ 7 \le "11"; MSL4 \ 8 \le "11"; MSL4 \ 9 \le "10";
MSL4\ 10 <= "10"; MSL2\ 5 <= '0'; MSL2\ 6 <= '0'; MSL2\ 7 <= '0'; MSL2\ 8 <= '0';
MSL4 11<="10"; MSL4 12<="10"; MSL2 9<='0'; MSL2 10<='0'; MSL2 11<='0'; M
SL2 12<='1'; MSL2 13<='0'; MSL2 14<='0'; MSL2 15<='0'; MSL2 16<='0';
MSL2 17<='1'; MSL2 18<='1'; MSL2 19<='0'; MSL2 20<='0'; MSL2 21<='0'; MS
L2 22<='1'; MSL2 23<='0'; MSL2 24<='0'; MSL2 25<='0'; MSL2 26<='0';
WAIT FOR 20 NS;
--TB FOR DFG-4
--INPUT'S
N1<="0100";N2<="0011";N3<="1111";N4<="0010";N5<="0001";
R1<="0010";R2<="0100";R3<="1010";R4<="0010";R5<="0001";
--ALU SEL'S
Sel1<="00010"; Sel2<="00000"; Sel3<="00001"; Sel4<="00010";
Sel5<="10011";
Sel6<="00000"; Sel7<="00000"; Sel8<="00001"; Sel9<="10011";
Sel10<="10011";
Sel11<="10000"; Sel12<="01101"; Sel13<="01110"; Sel14<="10011"
; Sel15<="10011" ;
Sel16<="01010"; Sel17<="01011"; Sel18<="10011"; Sel19<="10011";
Sel20<="10011";
Sel21<="00101"; Sel22<="10011"; Sel23<="10011"; Sel24<="10011";
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MSL4_1<="10"; MSL4_2<="11"; MSL8_1<="100"; MSL8_2<="101"; MSL4_3<="10"; MSL4_4<="10"; MSL4_5<="00"; MSL4_6<="01"; MSL2_3<='1'; MSL2_4<='0'; MSL8_3<="100"; MSL8_4<="100"; MSL4_7<="01"; MSL4_8<="10"; MSL4_9<="01"; MSL4_9<="01"; MSL4_10<="01"; MSL2_5<='0'; MSL2_6<='0'; MSL2_7<='0'; MSL2_8<='0'; MSL4_11<="10"; MSL4_12<="10"; MSL2_9<='1'; MSL2_10<='1'; MSL2_11<='0'; MSL2_12<='1'; MSL2_13<='0'; MSL2_14<='0'; MSL2_15<='0'; MSL2_16<='0'; MSL2_17<='1'; MSL2_18<='1'; MSL2_19<='0'; MSL2_20<='0'; MSL2_21<='0'; MSL2_22<='1'; MSL2_23<='0'; MSL2_24<='0'; MSL2_25<='0'; MSL2_26<='0';
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Sel25<="10011";

--MUX SEL'S

WAIT;

end process;

end Behavioral;