```
----------------------------------------------------------------------
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-- Company:
-- Engineer:
--
-- Create Date: 17.04.2023 22:54:46
-- Design Name:
-- Module Name: Mux2to1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.NUMERIC_STD.ALL;
use ieee.std_logic_unsigned.all;



ENTITY Mux2to1 IS
    PORT (
          K0,K1:IN STD_LOGIC_VECTOR(3 DOWNTO 0);     --mux inputs
          K: OUT STD_LOGIC_VECTOR(3 DOWNTO 0);       --mux output
          MSL2:IN STD_LOGIC                          --mux selector
             );
END ENTITY;
```

```
ARCHITECTURE BEHAVIORAL OF Mux2to1 IS
BEGIN
    PROCESS(K0,K1,MSL2)
    BEGIN
        CASE (MSL2) IS
            WHEN '0' =>  K<= K0;
            WHEN '1' =>  K<= K1;

           WHEN OTHERS =>
           K <= "0000";
        END CASE;
    END PROCESS;
END BEHAVIORAL;
```