```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 17.04.2023 22:37:19
-- Design Name:
-- Module Name: MUX8to1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.NUMERIC_STD.ALL;
use ieee.std_logic_unsigned.all;



ENTITY Mux8to1 IS
    PORT (
          I0,I1,I2,I3,I4,I5,I6,I7:IN STD_LOGIC_VECTOR(3 DOWNTO 0);
    --mux inputs
          I: OUT STD_LOGIC_VECTOR(3 DOWNTO 0);
    --mux output
          MSL8:IN STD_LOGIC_VECTOR(2 DOWNTO 0));
    --mux selector
END ENTITY;
```

```
ARCHITECTURE BEHAVIORAL OF Mux8to1 IS
BEGIN
    PROCESS(I0,I1,I2,I3,I4,I5,I6,I7,MSL8)
    BEGIN
        CASE (MSL8) IS
            WHEN "000" =>  I<= I0;
            WHEN "001" =>  I<= I1;
            WHEN "010" =>  I<= I2;
            WHEN "011" =>  I<= I3;
            WHEN "100" =>  I<= I4;
            WHEN "101" =>  I<= I5;
            WHEN "110" =>  I<= I6;
            WHEN "111" =>  I<= I7;
            WHEN OTHERS =>
            I<= "0000";
        END CASE;
    END PROCESS;
END BEHAVIORAL;
```