Digital Design (A)

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Altera starix II architecture

- It is a device contains a 2D row and column based architecture those rows and columns are used to connect labs according to my HDL code.
- It also contains a memory block structures and digital signal processing blocks.
- Each LAB (logic array block) contains 8 ALMs (adaptive logic modules) which provides effecient implementation of user logic functions.
- Each Stratix II device I/O pin is fed by an I/O element (IOE) located at
- The end of LAB rows and columns around the periphery of the device.

Figure 2–1. Stratix II Block Diagram