PES University, Bangalore



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**B.Tech., 4thSemester, March 2022**

**UE20CS252: Microprocessor and Computer Architecture**

**Assignment -2**

**Last Date of Submission : 1st April 2022.**

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| **Sl #** | **Question** |
| **1** | How many total bits are required for a direct –mapped cache with 16KB of data and 4 word blocks, assuming a 32-bit address? |
| **2** | Consider a cache with 64 blocks and a block size of 16bytes. To what block number does the byte address 1200map?  Assume all are decimal numbers. |
| **3** | Increasing associativity requires more comparators and more tag bits per cache block. Assuming ac cache of 4K blocks, 4 word block size, and a 32-bit address, find the total number of sets and the total number of tag bits for caches that are direct mapped, two-way and four-way set associative , and fully associative. |
| **4** | Recall that w have two write policies and write allocate policies, their combinations can be implemented in either in L1 or L2 cache.   |  |  |  | | --- | --- | --- | |  | **L1 cache:** | **L2 cache:** | | a | Write back, write allocate | Write –through, non write allocate | | b | Write back, write no allocate. | Write –through, write allocate |   i. Describe the procedure of handling an L1 write miss, considering the component  involved and the possibility of replacing a dirty block.  ii. For a multilevel exclusive cache( a block can only reside in one of the L1 and L2 caches) configuration, describe the procedure of handling an L1 write miss, considering the component involved and the possibility of replacing a dirty block. |
| **5.** | Describe the following each with an example.  a. Device polling  b. Interrupt-driven communication and interrupt handling mechanisms.  c. Memory mapped I/O and I/O mapped I/O techniques. |