**Features**

* Two 10-bit Successive approximation ADC
* Input multiplexing among 8 pins
* 0 to VREF(3V)
* conversion time >= 2.44us
* Burst Conversion for single and multiple inputs
* clock by APB clock
* max 4.5MHz – 11 cycles

**Register Description**

**A/D Control Register (AD0CR - 0xE003 4000 and AD1CR - 0xE006 0000)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Bits** | **Symbol** | **Description** | | | |
| **7:0** | **SEL** | * Selects which of AD0 [7:0] or AD1 [7:0] pins to be sampled and converted. * for AD0 – bit0, for AD7 – bit7 * software mode – only one channel * hardware mode – more than one channel | | | |
| **15:8** | **CKLDIV** | * **PCLK** divided by (CLKDIV+1) and should be less than 4.5MHz | | | |
| **16** | **BURST** | **1 –** Continuous conversion using CLKS rate and SEL selected channels – SART bits must be 000  **0 –** Single Conversion and require 11 clocks | | | |
| **19:17** | **CLKS** | **Used in BURST mode = 1** | | | |
| **000** | | 11 clocks/ 10bits | |
| **001** | | 10 clocks/ 9its | |
| **010** | | 9 clocks/ 8bits | |
| **011** | | 8 clocks/ 7bits | |
| **100** | | 7 clocks/ 6bits | |
| **101** | | 6 clocks/ 5bits | |
| **110** | | 5 clocks/ 4bits | |
| **111** | | 4 clocks/ 3bits | |
| **21** | **PDN** | **1 –** ADC is operational – switch on ADC | | | |
| **26:24** | **START** | **Used in BURST mode = 0** | | | |
| **000** | Don’t’ start | | |
| **001** | Start conversion now | | |
| **010** | Start conversion when the edge selected by bit 27 occurs on MAT0.2 | | External Match register of TIMER0 |
| **011** | Start conversion when the edge selected by bit 27 occurs on MAT0.0 | |
| **101** | Start conversion when the edge selected by bit 27 occurs on MAT0.1 | |
| **101** | Start conversion when the edge selected by bit 27 occurs on MAT0.3 | |
| **110** | Start conversion when the edge selected by bit 27 occurs on MAT1.0 | | External Match register of TIMER1 |
| **111** | Start conversion when the edge selected by bit 27 occurs on MAT1.1 | |
| **27** | **EDGE** | Which edge should the ADC start conversion   1. falling edge, 0 – rising edge | | | |

**A/D Global Data Register (AD0GDR - 0xE003 4004 and AD1GDR -**

**0xE006 0004)**

|  |  |  |
| --- | --- | --- |
| **Bits** | **Symbol** | **Description** |
| **15:6** | **RESULT** | Available when DONE == 1 – voltage on AD channels |
| **26:24** | **CHN** | Which channel, RESULT is available is give here |
| **30** | **OVERRUN** | 1 – some lost or overwritten values |
| **31** | **DONE** | 1 – when ADC completes conversion  Cleared by reading this register and writing ADCR |

**A/D Global Start Register (ADGSR - 0xE003 4008)**

* on both the ADC’s

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bits** | **Symbol** | **Description** | | |
| **16** | **BURST** | **1 –** Continuous conversion using CLKS rate and SEL selected channels – SART bits must be 000  **0 –** Single Conversion and require 11 clocks | | |
| **26:24** | **START** | **Used in BURST mode = 0** | | |
|  |  | **000** | Don’t’ start | |
| **001** | Start conversion now | |
| **010** | Start conversion when the edge selected by bit 27 occurs on MAT0.2 | External Match register of TIMER0 |
| **011** | Start conversion when the edge selected by bit 27 occurs on MAT0.0 |
| **101** | Start conversion when the edge selected by bit 27 occurs on MAT0.1 |
| **101** | Start conversion when the edge selected by bit 27 occurs on MAT0.3 |
| **110** | Start conversion when the edge selected by bit 27 occurs on MAT1.0 | External Match register of TIMER1 |
| **111** | Start conversion when the edge selected by bit 27 occurs on MAT1.1 |
| **27** | **EDGE** | Which edge should the ADC start conversion   1. - falling edge, 0 – rising edge | | |

**A/D Status Register (ADSTAT, ADC0: AD0STAT - 0xE003 4030 and**

**ADC1: AD1STAT - 0xE006 0030)**

|  |  |  |
| --- | --- | --- |
| **Bits** | **Symbol** | **Description** |
| **0** | **DONE0** | DONE status flag for AD channel 0 |
| **1** | **DONE1** | DONE status flag for AD channel 1 |
| **2** | **DONE2** | DONE status flag for AD channel 2 |
| **3** | **DONE3** | DONE status flag for AD channel 3 |
| **4** | **DONE4** | DONE status flag for AD channel 4 |
| **5** | **DONE5** | DONE status flag for AD channel 5 |
| **6** | **DONE6** | DONE status flag for AD channel 6 |
| **7** | **DONE7** | DONE status flag for AD channel 7 |
| **8** | **OVERRUN0** | OVERFUN status flag for AD channel 0 |
| **9** | **OVERRUN1** | OVERFUN status flag for AD channel 1 |
| **10** | **OVERRUN2** | OVERFUN status flag for AD channel 2 |
| **11** | **OVERRUN3** | OVERFUN status flag for AD channel 3 |
| **12** | **OVERRUN4** | OVERFUN status flag for AD channel 4 |
| **13** | **OVERRUN5** | OVERFUN status flag for AD channel 5 |
| **14** | **OVERRUN6** | OVERFUN status flag for AD channel 6 |
| **15** | **OVERRUN7** | OVERFUN status flag for AD channel 7 |
| **16** | **ADINT** | 1 – when any of the DONE flag is asserted and enabled via ADINTEN register |

**A/D Interrupt Enable Register (ADINTEN, ADC0: AD0INTEN -**

**0xE003 400C and ADC1: AD1INTEN - 0xE006 000C)**

|  |  |  |
| --- | --- | --- |
| **Bits** | **Symbol** | **Description** |
| **0** | **ADINTEN0** | **1 –** ADC channel 0 conversion generate an interrupt |
| **1** | **ADINTEN1** | **1 –** ADC channel 1 conversion generate an interrupt |
| **2** | **ADINTEN2** | **1 –** ADC channel 2 conversion generate an interrupt |
| **3** | **ADINTEN3** | **1 –** ADC channel 3 conversion generate an interrupt |
| **4** | **ADINTEN4** | **1 –** ADC channel 4 conversion generate an interrupt |
| **5** | **ADINTEN5** | **1 –** ADC channel 5 conversion generate an interrupt |
| **6** | **ADINTEN6** | **1 –** ADC channel 6 conversion generate an interrupt |
| **7** | **ADINTEN7** | **1 –** ADC channel 7 conversion generate an interrupt |
| **8** | **ADGINTEN** | **0 -**  Individual ADC channel enabled by ADINTEN[7:0] will generate interrupts  1 – Global DONE flag in ADDR is enabled to generate interrupt |

**A/D Data Registers (ADDR0 to ADDR7, ADC0: AD0DR0 to AD0DR7 -**

**0xE003 4010 to 0xE003 402C and ADC1: AD1DR0 to AD1DR7-0xE006 0010 to 0xE006 402C)**

* Holds the result when ADC conversion is complete and also indicates when conversion completes and overrun occurs.

|  |  |  |
| --- | --- | --- |
| **Bits** | **Symbol** | **Description** |
| **15:6** | **RESULT** | Available when DONE == 1 – voltage on AD channels |
| **26:24** | **CHN** | Which channel, RESULT is available is give here |
| **30** | **OVERRUN** | 1 – some lost or overwritten values |
| **31** | **DONE** | 1 – when ADC completes conversion  Cleared by reading this register and writing ADCR |