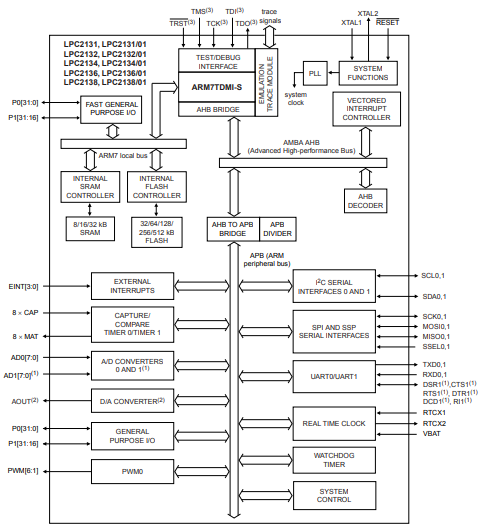
**LPC 2138**

**Features**

* 16/32 bit ARM7TDMI-S CPU
* with RISC principles
* maximum 60MHz operation using programmable on-chip PLL
* Embedded ICE and Embedded Trace – real time debugging and high speed tracing
* high speed Flash 512kB
* 128-bit memory interface
* 32-bit ARM Mode or 16-bit Thumb Mode
* on-Chip SRAM of 32kB
* Two 32-bit timers with four Capture and four compare, PWM channels
* single/dual 10-bit 8 channel ADC – 16 analog inputs
* 10-bit DAC
* 47 fast GPIO
* 9 edge/level triggered interrupt pins
* Real-time clock with independent power and dedicated 32kHz clock
* two UARTs, two Fast I2C, SPI and SSP
* Vectored Interrupt Controller with configurable priorities and vector addresses
* Can connect with external crystal form 1MHz to 25Mhz
* Power-on Reset and Brown-Out Detection

**Architecture**

* **ARMTDMI-S CPU**
* **ARM7 Local Bus** – interfacing with on-chip memory controller
* AMBA Advanced High-performance Bus(**AHB**) – interface with interrupt controller
* VLSI Peripheral Bus(**APB** – a superset of ARM’s AMBA Advanced Peripheral Bus) – for interface with on-chip peripheral Bus
* ABH to APB bridge interfaces the APB bus to AHB bus
* uses Little-Endian Byte Order
* can address 4GB(due to 32bit)
* AHB peripheral allocated 2MB top of 4GB RM memory space
  + Each **AHB** peripheral uses 16kB within 2MB
* **APB** peripheral allocated 2MB at the 3.5GB address point
  + Each **APB** peripheral uses 16kB within 2MB



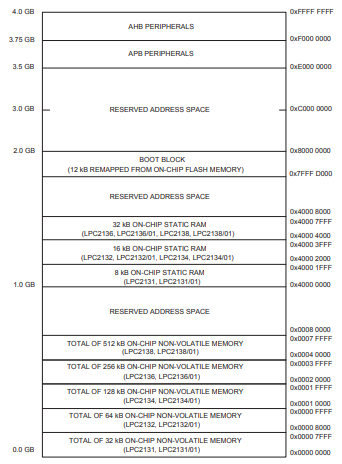
**Flash Memory**

* 512kB Flash for both code an data
* programming using
  + serial built-in JTAG
  + ISP
  + UART0
  + In Application Programming(IAP) – erase and program Flash while application is running

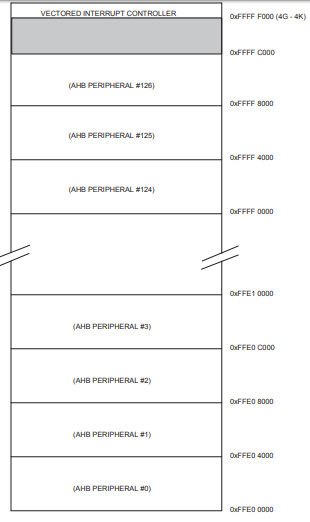
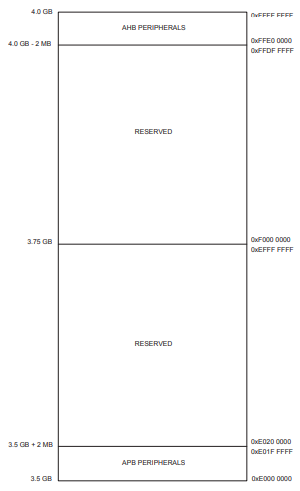
**SRAM**

* 32kB of SRAM
* can be accessed as 8-bit, 16-bit and 32-bit

**MEMORY MAPS**



* Interrupt vector area supports address remapping.
* Both AHB and APB peripherals areas are 2MB which are divided up to 128 peripherals with each peripheral has 16kB.
* Code resides in the natural location in memory map
* The interrupt vectors on ARM7 is at 0x0000\_0000 to 0x0000\_001C
* Interrupt Service vector can be remapped via Memory Mapping Control.
* Prefetch abort and data abort exceptions are generates appropriate bus cycle about exception if an access to
  + reserved or unassigned address region
  + unassigned AHP peripheral spaces
  + unassigned APB peripheral spaces



**Memory Accelerator Module (MAM)**

* performance is maximized when code is running in Flash Memory
* MAM attempts to have next instruction needed in its latches to prevent CPU fetch stalls.

**System Control Blocks**

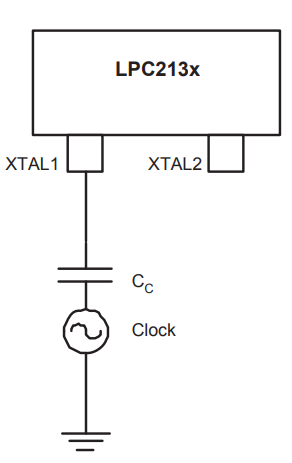
* Crystal Oscillator
* External Interrupt Inputs
* Miscellaneous System Controls and Status
* Memory Mapping Control
* PLL
* Power Control
* Reset
* APB Divider
* Wake-up Timer

**Crystal Oscillator**

|  |  |
| --- | --- |
| **Pin Name** | **Description** |
| XTAL1 | Crystal Oscillator Input – Input to oscillator and internal clock generator circuit |
| XTAL2 | Crystal Oscillator Output – Output from oscillator amplifier |

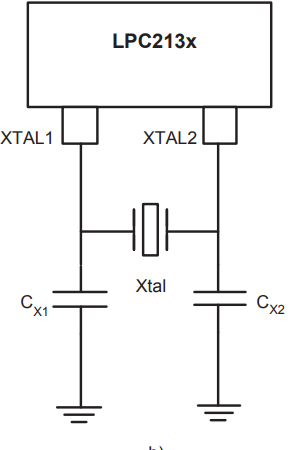
* the microcontroller’s onboard oscillator circuit support only external crystal of 1MHz to 30MHz.
* If on-chip PLL or boot-loader is used – then only 10MHz to 25MHz.
* oscillator output frequency is FOSC and ARM processor clock is FCCLK
* onboard oscillator operates in

1. Slave Mode
2. Oscillation Mode
3. **Slave Mode**



* input clock is coupled by 100pF capacitor(CC) with minimum amplitude of 200mVrms clock source
* output pin X2 is left unconnected
* FOSC­ can be 1MHz to 50Mhz
* no external crystal oscillator

1. **Oscillation Mode**



* limits F­­­OSC­­ to 1MHz to 30Mhz
* C­­X1 ­and Cx2 ­­­can be dependent of Frequency used -- see datasheet

**External interrupt**

|  |  |
| --- | --- |
| **Pin name** | **Description** |
| EINT0 | External Interrupt input 0 – pins ***P0.1*** and ***P0.16*** |
| EINT1 | External Interrupt input 1 – pins ***P0.2*** and ***P0.4*** |
| EINT2 | External Interrupt input 2 – pins ***P0.7*** and ***P0.15*** |
| EINT3 | External Interrupt input 3 – pins ***P0.20*** and ***P0.30*** |
| RESET’ | External Reset Input – low level – 0x0000\_0000 – default state |

* four interrupt sources
* can be used to wake-up processor from power-down mode

**Register Description**

**External Interrupt Flag register (EXTINT - 0xE01F C140)**

* an interrupt causes interrupt flag set in **EXTINT** register
* will cause a interrupt request to **VIC** if interrupt in enabled on this pin
* **EXINT** bits must be cleared to handle to handle further interrupt

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **7:4 - Reserved** | **3 – EINT3** | **2-EINT2** | **1-EINT1** | **0-EINT0** |

**External Interrupt Mode register (EXTMODE - 0xE01F C148)**

* used to select if EINT pins are level-edge triggered
* should be enabled by VICIntEnable register
* 0 – Level triggered and 1 – Edge triggered

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **7:4 - Reserved** | **3 – EXTMODE3** | **2- EXTMODE2** | **1- EXTMODE1** | **0- EXTMODE0** |

**External Interrupt Polarity register (EXTPOLAR - 0xE01F C14C)**

* In level-sensitive
  + 1 - active-high
  + 0 - active-low
* In edge-sensitive
  + 1 - Rising Edge
  + 0 - Falling Edge
* should be enabled by VICIntEnable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **7:4 - Reserved** | **3 – EXTPOLAR3** | **2- EXTPOLAR2** | **1- EXTPOLAR1** | **0- EXTPOLAR0** |

**Multiple External Interrupt pins**

* can select multiple pins for each EINT[3:0] using Pins select register
* In Active-low sensitive mode
  + states of all pins selected for the same EINTx functionally are combined using positive logic AND gate
* In Active-high sensitive mode
  + states of all pins selected for the same EINTx functionally are combined using positive logic OR gate
* In Edge sensitive mode
  + pin with lowest GPIO port number is used
  + should not be used

**Steps:**

**Other system controls**

**System Control and Status Flag register (SCS - 0xE01F C1A0)**

|  |  |  |
| --- | --- | --- |
| **31-2 – Reserved** | **1 – GPIO1M** | **0 – GPIO0M** |

* for mode selection
* 0 – GPIO port0/ port1 is accessed via APH address
* 1 - GPIO port0/ port1 is accessed via addresses in on chip memory range
  + High speed GPIO
  + enables port masking

**Reset**

* three sources for RESET
  + RESET’ pin
    - Schmitt trigger with glitch filter
    - minimum of 10ms assertion when power on and 300ns when oscillator is running
  + Watchdog Reset
  + Brown-Out-Detector Reset

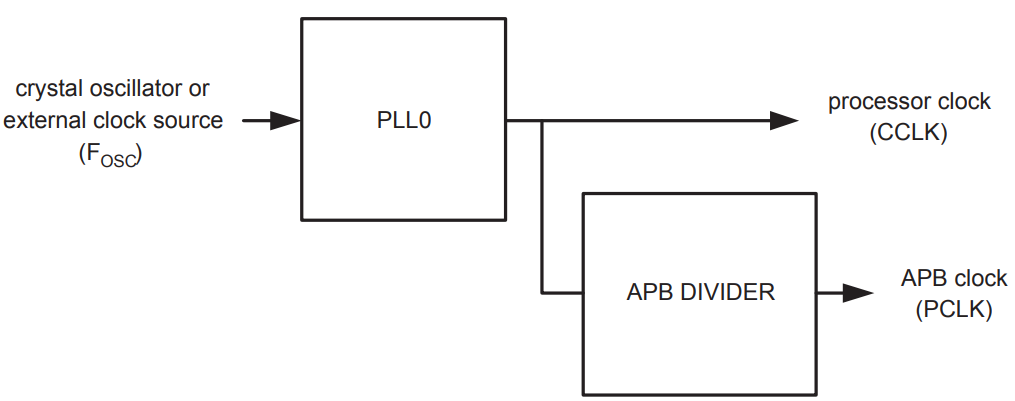
**Reset Source Identification Register (RSIR - 0xE01F C180)**

* contains one bit for each source of Reset

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **7-4 – Reserved** | **3 – BODR** | **2 – WDTR** | **1 – EXTR** | **0 - POR** |

* **POR –** indicates Power On Reset, assertedby POR signal
* **EXTR –** indicates assertion of RESET’, cleared by POR
* **WDTR –** WatchDog Timer times out
* **BODR –** when 3.3V power reaches below 2.6V

**APB Divider**



* gives the relationship between CCLK and PCLK
* provide clock to peripherals via APB bus
  + default is ¼th of CCLK
* allow power saving when peripherals are not required
* APB divider uses the PLL output

**Register Description**

**VPBDIV register (APBDIV - 0xE01F C100)**

|  |  |
| --- | --- |
| **7:2 – Reserved** | **1:0 - APBDIV** |

|  |  |
| --- | --- |
| **APBDIV** | **Description** |
| **00** | ¼ th of CCLK |
| **01** | Same as CCLK |
| **10** | ½ th of CCLK |
| **11** | Reserved |

**Pin Connect Block**

* Allows individual pin configuration for the desired function to each pin
* selected pins have more than one function

**Register Description**

**Pin Function Select Register 0 (PINSEL0 - 0xE002 C000)**

* for selecting pin functionality of P0.0 to P0.15

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **Symbol** | **Value** | **Function** |
| **1:0** | **P0.0** | **00** | GPIO Port 0.0 |
| **01** | TXD(UART0) |
| **10** | PWM1 |
| **11** | Reserved |
| **3:2** | **P0.1** | **00** | GPIO Port 0.1 |
| **01** | RXD(UART0) |
| **10** | PWM3 |
| **11** | EINT0 |
| **….** |  |  | **See datasheet** |
| **31:30** | **P0.15** | **00** | GPIO Port 0.15 |
| **01** | RI(UART1) |
| **10** | EINT2 |
| **11** | AD1.5 |

**Pin Function Select Register 1 (PINSEL1 - 0xE002 C004)**

* for selecting pin functionality of P0.16 to P0.31

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **Symbol** | **Value** | **Function** |
| **1:0** | **P0.16** | **00** | GPIO Port 0.16 |
| **01** | EINT0 |
| **10** | Match 0.2(Timer0) |
| **11** | Capture 0.2(Timer0) |
| **3:2** | **P0.17** | **00** | GPIO Port 0.17 |
| **01** | Capture 1.2(Timer 1) |
| **10** | SCK |
| **11** | Match 1.2(Timer1) |
| **….** |  |  | **See datasheet** |
| **31:30** | **P0.31** | **00** | GPO port only |
| **01** | Reserved |
| **10** | Reserved |
| **11** | Reserved |

**Pin Function Select Register 2 (PINSEL2 - 0xE002 C014)**

* for selecting pin functionality of P1.36 to P1.16

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **Symbol** | **Value** | **Function** |
| **1:0** | **-** | **-** | Reserved |
| **2** | **GPIO/DEBUG** | **0** | P1.36 to P1.26 is uses as GPIO pins |
| **1** | P1.36 to P1.26 is uses as Debug pins |
| **3** | **GPIO/TRACE** | **0** | P1.36 to P1.26 is uses as GPIO pins |
| **1** | P1.36 to P1.26 is uses as Debug pins |
| **31:4** | **-** | **-** | Reserved |

**GPIO**

* all I/O defaults to input after reset
* P0.0 – P0.31 and P1.16 – P1.31
  + 30 I/O and one output only on PORT0
  + 16 pins on PORT1
* Both Legacy and fast registers
  + but use either of it
* IOPIN, IOSET, IODIR, IOCLR
* FIODIR, FIOPIN, FIOSET, FIOCLR