**Feature**

* Seven match register – so 6 single edge controlled or 3 double edge controlled PWM output or mix
* both positive and negative going pulses
* Good resolution
* Can be used as standard timer
* one 32-bit Timer/Counter with a programmable 32-bit Prescalar

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PWM Channel** | **Single Edge PWM(PWMSELn = 0)** | | **Double Edge PWM(PWMSELn = 1)** | |
| **Set by** | **Reset by** | **Set by** | **Reset by** |
| **1** | Match 0 | Match 1 | Match 0 | Match 1 |
| **2** | Match 0 | Match 2 | Match 1 | Match 2 |
| **3** | Match 0 | Match 3 | Match 2 | Match 3 |
| **4** | Match 0 | Match 4 | Match 3 | Match 4 |
| **5** | Match 0 | Match 5 | Match 4 | Match 5 |
| **6** | Match 0 | Match 6 | Match 5 | Match 6 |

* Don’t’ use PWM 1, 3 5 for double edge PWM output

**Register Description**

**PWM Interrupt Register (PWMIR - 0xE001 4000)**

* contains interrupt flags for the 7 PWM channels
* writing 1 will reset the interrupt

|  |  |  |
| --- | --- | --- |
| **Bits** | **Symbol** | **Description** |
| **0** | **PWMMR0** | Interrupt Flag for PWM match channel 0 |
| **1** | **PWMMR1** | Interrupt Flag for PWM match channel 1 |
| **2** | **PWMMR2** | Interrupt Flag for PWM match channel 2 |
| **3** | **PWMMR3** | Interrupt Flag for PWM match channel 3 |
| **7:4** | **-** | Reserved |
| **8** | **PWMMR4** | Interrupt Flag for PWM match channel 4 |
| **9** | **PWMMR5** | Interrupt Flag for PWM match channel 5 |
| **10** | **PWMMR6** | Interrupt Flag for PWM match channel 6 |
| **15:11** | **-** | Reserved |

**PWM Timer Control Register (PWMTCR - 0xE001 4004)**

* control operation of PWM Timer Counter
* ***PWM Enable*** bit should be set

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **7:4 – Reserved** | **3 – PWM Enable** | **2 – Reserved** | **1 – Counter Reset** | **0 – Counter Enable** |

**PWM Timer Counter (PWMTC - 0xE001 4008)**

* 32-bit counter counts from 0x0000\_0000 to 0xFFFF\_FFFF and then wraps around to 0x0000\_0000

**PWM Prescale Register (PWMPR - 0xE001 400C)**

* the maximum value of the Prescale Counter value

**PWM Prescale Counter register (PWMPC - 0xE001 4010)**

* the actual prescale counter
* controls the PCLK division

**PWM Match Registers (PWMMR0 - PWMMR6)**

* the match register for PWM checking

**PWM Match Control Register (PWMMCR - 0xE001 4014)**

* the match control register to control when Counter reaches one of the PWM Match Register and what should happen on the channel output

|  |  |  |
| --- | --- | --- |
| **Bits** | **Symbol** | **Description** |
| **0** | **PWMMR0I** | 1 – Interrupt when PWMMR0 equals PWMTC |
| **1** | **PWMMR0R** | 1 – Reset PWMTC when PWMMR0 equals PWMTC |
| **2** | **PWMMR0S** | 1 – Stop PWMTC, PWMPC & PWMTCR [0] (Counter enable) is cleared when PWMMR0 equals PWMTC |
| **3** | **PWMMR1I** | 1 – Interrupt when PWMMR1 equals PWMTC |
| **4** | **PWMMR1R** | 1 – Reset PWMTC when PWMMR0 equals PWMTC |
| **5** | **PWMMR1S** | 1 – Stop PWMTC, PWMPC & PWMTCR [0] (Counter enable) is cleared when PWMMR1 equals PWMTC |
| **6** | **PWMMR2I** | 1 – Interrupt when PWMMR2 equals PWMTC |
| **7** | **PWMMR2R** | 1 – Reset PWMTC when PWMMR2 equals PWMTC |
| **8** | **PWMMR2S** | 1 – Stop PWMTC, PWMPC & PWMTCR [0] (Counter enable) is cleared when PWMMR2 equals PWMTC |
| **9** | **PWMMR3I** | 1 – Interrupt when PWMMR3 equals PWMTC |
| **10** | **PWMMR3R** | 1 – Reset PWMTC when PWMMR3 equals PWMTC |
| **11** | **PWMMR3S** | 1 – Stop PWMTC, PWMPC & PWMTCR [0] (Counter enable) is cleared when PWMMR3 equals PWMTC |
| **12** | **PWMMR4I** | 1 – Interrupt when PWMMR4 equals PWMTC |
| **13** | **PWMMR4R** | 1 – Reset PWMTC when PWMMR4 equals PWMTC |
| **14** | **PWMMR4S** | 1 – Stop PWMTC, PWMPC & PWMTCR [0] (Counter enable) is cleared when PWMMR4 equals PWMTC |
| **15** | **PWMMR5I** | 1 – Interrupt when PWMMR5 equals PWMTC |
| **16** | **PWMMR5R** | 1 – Reset PWMTC when PWMMR5 equals PWMTC |
| **17** | **PWMMR5S** | 1 – Stop PWMTC, PWMPC & PWMTCR [0] (Counter enable) is cleared when PWMMR5 equals PWMTC |
| **18** | **PWMMR6I** | 1 – Interrupt when PWMMR6 equals PWMTC |
| **19** | **PWMMR6R** | 1 – Reset PWMTC when PWMMR6 equals PWMTC |
| **20** | **PWMMR6S** | 1 – Stop PWMTC, PWMPC & PWMTCR [0] (Counter enable) is cleared when PWMMR6 equals PWMTC |
| **31:21** | **-** | Reserved |

**PWM Control Register (PWMPCR - 0xE001 404C)**

* enable and select type of each PWM channel

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **Symbol** | **Description** | |
| **1:0** | **-** | Reserved | |
| **2** | **PWMSEL2** | 1 – Double edge | 0 – Single edge |
| **3** | **PWMSEL3** | 1 – Double edge | 0 – Single edge |
| **4** | **PWMSEL4** | 1 – Double edge | 0 – Single edge |
| **5** | **PWMSEL5** | 1 – Double edge | 0 – Single edge |
| **6** | **PWMSEL6** | 1 – Double edge | 0 – Single edge |
| **8:7** | **-** | Reserved | |
| **9** | **PWMENA1** | 1 – PWM1 output is enabled | |
| **10** | **PWMENA2** | 1 – PWM2 output is enabled | |
| **11** | **PWMENA3** | 1 – PWM3 output is enabled | |
| **12** | **PWMENA4** | 1 – PWM4 output is enabled | |
| **13** | **PWMENA5** | 1 – PWM5 output is enabled | |
| **14** | **PWMENA6** | 1 – PWM6 output is enabled | |
| **15** | **-** | Reserved | |