**Phase Locked Loop (PLL)**

* can accept input frequency of 10MHz to 25MHz
* Using Current Controlled Oscillator(CCO), the range is multiplied to 10MHz to 60MHz into FCCLK.
* multiplier value can be from 1 to 32 but in practice its’ 6 due to upper frequency limit of CPUT
* CCO operates in 156MHz to 320MHz – but uses an additional divider(2 or 4 or 8 or 16) to get 50% duty cycle clock
* controlled by **PLLCON** register(activation) and **PLLCFG** register(configuration)
* Protection similar to Watchdog Timer is available to stop accidental changes – see **PLLFEED** register.
* enabled, configured and activated by the software and then wait for PPL to lock and then connect PLL to clock source

**Register Description**

**PLL Control register (PLLCON - 0xE01F C080)**

* updating PLL control bits
* bits to enabled and connect PLL
* enabling attempts to lock to current setting of multiplier and divider value
* changes takes place only after ***PLL feed***
* PLL must be set up, enabled and locked before using as clock source

|  |  |  |
| --- | --- | --- |
| **7:2 – Reserved** | **1 – PLLC** | **1 - PLLE** |

* PLLE – PLL Enable – After valid ***PLL feed*** allows active the PLL and lock it to requested frequency
* PLLC – PLL Connect – After valid ***PLL feed*** and PLLE is one, connects PLL to clock source of microcontroller.

**PLL Configuration register (PLLCFG - 0xE01F C084)**

* update PLL configuration values
* changes takes place only after ***PLL feed***
* PLL multiplier and divider values

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| --- | --- | --- |
| **7 – Reserved** | **6:5 – PSEL** | **4:0 – MSEL** |

* MSEL – PLL Multiplier value – represented by M
  + find M using formula and write M-1 to MSEL
* PSEL – PLL Divider value – represented by P
  + find P using formula and write P for values satisfying CCO frequency

|  |  |
| --- | --- |
| **PSEL** | **Value of P** |
| **00** | 1 |
| **01** | 2 |
| **10** | 4 |
| **11** | 8 |

|  |  |
| --- | --- |
| **MSEL** | **Value of M** |
| **00000** | **0** |
| **00001** |  |
| **…** |  |
| **11110** | **31** |
| **11111** | **32** |

|  |  |
| --- | --- |
| **Elements** | **Description** |
| **F0SC** | Frequency of external/crystal oscillator |
| **FCCO** | Frequency of PLL current controller oscillator |
| **CCLK** | PLL output Frequency and the Processor clock frequency |
| **M** | MSEL bit in PLLCFG register – multiplier |
| **P** | PSEL bit in PLLCFG register – divider |

**PLL output Frequency and the Processor clock frequency**

**CCLK = M x FOSC­ = FCCO­­ / (2 x P)**

**Frequency of PLL current controller oscillator**

**FCCO ­= CCLK x 2 x P = FOSC­­ x M x 2 x P**

**PLL Status register (PLLSTAT - 0xE01F C088)**

* current configuration of PLL

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **15:11 – Reserved** | **10 – PLOCK** | **9 - PLLC** | **8 - PLLE** | **7 – Reserved** | **6:5 – PSEL** | **4:0 - MSEL** |

* PLLE – when one, the PLL is currently activated and when zeros, PLL is off. during power-down mode, it is off
* PLLC – when PLLE and PLLC are both one, the PLL is connected as clock source to microcontroller
* PLOCK – reflects the PLL lock status

**Note: PLOCK** bits can cause interrupt which helps to determine if PLL has achieved the lock.

***PLL FEED***

* done using PLLFEED register (PLLFEED - 0xE01F C08C)
* Feed sequence
  + ***write value 0xAA to PLLFEED***
  + ***write value 0x55 to PLLFEED***
* interrupt must be disabled during feed operation

**Steps**

1. Enable the PLL by setting PLLE bit in PLLCON.
2. Set the Multiplier and Divider value by setting the MSEL and PSEL bits of PLLCFG.
3. Perform a PLL feed by.
   * ***write value 0xAA to PLLFEED***
   * ***write value 0x55 to PLLFEED***
4. Wait until the PLL gets locked by checking for 1 at PLOCK bit in PLLSTAT.
5. Connect the PLL by setting PLLC bit in PLLCON.
6. Perform a PLL feed by.
   * ***write value 0xAA to PLLFEED***
   * ***write value 0x55 to PLLFEED***