**Features**

* Two 32-bit Timer/Counter with programmable 32-bit Prescalar
* External-Even Counting
* Four 32-bit capture channels per timer
* Four 32-bit Match register
* use external clock

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| **Pins** | **Type** | **Description** |
| **CAP0[3:0] CAP1[3:0]** | **Input** | Transition on any of the capture pin can cause the Timer Counter value to be loaded into any of the Capture register and optionally generate interrupt. |
| **MAT0[3:0] MAT1[3:0]** | **Output** | When Match register 0/1 equals the timer counter value, the output of this pin may toggle, go low, go high and also generate optional interrupt. |

**Register Description**

**Interrupt Register (IR, TIMER0: T0IR - 0xE000 4000 and TIMER1: T1IR - 0xE000 8000)**

* contains the flag bits for match and capture channel
* writing 1 will reset the interrupt

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| **Bits** | **Symbol** | **Description** |
| **7:4** | CR[3:0] Interrupt | Interrupt Flag for capture channel [3:0] event |
| **3:0** | MR[3:0] Interrupt | Interrupt Flag for match channel [3:0] event |

**Timer Control Register (TCR, TIMER0: T0TCR - 0xE000 4004 and**

**TIMER1: T1TCR - 0xE000 8004)**

* To enabling counting and to reset values of timer counter and prescale counter

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| **7:2 – Reserved** | **1 – Counter Reset** | **0 – Counter Enable** |

**Count Control Register (CTCR, TIMER0: T0CTCR - 0xE000 4070 and**

**TIMER1: T1CTCR - 0xE000 8070)**

* used to select amount Timer Mode and different Counter mode
* select which edge
* select which pin

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| **Bits** | **Symbol** | **Value** | **Description** | |
| **1:0** | Counter /Timer Mode | 00 | Timer Mode | Increment of each rising PCLK edge |
| 01 | Counter Mode | Increment of rising edge on CAP input selected by bits **TIMERn[**3:2] |
| 10 | Increment of falling edge on CAP input selected by bits **TIMERn[**3:2] |
| 11 | Increment of both edge on CAP input selected by bits **TIMERn[**3:2] |
| **3:2** | Count Input Select | 00 | CAP0.0 for TIMER0 and CAP1.0 for TIMER1 | |
| 01 | CAP0.1 for TIMER0 and CAP1.1 for TIMER1 | |
| 10 | CAP0.2 for TIMER0 and CAP1.2 for TIMER1 | |
| 11 | CAP0.3 for TIMER0 and CAP1.3 for TIMER1 | |
| **7:4** | - | - | Reserved | |

**Timer Counter (TC, TIMER0: T0TC - 0xE000 4008 and TIMER1:**

**T1TC - 0xE000 8008)**

* 32-bit counter from 0x0000\_0000 to 0xFFFF\_FFFF and then wraps around to 0x0000\_0000 – no interrupt on overflow(can use match register)

**Prescale Register (PR, TIMER0: T0PR - 0xE000 400C and TIMER1:**

**T1PR - 0xE000 800C)**

* 32-bit Prescalar value for the maximum value of Prescale Counter
* upto which the Prescale Counter register should reach

**Prescale Counter Register (PC, TIMER0: T0PC - 0xE000 4010 and**

**TIMER1: T1PC - 0xE000 8010)**

* The actual Prescale Counter, that counts upto Prescale Register value
* Prescale Counter register increments on every PCLK value and when it reaches the Prescale Register value, it increments the Timer Counter.

**Match Registers (MR0 - MR3)**

* Match register values compared continuously with Timer Counter value.

**Match Control Register (MCR, TIMER0: T0MCR - 0xE000 4014 and**

**TIMER1: T1MCR - 0xE000 8014)**

* What operation to perform when there is match between Timer Counter value and any of the Match Register values.

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| **Bits** | **Symbol** | **Description** |
| **0** | **MR0I** | 1 – Generate Interrupt on match between TC and MR0 |
| **1** | **MR0R** | 1 – TC resets on match between TC and MR0 |
| **2** | **MR0S** | 1 – TC and PC stops and TCR[0](Counter enable) becomes 0 on match between TC and MR0 |
| **3** | **MR1I** | 1 – Generate Interrupt on match between TC and MR1 |
| **4** | **MR1R** | 1 – TC resets on match between TC and MR1 |
| **5** | **MR1S** | 1 – TC and PC stops and TCR[0](Counter enable) becomes 0 on match between TC and MR1 |
| **6** | **MR2I** | 1 – Generate Interrupt on match between TC and MR2 |
| **7** | **MR2R** | 1 – TC resets on match between TC and MR2 |
| **8** | **MR2S** | 1 – TC and PC stops and TCR[0](Counter enable) becomes 0 on match between TC and MR2 |
| **9** | **MR3I** | 1 – Generate Interrupt on match between TC and MR3 |
| **10** | **MR3R** | 1 – TC resets on match between TC and MR3 |
| **11** | **MR3S** | 1 – TC and PC stops and TCR[0](Counter enable) becomes 0 on match between TC and MR3 |
| **15:12** | **-** | Reserved |

**Capture Registers (CR0 - CR3)**

* the value of Timer Counter is stored in Capture Register when capture even occurs.

**Capture Control Register (CCR, TIMER0: T0CCR - 0xE000 4028 and**

**TIMER1: T1CCR - 0xE000 8028)**

* which capture register to store, which pin to capture, which edge to capture and interrupt should be generated or not?

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| **Bits** | **Symbol** | **Description** |
| **0** | **CAP0RE** | 1 – Capture on CAPn.0 rising edge on CAPn.0 pin will cause capture of TC to CR0 |
| **1** | **CAP0FE** | 1 – Capture on CAPn.0 falling edge on CAPn.0 pin will cause capture of TC to CR0 |
| **2** | **CAP0I** | 1 – Interrupt on Capn.0 event – loading of CR0 to TC |
| **3** | **CAP1RE** | 1 – Capture on CAPn.1 rising edge on CAPn.1 pin will cause capture of TC to CR1 |
| **4** | **CAP1FE** | 1 – Capture on CAPn.1 falling edge on CAPn.1 pin will cause capture of TC to CR1 |
| **5** | **CAP1I** | 1 – Interrupt on CAPn.1 event – loading of CR1 to TC |
| **6** | **CAP2RE** | 1 – Capture on CAPn.2 rising edge on CAPn.2 pin will cause capture of TC to CR2 |
| **7** | **CAP2FE** | 1 – Capture on CAPn.2 falling edge on CAPn.2 pin will cause capture of TC to CR2 |
| **8** | **CAP2I** | 1 – Interrupt on CAPn.2 event – loading of CR2 to TC |
| **9** | **CAP3RE** | 1 – Capture on CAPn.3 rising edge on CAPn.3 pin will cause capture of TC to CR3 |
| **10** | **CAP3FE** | 1 – Capture on CAPn.3 falling edge on CAPn.3 pin will cause capture of TC to CR3 |
| **11** | **CAP3I** | 1 – Interrupt on CAPn.3 event – loading of CR3 to TC |
| **15:12** | **-** | Reserved |

**External Match Register (EMR, TIMER0: T0EMR - 0xE000 403C; and**

**TIMER1: T1EMR - 0xE000 803C)**

* controls and status of external match pins MAT[0:3]
* what should happen to MAT[3:0] pins on match

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| **Bits** | **Symbol** | **Description** |
| **0** | **EM0** | External Match 0 - State of output pins MAT0.0/MAT1.0 |
| **1** | **EM1** | External Match 1 - State of output pins MAT0.1/MAT1.1 |
| **2** | **EM2** | External Match 2 - State of output pins MAT0.2/MAT1.2 |
| **3** | **EM3** | External Match 3 - State of output pins MAT0.3/MAT1.3 |
| **5:4** | **EMC0** | External Match Control 0 – determine the functionality of External Match 0 |
| **7:6** | **EMC1** | External Match Control 1 – determine the functionality of External Match 0 |
| **9:8** | **EMC2** | External Match Control 2 – determine the functionality of External Match 2 |
| **11:10** | **EMC3** | External Match Control 3 – determine the functionality of External Match 3 |
| **15:12** | **-** | Reserved |

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| **EMC[11:10],EMC[9:8], EMC[7:6], EMC[5:4]** | **Function** |
| **00** | **-** |
| **01** | Clear corresponding External Match bit/output |
| **10** | Set corresponding External Match bit/output |
| **11** | Toggle corresponding External Match bit/output |