**Description**

* 12-bit successive approximation ADC
* up to 18 multiplexed channels – 16 external + 2 internal source
* single conversion mode, continuous mode, discontinuous mode
* ADC input clock is APB2 clock and not more than 14 MHz
* Scan mode for conversion among channels
* 2.4V to 3.6V supply Voltage
* ADCx\_IN[15:0]
* powered on by ***ADON*** bit in ***ADC\_CR2*** register
* stopped by clearing the ***ADON*** bit
* dedicated programmable Prescaler for ADC clock
* Temperature sensor is @ ADCx\_IN16 and internal reference voltage is @ ADCx\_IN17

**Channel Selection**

* can select any of 16 multiplexed channels in any order
* two ways to group them
  + **Regular** Group
  + **Injected** Group

1. **Regular** Group

* composed up to 16 conversion
* order is selected by ***ADC\_SQRx*** registers
* number of conversion is selected by ***L[3:0]*** bits in ***ADC\_SQR1*** registers

1. **Injected** Group

* composed up to 4 conversions
* order is selected by ***ADC\_JSQRx*** registers
* number of conversion is selected by ***L[1:0]*** bits in ***ADC\_JSQR*** registers

**Modes:**

1. Single Conversion Mode
2. Continuous conversion Mode
3. Scan Mode
4. Discontinuous Mode
5. **Single Conversion Mode**

* does one conversion
* started by setting ***ADON*** bit in register ***ADC\_CR2*** or external trigger
* ***CONT*** bit should be 0
* If **Regular channel** was converted
  + Conversion data is in 16-bit register – ***ADC\_DR***
  + ***EOC*** flag is set
  + interrupt tis generated if ***EOCIE*** bit is set
* If **Injected channel** was converted
  + Conversion data is in 16-bit register – ***ADC\_DRJ1***
  + ***JEOC*** flag is set
  + interrupt tis generated if ***JEOCIE*** bit is set

1. **Continuous Conversion mode**

* ADC starts another conversion as soon as it finished one.
* started by setting ***ADON*** bit in register ***ADC\_CR2*** or external trigger
* ***CONT*** bit should be 1
* If **Regular channel** was converted
  + Conversion data is in 16-bit register – ***ADC\_DR***
  + ***EOC*** flag is set
  + interrupt tis generated if ***EOCIE*** bit is set
* If **Injected channel** was converted
  + Conversion data is in 16-bit register – ***ADC\_DRJ1***
  + ***JEOC*** flag is set
  + interrupt tis generated if ***JEOCIE*** bit is set

1. **Scan Mode**

* scan a group (either regular or injected)
* by setting ***SCAN*** bit in register -  ***ADC\_CR1***
* scans all channels in
  + ***ADC\_SQRx*** register for regular channels
  + ***ADC\_JSQRx*** register for injected channels
* a single conversion on each channel of the group
* After each end of conversion, the next channel of the group is converted automatically
* Depending on the ***CONT*** bit, conversion may be **Single** or **Continuous**
* ***DMA*** bit must be set to transfer the converted data to SRAM after each update of ***ADC\_DR***

1. **Discontinuous Mode**

* Convert subgroup of sequence on trigger
  + eg). n =3 and channel to converted are 0,1,2,3,6,7,9,10
  + first trigger, sequence converted 0,1,2 and EOC is generate
  + second trigger, sequence converted 3,6,7 and EOC is generate
  + third trigger, sequence converted 9,10 and EOC is generate
  + fourth trigger, sequence converted 0,1,2 and EOC is generate
  + and so on..
* for Regular group
  + enabled by setting ***DISCEN*** bit in ***ADC\_CR1*** register
  + n is set in ***DISCNUM[2:0]***in **ADC\_*CR1*** register
* for Injected group
  + enabled by setting **J*DISCEN*** bit in ***ADC\_CR1*** register
  + n is set in ***DISCNUM[2:0]***in **ADC\_*CR1*** register

**Note:**

* Single mode is one channel one time
* continuous mode is one channel continuous
* Scan mode is many channel(GROUP) conversion
  + may be single or continuous
* Discontinuous is few of many channel(GROUP) conversion
  + continuous

**ADC Calibration**

* built-in self-calibration
* should be done after power-up
* first set ***ADON*** bit
* wait at least two clock cycles
* ***CAL*** bit in ***ADC\_CR2*** register is set

**DMA request**

* DMA should be used in regular group for more than one channel conversion
* user can select the destination location for ADC\_DR register
* only ADC1 and ADC3 has DMA capability
* ADC2 can use Dual ADC mode for DMA

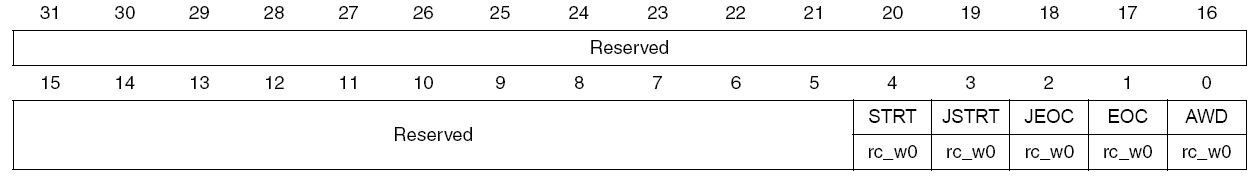
**Reading temperature**

1. Select the ADCx\_IN16 input channel
2. Select sample time of 17.1us
3. Set ***TSVREFE*** bit in ***ADC\_CR2*** register
4. set ***ADON*** bit
5. read the VSENSE in ADC\_DR register
6. Temperature = [(V25 - VSENSE)/ Avg\_Slope] + 25

|  |  |  |  |
| --- | --- | --- | --- |
| **ADC Channel** | **ADC1** | **ADC2** | **ADC3** |
| **ADC channel 0** | PA0 | PA0 | PA0 |
| **ADC channel 1** | PA1 | PA1 | PA1 |
| **ADC channel 2** | PA2 | PA2 | PA2 |
| **ADC channel 3** | PA3 | PA3 | PA3 |
| **ADC channel 4** | PA4 | PA4 |  |
| **ADC channel 5** | PA5 | PA5 |  |
| **ADC channel 6** | PA6 | PA6 |  |
| **ADC channel 7** | PA7 | PA7 |  |
| **ADC channel 8** | PB0 | PB0 |  |
| **ADC channel 9** | PB1 | PB1 |  |
| **ADC channel 10** | PC0 | PC0 | PC0 |
| **ADC channel 11** | PC1 | PC1 | PC1 |
| **ADC channel 12** | PC2 | PC2 | PC2 |
| **ADC channel 13** | PC3 | PC3 | PC3 |
| **ADC channel 14** | PC4 | PC4 |  |
| **ADC channel 15** | PC5 | PC5 |  |

**ADC Registers**

**ADC status register (ADC\_SR)**



**STRT – Regular channel Start flag**

* set by hardware and cleared by software
* set when regular channel conversion starts

**STRT – Injected channel Start flag**

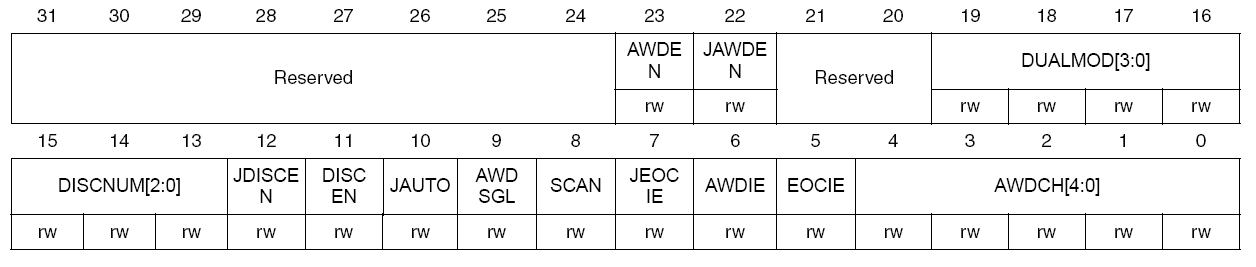
* set by hardware and cleared by software
* set when injected channel conversion starts

**JEOC – Inject Channel End of conversion**

* set by hardware and cleared by software
* 1 – all injected group channel conversion completed

**EOC – End of conversion**

* set by hardware and cleared by software
* 1 – conversion completed of regular of injected channel

**ADC control register 1 (ADC\_CR1)**

**DISCNUM [2:0]**

* defines the number for regular channels to be converted in discontinuous mode after receiving external trigger
* 000 – 1 channel, 111 – 8 channel

**JDISCENT – Discontinuous Mode on injected channel**

* **1 –** Discontinuous mode on injected channel enabled

**DISCENT – Discontinuous Mode on regular channel**

* **1 –** Discontinuous mode on regular channel enabled

**SCAN – Scan Mode**

* **1 –** enabled scan mode with the input selected by ***ADC\_SQRx*** or ***ADC\_JSQRX***

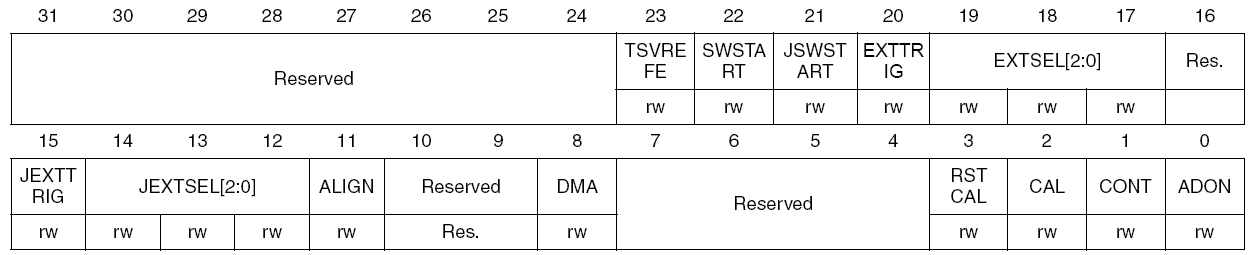
**JEOCIE – Interrupt enable for Injected channels**

* **1 –** enabled JEOC interrupt when JEOC bit is set for end of conversion interrupt by injected channels

**EOCIE – Interrupt enable for EOC**

* **1 –** enabled ECO interrupt when EOC bit is set for end of conversion interrupt by regular channels

**ADC control register 2 (ADC\_CR2)**

**TSVREF – Temperature sensor and VREFINT enable**

* **1-** enable temperature sensor and VREFINT channel

**SWSTART – Start conversion of regular channels**

* set by software cleared by hardware to start group of regular channels

**JSWSTART – Start conversion of injected channels**

* set by software cleared by hardware to start group of injected channels

**ALIN – Data alignment**

* **0 –** Right alignment, 1 – Left alignment

**DMA – Direct Memory access mode**

* set and cleared by software

**CAL – ADC Calibration**

* to start calibration
* set by software and cllared by hardware

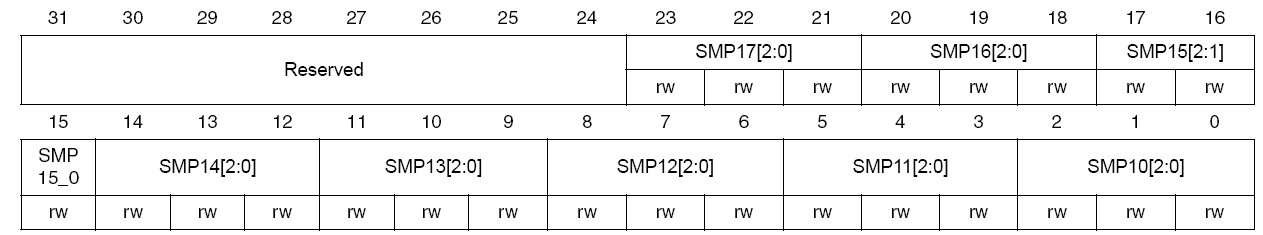
**CONT – Continuous conversion**

* **0 –** Single conversion mode
* **1 –** Continous conversion Mode

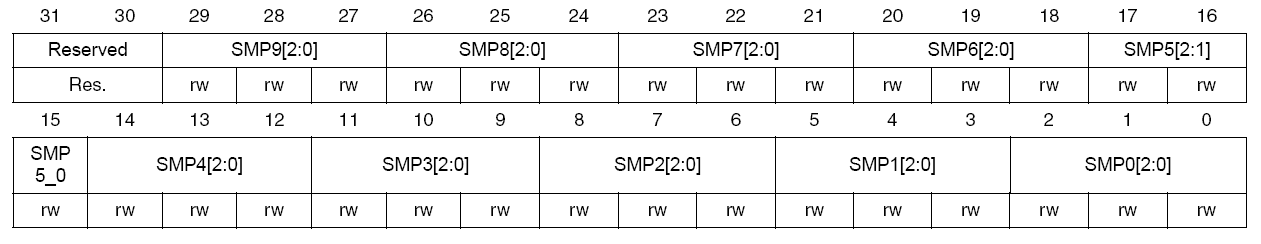
**ADON – ADC on/off**

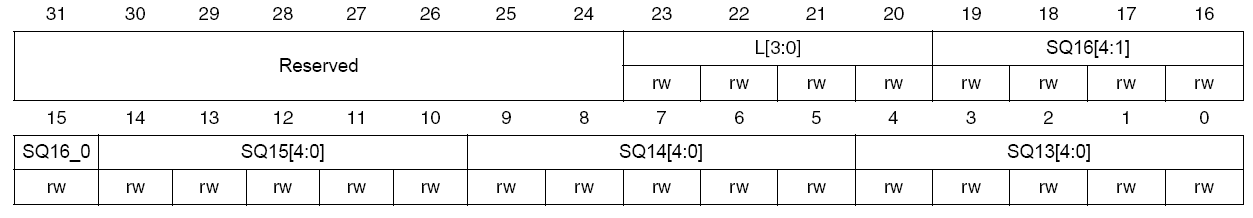
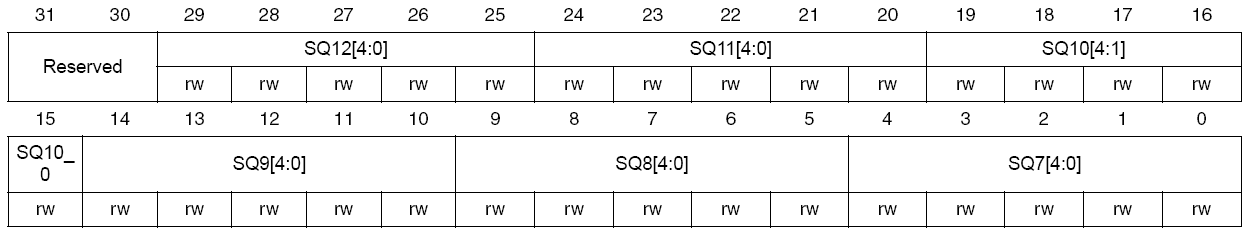
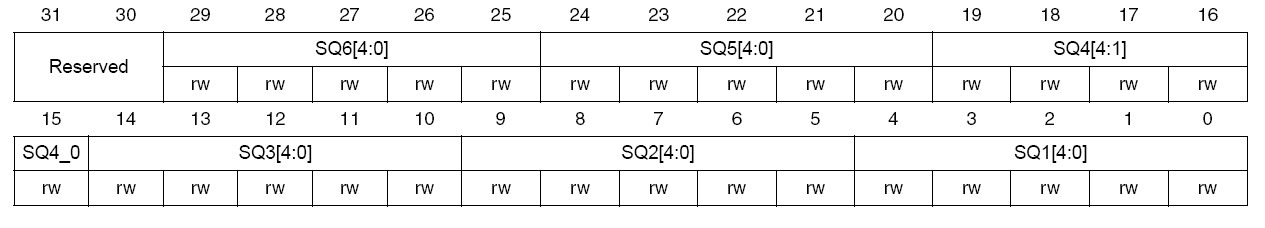
* **0 –** enable ADC and to start conversion

**ADC sample time register 1 (ADC\_SMPR1)**



**ADC sample time register 2 (ADC\_SMPR2)**



**ADC regular sequence register 1 (ADC\_SQR1)****ADC regular sequence register 2 (ADC\_SQR2)****ADC regular sequence register 3 (ADC\_SQR3)**

**L [3:0] - Regular channel sequence length**

* total number of conversion in regular channel conversion sequence

**SQ1z [4:0] – zth conversion in regular sequence**

* should be written with which channel