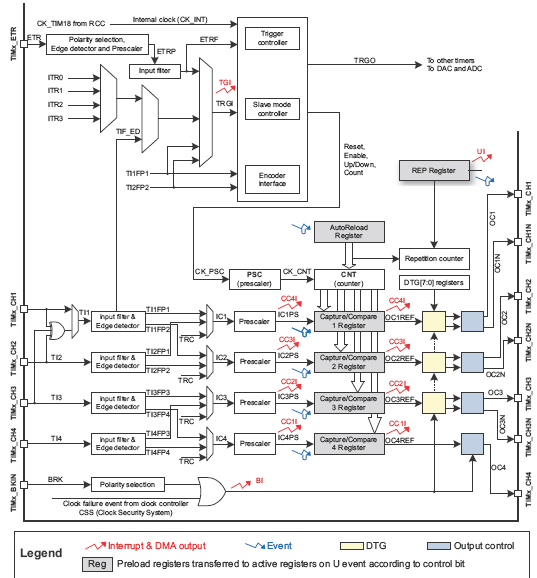
**Introduction**

* Timer 8 is available in high-density and XL-density devices
* 16-bit auto-reload counter driven by programmable Prescaler
* different from General purpose timers
* 16-bit up, down, up/down auto-reload counter
* 16-bit programmable Prescaler
* 4 Independent channels
  + Input Capture
  + Output Compare
  + PWM generation
  + One-pulse mode output
* Synchronization circuit to interconnect several timers together
* Interrupt/DMA generation on
  + Update – counter overflow/underflow, counter initialization (either software of internal/external trigger)
  + Trigger event (counter start, stop, initialization, count by internal/external trigger)
  + Input capture
  + Output compare
  + Break Input
* Incremental (Quadrature) encoder and hall-sensor circuitry for positioning purposes



**Functional Description**

**Time-base unit**

* **16-bit** counter with auto-reload register
* count up, down, up and down
* includes
  + Counter Register (***TIMx\_CNT***)
  + Prescaler Register (***TIMx\_PSC***)
  + Auto-reload Register (***TIMx\_ARR***)
  + Repetition counter Register (***TIMx\_RCR***)
* Auto-reload register is loaded to preload register and later to shadow register @
  + update event (***UEV***)
  + depending on ***ARPRE(***Auto-reload preload enable bit***)*** in ***TIMx\_CR1***
* Counter is clocked by Prescaler output ***CK\_CNT*** – enabled only when ***CEN*** bit in ***TIMx\_CR1*** register is set

**Note:**

**U**pdate event (***UEV***) is sent when the counter reaches overflow, underflow and the ***UDIS***bit is 0 in ***TIMx\_CR1***

***UEV*** event is disabled by setting ***UDIS*** bit in ***TIMx\_CR1***

When update event occurs (***UEV***),

* all the registers are updated
* the update flag (***UIF*** bit in ***TIMx\_SR***) is set depending on the ***USR*** bit
* the repetition counter is reloaded with ***TIMx\_RCR***
* auto-reload shoaddow register is updated with preload value (***TIMx\_ARR***)
* buffer of prescalre is reloaded with ***TIMx\_PSC***

**Prescaler description**

* divide the counter clock by any value between 1 and 65536
* 16-bit counter controlled through 16-bit register in ***TIMx\_PSC***
* can be changed on the fly – and it takes into account at the next update event

**Counter Modes**

1. **Up counting mode**

* counts up from 0 to auto-reload value and then restarts from 0 and generate overflow event
* if repetition counter is used, then ***UEV*** is generated after up counting is repeated for number of time programmed in repetition counter register +1 (***TIMx\_RCR + 1***)
* Else, the update event is generated at each counter overflow
* setting ***UG*** bit in ***TIMx\_EGR***register also generates ***UEV***
* setting the ***URS(***update request selection***)***  bit is set, and setting ***UG*** bit in ***TIMx\_EGR***register also generates ***UEV*** but without setting the ***UIF*** flag

1. **Down counting mode**

* counts down from auto-reload value down to 0 and then restarts from auto-reload value and generates a counter underflow event
* if repetition counter is used, then ***UEV*** is generated after down counting is repeated for number of time programmed in repetition counter register +1 (***TIMx\_RCR + 1***)
* Else, the update event is generated at each counter underflow
* setting ***UG*** bit in ***TIMx\_EGR***register also generates ***UEV***
* setting the ***URS(***update request selection***)***  bit is set, and setting ***UG*** bit in ***TIMx\_EGR***register also generates ***UEV*** but without setting the ***UIF*** flag

1. **Center-aligned mode (up/down counting)**

* counter counts from 0 to auto-reload value generates a counter overflow event then counts from auto-reload value to 1 and generates a counter underflow even and then restarts from 0
* active when ***CMS*** bits in ***TIMx\_CR1*** is not equal to 00
* output compare interrupt flag is set when
  + counter counts down (Center aligned mode 1, CMS=”01”)
  + counter counts up (Center aligned mode 2, CMS=”10”)
  + counter counts up and down (Center aligned mode 3, CMS=”01”)
* ***DIR*** bits updated by hardware gives the current direction of counter

**Repetition Counter**

* the UEV is generated only when the repetition counter reaches zeros
* the data are transferred from preload register to shadow register every N+1 counter overflows or underflows where N is the value in TIMx\_RCR repetition counter register
* The repetition counter is decremented
  + At each counter overflow in upcounting mode
  + At each counter underflow in downcounting mode
  + At each overflow and at each underflow in center-aligned mode
* repetition counter is auto-reload
* the repetition counter value is reloaded with concent of TIMx\_RCR when the update event is generated by software

**Clock selection**

* counter clock can be
  + Internal clock (CK\_INT)
  + External clock mode1 : External input pin
  + External clock mode2 : External trigger input pin
  + Internal trigger inputs (ITRx) : using one timer as prescaler for another timer

**Internal clock source (CK\_INT)**

* slave mode controller – disabled – SMS = 000
* CEN = 1
* prescaler is clocked by internal clock CK\_INT

**External clock source mode 1**

* when SMS = 111 in TIMx\_SMCR register
* each rising or falling edge on selected input

**External clock source mode 2**

* writing ECE = 1 in TIMx\_SMCR register
* each rising or falling edge on external trigger input ETR

**Capture/ Compare channels**