**RESET**

* System Reset, Power Reset, Backup domain Reset

**System Reset**

* Sets all registers to their reset values except the reset flags in clock Controller ***CSR*** register and the registers in Backup domain.
* Generated when
  1. Low level on the NRST pin (external reset).
  2. Window watchdog end of count condition (WWDG reset).
  3. Independent Watchdog end of count condition (IWDG reset).
  4. A software Reset (SW reset)
     + ***SYSRESETREQ*** bit in Cortex – M3 Application Interrupt and Reset Control Register must be forced to 1.
  5. Low-power Management reset
     + Reset generated when entering Standby Mode
       - Enabled by clearing ***nRST\_STBY*** bit in User Option Bytes.
       - Whenever Standby mode entry sequence is successfully executed, the system resets instead of entering Standby mode.
     + Reset when entering Stop Mode
       - Enabled by clearing ***nRST\_STOP*** bit in User Option Bytes.
       - Whenever Stop mode entry sequence in successfully executed, the device reset instead of entering Stop Mode.
* Reset sources is found in Control/Status register (***RCC\_CSR***).

**Poser Reset**

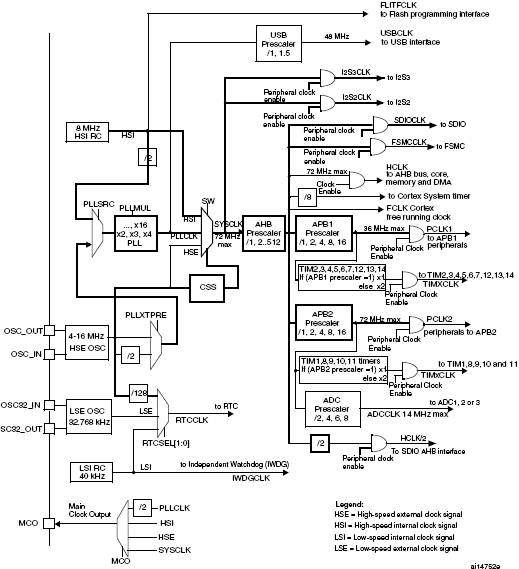
* Resets all register to their reset value, except the Backup Domain
* generated by

1. Power-on/ Power-down Reset (POR/ PDR reset)
2. When exiting Standby mode

**Backup Domain Reset**

* affects only the backup domain
* generated when
  1. Software reset triggered by setting ***BDRST*** bit in ***RCC\_BDCR*** (Backup Domain Control Register).
  2. VDD or VBAT power on, if both supplies have been powered off

**CLOCKS**



**Clock Tree**

* Three different clock sources to drive the system clock (***SYSCLK***)
  1. **HSI** oscillator clock (**High-Speed internal** clock signal)
  2. **HSE** oscillator clock (**High-Speed External** clock signal)
  3. PLL clock
* Also has two secondary clock sources
  1. 40 kHz **low speed internal** RC (**LSI** RC) – drives independent watchdog and optionally the RTC used for Auto-wakeup from Stop/ Standby mode.
  2. 32.768 kHz **low speed external** crystal (**LSE** crystal) – optionally drives the Real-time clock. (***RTCCLK***)
* When HSI is used as PLL clock input, the maximum system clock possible is 64MHz.
* The maximum frequency of AHB and APB2 domain is 72MHz.
* The maximum frequency of APB1 domain is 36MHz

***HCLK***

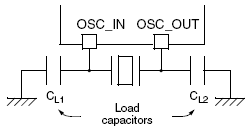
* AHB clock
* max 72MHz selected by AHB Prescalar
* derived from SYSCLK

**Usage**

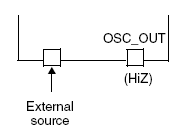
* System Timer (SysTick) external clock is fed HCLK/8
* SDIO AHB interface is clocked with HCLK/2.
* ADCs is clocked with High speed domain(APB2) divided by 2, 4, 6 or 8
* Flash Memory programmable interface clock (FLITFLCK) is always HSI clock (8 MHz) and is free running.
* USB Interface is clocked by PLL which must be programed to output 48 or 72MHz to get 48MHz USBCLK

**HSE clock**

* Generated by two sources
  1. HSE external crystal/ ceramic resonator (HSE crystal)



* + - 4 to 16 MHz external oscillator
    - Enabled by ***HSEON*** in ***RSS\_CR*** (Clock interrupt register).
    - Stability status is given by ***HSERDY*** flag in ***RSS\_CR***
  1. HSE user external clock (HSE bypass)



* + - max 25 MHz external clock source
    - enabled by setting ***HSEBYP*** and ***HSEON*** bit is ***RCC\_CR***
    - can be square, sinus, triangle with 50% duty cycle has to drive ***OSC\_IN*** pin, while ***OSC\_OUT*** pin must be left HI-Z.

**HSI Clock**

* generated by internal 8 MHz RC oscillator
* used directly as system clock
* divided by 2 to be used as PLL input
* faster setup time
* Stability status is denoted ***HSIRDY*** flag in ***RCC\_CR***
* Switched on by ***HSION*** bit setting in ***RCC\_CR***

**PLL Clock**

* can multiply either HSI RC output or HSE crystal output
* Before using, the following must be enabled
  1. the HSI oscillator divide by 2 or HSE oscillator for PLL input
  2. multiplication factor
* Interrupt can be generated when PLL is ready by enabling in ***RCC\_CIR*** (Clock Interrupt Register).

**LSE Clock**

* 32 kHz Low speed external crystal or ceramic resonator.
* low-power, high accurate for RTC
* ***LSEON*** bit must be set in Backup Domain Control (***RCC\_BDCR***).
* ***LSERDY*** bit in ***RCC\_BDCR*** gives stability status.
* Interrupt can be generated when ready by enabling in ***RCC\_CIR.***

**LSE Bypass (External Source)**

* up to 1MHz
* enabled by ***LSEON*** and ***LSEON*** in ***RCC\_BDCR***
* can be 50% duty cycle drive to ***OSC32\_IN*** while ***OSC32\_OUT*** should be left HI-Z

**LSI clock**

* LSI RC acts as low-power clock source runs in stop and standby mode for independent watchdog (IWDG) and Auto-wakeup unit (AWU).
* Clock frequency of 40 kHz (between 30 kHz to 60 kHz).
* ***LSION*** bit enables the LSI RC in Control/Status register ***RCC\_CSR***
* ***LSIRDY*** bit in ***RCC\_CRS*** indicates the stability status.
* only in high-Density, XL-density and connectivity line

**System Clock (SYSCLK) selection**

* After reset, HIS oscillator is selected as system clock.
* Status bit in Clock Control register (***RCC\_CR***).

**RTC clock**

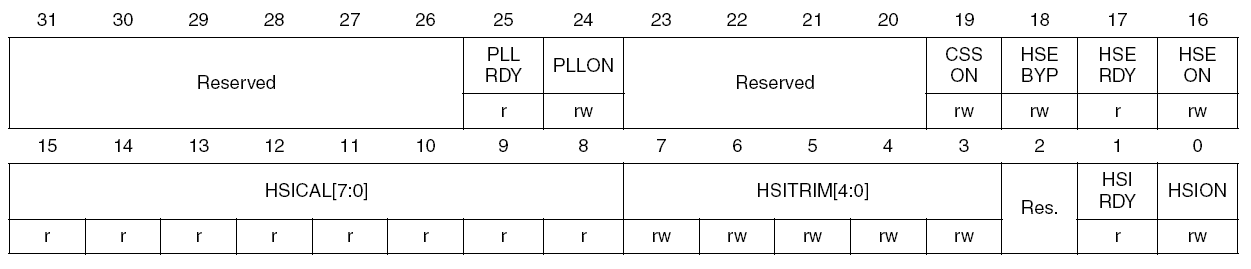
* ***RTCCLK*** clock can be HSE/128, LSE, LSI
* Selected by ***RTCSEL [1:0]*** in ***RCC\_BDCR*** (Backup domain control register).
  1. If LSE is selected as RTC clock – RTC continues to work even if the VDD supply is switched off only when VBAT supply is given.
  2. If LSI is selected as Auto-Wakeup Unit - AWU state is not guaranteed if the VDD supply is powered off.
  3. If the HSE/8 is selected as RTC clock - RTC state is not guaranteed if VDD supply is powered off or if the internal voltage regulator is powered off.

**Clock-out capability**

* Microcontroller clock output (MCO) allows output onto the external ***MCO*** pin
* Can be the following controlled by ***MCO[2:0]*** in Clock Configuration register ***RCC\_CFGR***
  1. SYSCLK
  2. HSI
  3. HSE
  4. PLL clock divided by 2

**RCC Registers**

**Clock Control Register (RCC\_CR)**



**PLLRDY – PLL Clock Ready Flag**

* Set by hardware
* 1 – indicates that the PLL is locked

**PLLON – PLL enabled**

* 1 – PLL clock is enabled
* Set and Cleared by hardware when entering Stop or Standby mode.

**CSSON – Clock Security System enabled**

**HSEBYP – External high-speed clock bypass**

* Set and cleared by software
* To bypass the oscillator with external clock.
* can be written only if HSE oscillator is disabled
* 1 – external 4 – 16 MHz oscillator bypassed with external clock

**HSERDY – External high-speed clock ready flag**

* Set by hardware indicating the HSE oscillator is stable
* 1 – HSE oscillator is ready

**HSEON – HSE clock enable**

* set and cleared by software
* cleared by hardware to stop the HSE oscillator when entering the stop and standby mode
* 1 – HSE oscillator ON

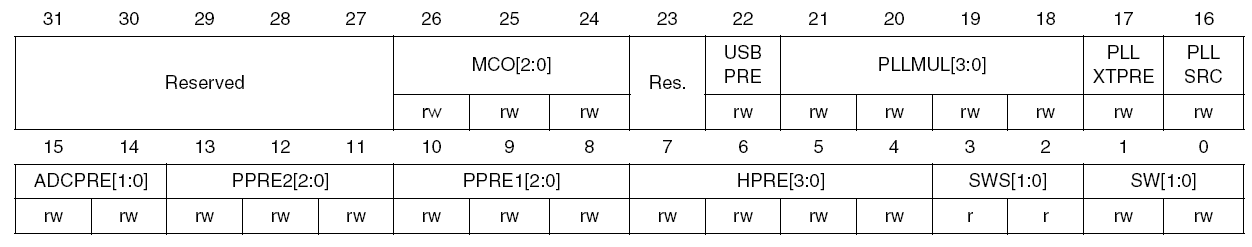
**HSIRDY – Internal high-speed clock ready flag**

* Set by hardware to indicate that internal 8 MHz oscillator is stable.
* 1 – stable 8 MHz oscillator

**HSION – Internal high-speed clock enable**

* Set and cleared by software
* 1 – Internal 8MHz RC oscillator ON.

**Clock configuration register (RCC\_CFGR)**



**MCO – Microcontroller clock output**

* can’t be more than 50MHz(maximum I\O speed)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **0xx** | **100** | **101** | **110** | **111** |
| No clock | SYSCLK | HSI clock | HSE clock | PLL clock / 2 |

**USBPRE – USB Prescaler**

* to generate 48MHz USB clock
* must be set before enabling USB clock in ***RCC\_ABP1ENR***
* 0 – PLL clock divided by 1.5
* 1 – PLL clock is not divided

**PLLMUL – PLL multiplication factor**

* **PLL** output can’t be more than 72MHz

|  |  |
| --- | --- |
| **PLLMUL** | **Multiplication Factor** |
| **0000** | PLL input clock x 2 |
| **0001** | PLL input clock x 3 |
| **0010** | PLL input clock x 4 |
| **0011** | PLL input clock x 5 |
| **0100** | PLL input clock x 6 |
| **0101** | PLL input clock x 7 |
| **0110** | PLL input clock x 8 |
| **0111** | PLL input clock x 9 |
| **1000** | PLL input clock x 10 |
| **1001** | PLL input clock x 11 |
| **1010** | PLL input clock x 12 |
| **1011** | PLL input clock x 13 |
| **1100** | PLL input clock x 14 |
| **1101** | PLL input clock x 15 |
| **1110** | PLL input clock x 16 |
| **1111** | PLL input clock x 16 |

**PLLXTPRE – HSE divider for PLL entry**

* **0 –** HSE clock not divided
* **1 –** HSE clock divided by 2

**PLL – PLL entry clock source**

* **0 -**  HSI oscillator clock/ 2 selected as PLL input clock
* **1 –** HSE oscillator clock selected as PLL input clock

**ADCPRE – ADC prescaler**

|  |  |
| --- | --- |
| **ADCPRE** | **ADC source** |
| **00** | PCLK2 divided by 2 |
| **01** | PCLK2 divided by 4 |
| **10** | PCLK2 divided by 6 |
| **11** | PCLK2 divided by 8 |

**PPRE2 – APB High-speed presclaer (APB2)**

|  |  |
| --- | --- |
| **PPRE2** | **APB2 CLOCK** |
| **0xx** | HCLK not divided |
| **100** | HCLK divided by 2 |
| **101** | HCLK divided by 4 |
| **110** | HCLK divided by 8 |
| **1111** | HCLK divided by 16 |

**PPRE1 – APB High-speed prescalar (APB1)**

* cant’ be more than 36MHz

|  |  |
| --- | --- |
| **PPRE1** | **APB1 CLOCK** |
| **0xx** | HCLK not divided |
| **100** | HCLK divided by 2 |
| **101** | HCLK divided by 4 |
| **110** | HCLK divided by 8 |
| **1111** | HCLK divided by 16 |

**HPRE – AHB Prescaler**

|  |  |
| --- | --- |
| **HPRE** | **HCLK (AHB clock)** |
| **0xxx** | SYSCLK not divided |
| **1000** | SYSCLK divided by 2 |
| **1001** | SYSCLK divided by 4 |
| **1010** | SYSCLK divided by 8 |
| **1011** | SYSCLK divided by 16 |
| **1100** | SYSCLK divided by 64 |
| **1101** | SYSCLK divided by 128 |
| **1110** | SYSCLK divided by 256 |
| **1111** | SYSCLK divided by 512 |

**SWS – System clock switch status**

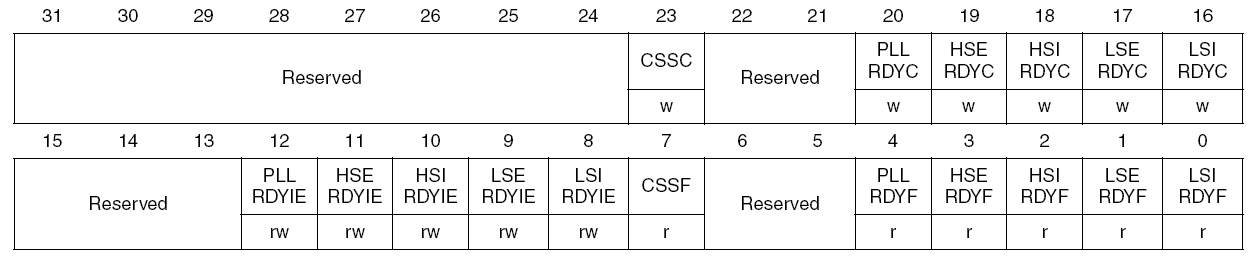
|  |  |
| --- | --- |
| **SYS** | **Which is used as system clock** |
| **00** | HSI oscillator |
| **01** | HSE oscillator |
| **10** | PLL |

**SW – System clock**

* to select SYSCLK source

|  |  |
| --- | --- |
| **SYS** | **System Clock** |
| **00** | HSI oscillator |
| **01** | HSE oscillator |
| **10** | PLL |

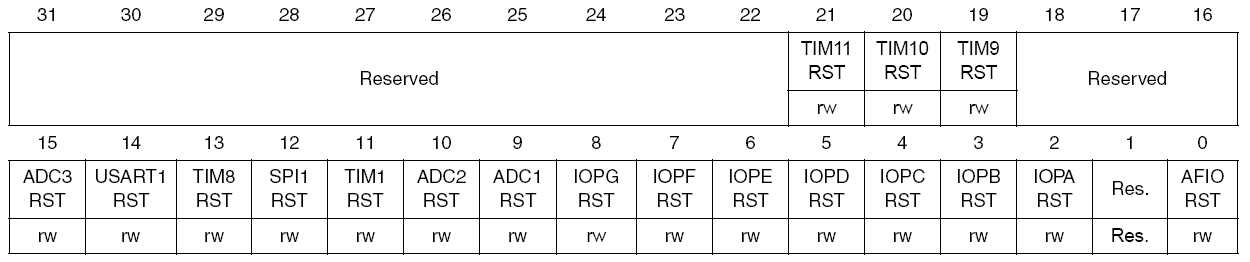
**Clock interrupt register (RCC\_CIR)**



-- see datasheet

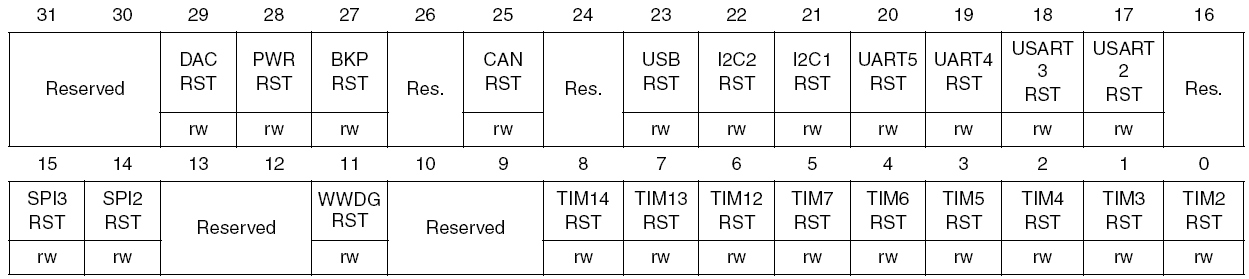
**APB2 peripheral reset register (RCC\_APB2RSTR)**

* 1 - to reset particular APB2 peripheral



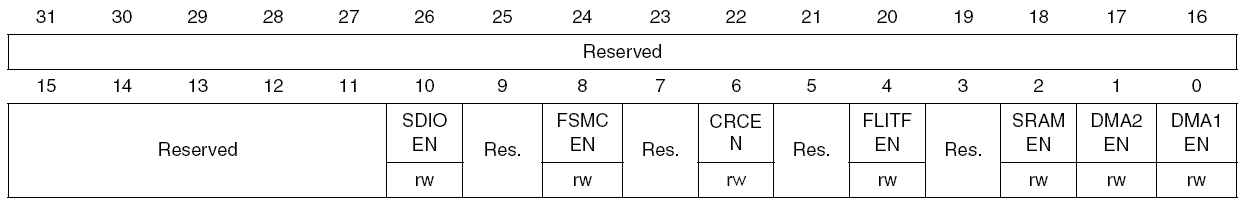
**APB1 peripheral reset register (RCC\_APB2RSTR)**

* 1 - to reset particular APB1 peripheral



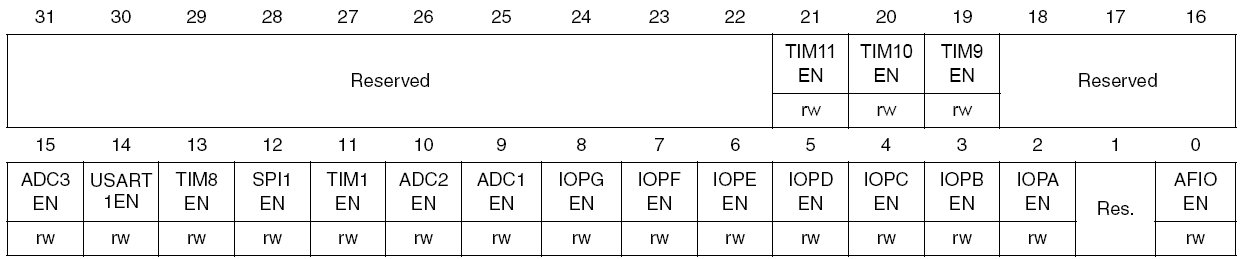
**AHB peripheral clock enable register (RCC\_AHBENR)**

* **1 –** enable AHB peripheral clocks



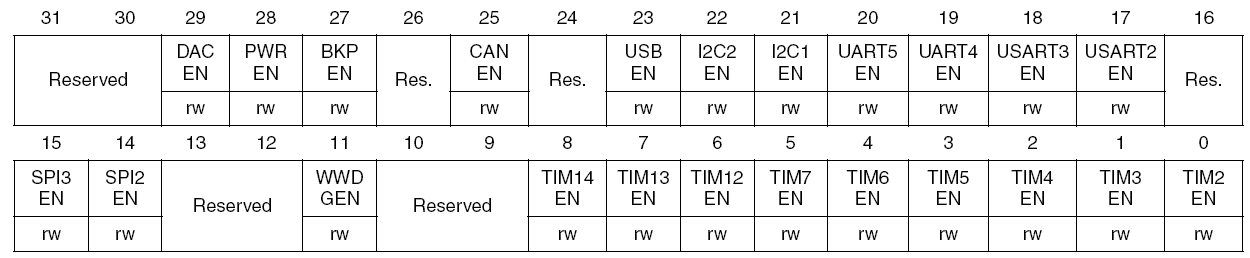
**APB2 peripheral clock enable register (RCC\_APB2ENR)**

* **1 –** enable APB2 peripherals



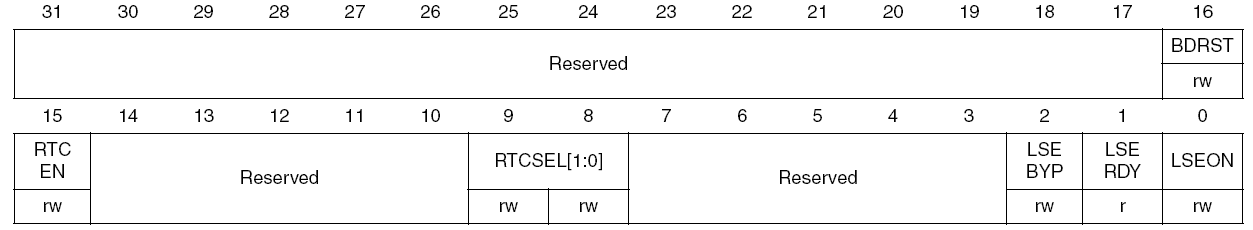
**APB1 peripheral clock enable register (RCC\_APB1ENR)**

* **1 –** enable APB1 peripherals



**Backup domain control register (RCC\_BDCR)**

* ***LSEON, LSEBYP, RTCSEL, RTCSEL*** of ***RCC\_BDCR*** can be modified only when ***DBP*** bit of ***PWM\_CR***.



**BDRST – Backup Domain Software reset**

* **1 –** reset the entire Backup domain

**RTCEN – RTC CLOCK ENABLE**

* **1 –** enable RTC clock

**RTCSEL [1:0] - RTC clock source selection**

* select the clock source for RTC
* Once selected, can only be changed when Backup domain rest.
* BDRST bit is used to reset.

|  |  |
| --- | --- |
| **RTCSEL [1:0]** | **Clcok Source** |
| **00** | No clock |
| **01** | LSE oscillator |
| **10** | LSI oscillator |
| **11** | HES oscillator clock / 128 |

**LSEBYP – External Low-speed oscillator bypass**

* Set and cleared by software to bypass oscillator in debug mode.
* Written only when external set and cleared by software to bypass oscillator in debug mode.
* Written only when external 32 kHz oscillator is disabled.
* 1 – LSE oscillator bypassed.

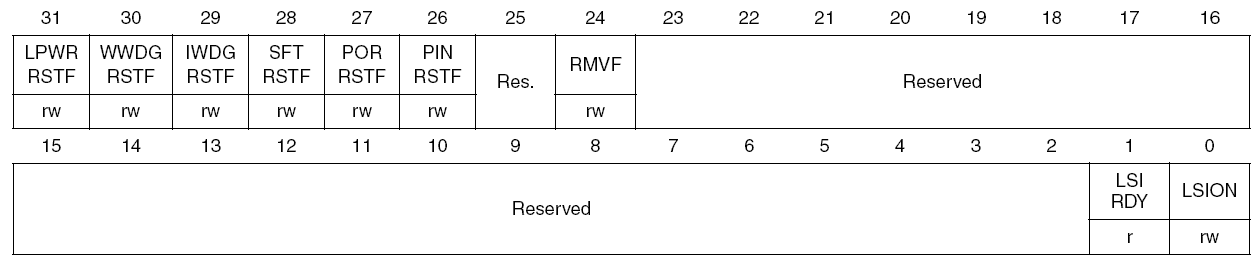
**LSERDY – External Low-speed oscillator ready**

* set and cleared by hardware to indicate when the external 32 kHz oscillator is stable.
* 1 – External 32 kHz oscillator is ready

**LSEON – External Low-speed oscillator enable**

* set and cleared by software
* 1 – External 32 kHz oscillator ON

**Control/status register (RCC\_CSR)**



**LSIRDY – Internal Low-speed oscillator ready**

* set and cleared by hardware to indicate when the internal 40 kHz oscillator is stable.
* 1 – internal 40 kHz oscillator is ready

**LSION – Internal Low-speed oscillator enable**

* set and cleared by software
* 1 – Internal 40 kHz oscillator ON