Narendran

VLSI Verification, Emulation/ Validation, RTL Designer

Bangalore
+91 99 00 238 737
narenkn@gmail.com
narenkn@narenkn.com

www.narenkn.com

GitHub: www.github.com/narenkn

EXPERIENCE

AMD, Bangalore — *PMTS*

4 August 2008 - PRESENT

DFT Verification, Gatesim, Scandump, SATA/PCIE Verification, Infinity Fabric Verification, Infinity Fabric Emulation.

TooMuch Semiconductor Solutions, Bangalore — *Director*

5 July 2004 – 31 July 2008

System Verilog and Conventional Verification, C++ based stimulus with PLI/VPI.

Texas Instruments, Bangalore — *IC Design Engineer*

5 Mar 2001 – 30 June 2004

RTL Design, STA, DFT/ATPG, Functional Test Vectors, Specman/E Verification.

EDUCATION

PSG College of Technology, Coimbatore — *Master of Engineering (Applied Electronics)*

AUGUST 1999 - JANUARY 2001

Presented thesis paper in "Innovative approaches to increase cycle-length of PRBS during generation of white-noise" in REC Suratkal, Year 2000.

Class Representative.

Amrita Institute of Technology, Coimbatore — *Bachelor of Engineering (Electrical and Electronics Engineering)*

SEPTEMBER 1995 - APRIL 1999

Only team to win industry sponsorship project- "Premier Electronics Pvt. Ltd." during academic year 1998-99.

Secured 3rd place in EEE batch of '99

SKILLS

VLSI Verification, C++ based Verification, Emulation, RTL Design, STA

AWARDS & RECOGNITIONS

SNUG-2013 Won Best Paper Award (Innovative Approach to Overcome Limitations of Netlist Simulations, Co-Author) with a cash prize of ₹25,000/-. [AMD 2013]

Filed Patent Application "Playback Methodology for Verification Components" (https://patents.google.com/patent/US20130024178A1/en). [AMD 2011]

Surfboard Tool Surfboard application provides python access to FSDB data. Used by multiple teams for power analysis, micro-benchmarking and debug automation/ signature classification. [AMD 2015]

Won a team challenge contest with cash award to make a best ECO fix for RTL change.[TI 2001]

Recognition from Director for FakeDFxEnv - Innovative solution to prefetch DFT verification activity with soft model of JTAG tap hierarchy specification.

TDLEdit TDLEdit is a perl utility that provides procedural access to Tester Vectors of any Automated Test Equipment (ATE). Recognized for reducing functional vector development and qualification process by 30%.

INDUSTRY PROJECTS

Infinity Fabric Emulation Owner— *AMD*

Owner of Emulation based verification of atleast 7 different products, spanning **three generations**. Methodologies used were Synthesisable TB, Simulation Acceleration. Noted for **enhancing Simulation Acceleration by a large factor**. Hands-on on QT & Veloce platforms.

CPU Exerciser's Verification Lead — AMD (2015-2016)

Lead for 5 different x86/A64 random stimulus generators, including multi-threading, power state changes, privilege changes.

SOC Verification Lead — AMD (2014-2015)

India Lead for the SOC Verification team with ARM's A64 processor together with a host of peripherals like PCIE, SATA, DDR. Owner for different SOC test plans. Designed and **architected the C utility library** used in SOC tests.

DFT, Scandump, Gatesim Verification Lead — AMD (2008-2013)

DFT Features such as JTAG, Clocking, LBIST, MBIST, Low power and power gating modes, JTAG checks, Clock freeze, Scan, Design for Debug (HDT/DSM), RO/Thermal.

Ownership on Multicore CPUs and Fusion SOCs.

Director — TooMuch Semiconductor Solutions (2004-2008)

Client Projects Executed and delivered different projects for Broadcom, Qualcomm, Montalvo Systems, Synopsys.

Incorporation and Growth of TooMuch Founding member of TooMuch and helped grow to a 30-member organization before exit by sale to Blueberry Design Services.

IC Design Engineer / SOC Verification Lead — Texas Instruments (2001-2004)

RTL Design – DDR Memory Controller Enhancemens; LEC; Spec Author.

DFT – Scan & ATPG Ownership; Functional Test Vector generation and creation of new vector generation process.

Verification – Unit level with E-language; Back-annotated netlist simulations; Regression maintenance and debug team lead for SOCs with varied peripherals (UART, SCI, SPI, CAN, I2C, SMBUS).

Emulation – Ownership to bringup of SOC on QuickTurn to aid silicon bringup and software development. Considerably Enhanced Synthesisable TB used for this effort.

Application Notes Authored two different application notes for usage of Self-Refresh mode in DRAM and another to interface 256Kbit SDRAM. [TI 2002]

Community Contributions

cDump - a library to enable dumping of C variables into FSDB.

svTypes - a library that eases the transfer of multi-bit values from/to C program.

Surfboard – library that enables python script access to waveform data stored as FSDB files.

Opencores Few projects contributed in www.opencores.org and were used by community. [TooMuch 2006-2008]. AHB2Wishbone, Wishbone2AHB, AHB Arbiter, I2C Master-Slave

Internal Presentations

JTAG tools to reduce Time to Verification - solution to handle JTAG30 pipeline flops with no effort. Judged runnerup paper in Vidyuth 2011, award with cash prize and trophy.

Rebirth of dual-sim approach to Gatesims – Improved gatesim methodology to run 10x faster. Won Poster award in AATC 2013.

Scansim - Environment to validate single chain scandump vectors (instead of Emulator). Won Poster award in AATC 2012.

AutoIPConfig - An enhancement to verification infrastructure for automatic IPConfig programming. [Selected as poster AATC 2011]

TDLEdit – Paper presented and recognized with certificate.