CMOS Design Project

Indian Institute of Information Technology, Nagpur

ECL 312: CMOS Design

A Project Report on: 2 Bit Flash ADC using Subthreshold Technique

Submitted By:

Naresh Godara (BT23ECI013)

Under the Guidance of:

Prof. Paritosh Peshwe

Department of Electronics and Communication

Project Overview

A Flash Type ADC, also known as a Parallel ADC, is one of the fastest types of analog-to-digital converters. It operates by comparing the input analog signal to multiple reference voltages simultaneously, converting the analog signal to its corresponding digital value in a single step. Due to its high speed, it is commonly used in applications requiring rapid signal processing, such as in high-frequency communication systems, oscilloscopes, and video systems.

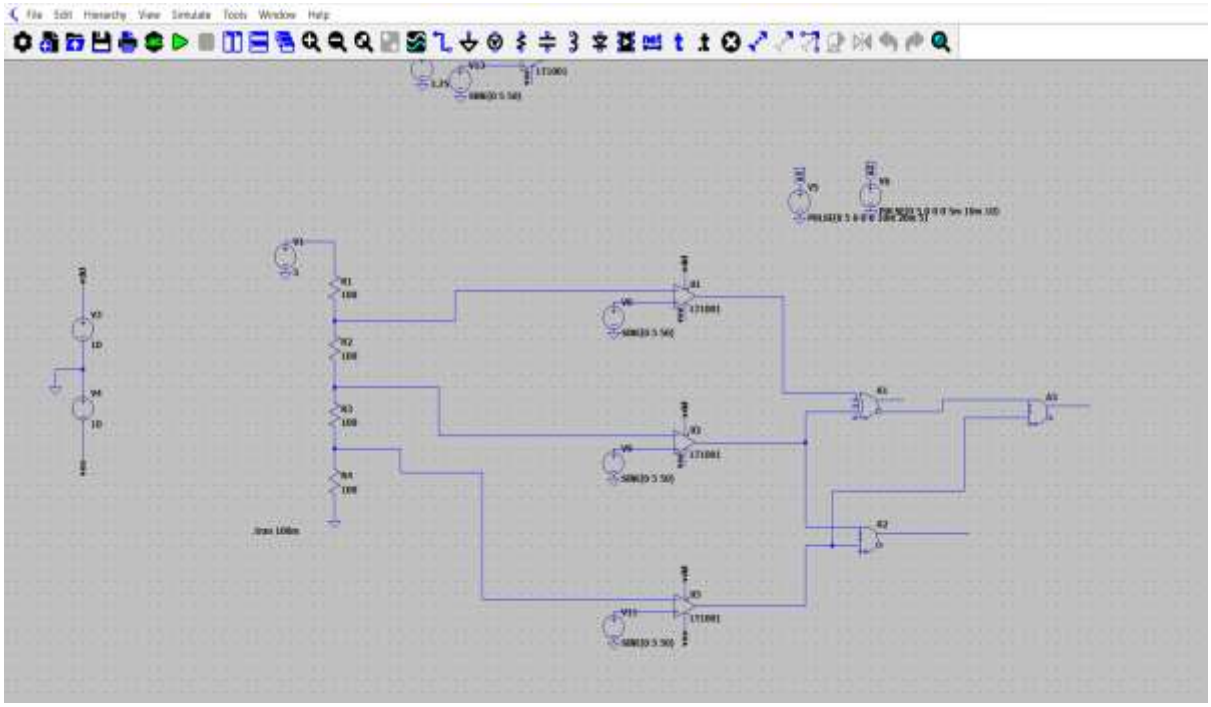
Working Principle of Flash ADC

The core working principle of a Flash ADC revolves around the use of a network of comparators and resistors that convert an analog input into a digital output almost instantly. Let's break down the process:

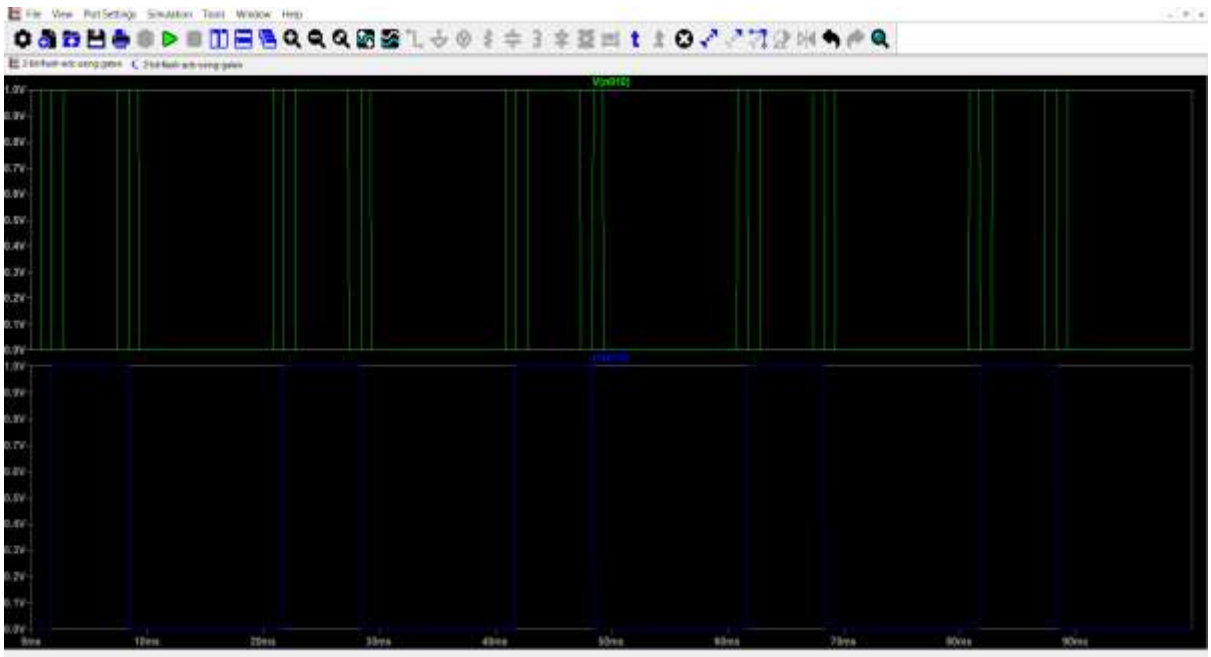
- **Resistor Ladder Network:** A resistor ladder network is used to generate a set of reference voltages. This network consists of equal-value resistors connected in series between the reference voltage (usually the power supply voltage) and ground. The voltage drop across each resistor creates multiple reference voltages.
- **Comparator Array:** A series of comparators is connected to each node of the resistor ladder network. Each comparator compares the input analog voltage with its respective reference voltage. If the input signal is higher than the reference voltage, the comparator outputs a logical "1." If it is lower, the output is a logical "0".
- **Encoder:** The outputs of the comparators are then fed into a digital encoder. The encoder takes the raw comparator outputs (which may be in a thermometer code format) and converts them into a binary code, representing the digital equivalent of the analog input.
- **Digital Output:** The encoder produces the final binary output, which represents the input analog signal as a digital value.

This process occurs in a single clock cycle, which is why Flash ADCs are known for their ultra-fast conversion times.

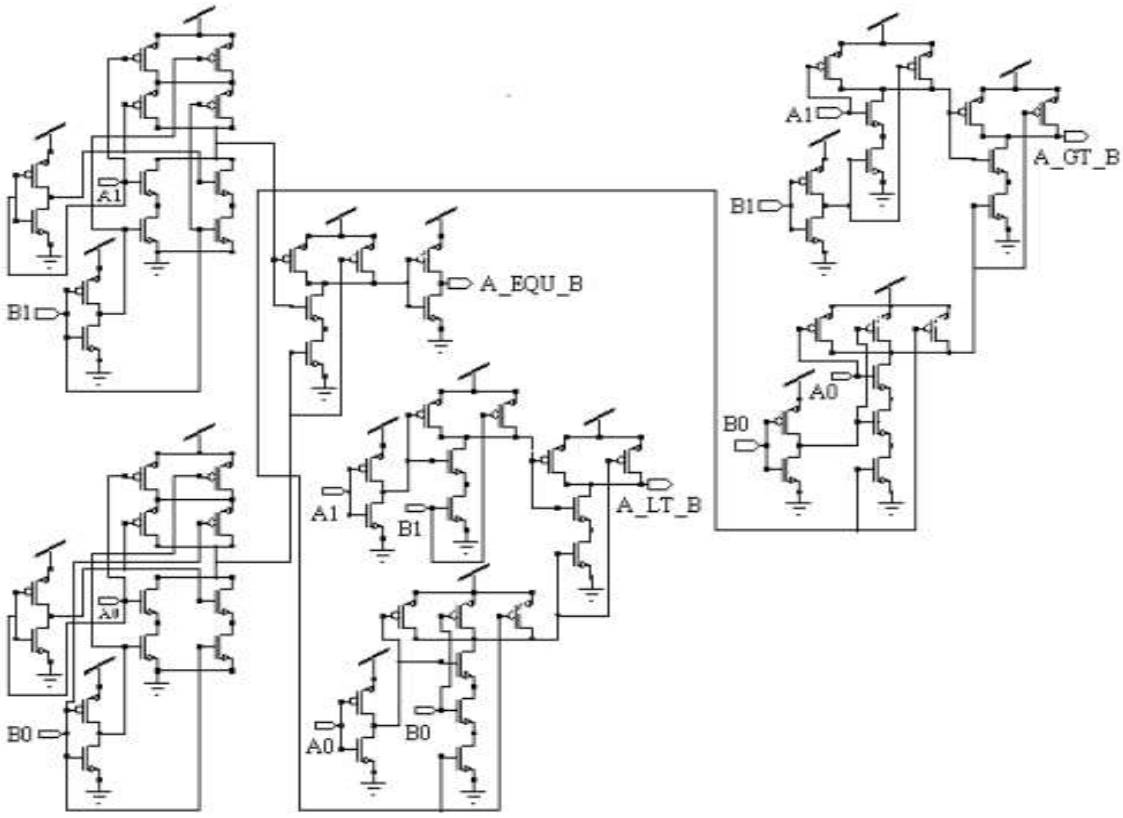
Circuit of 2 Bit Flash ADC using gates and Operational Amplifier



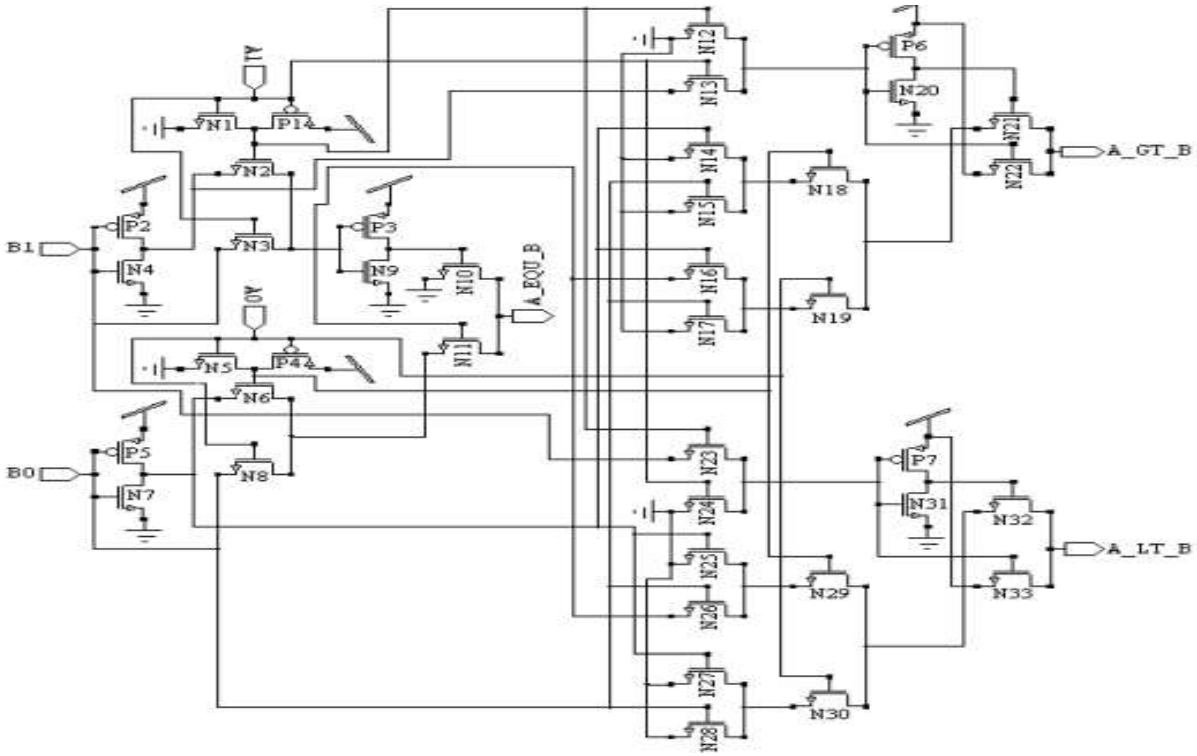
Output of Above Circuit for Sine Wave



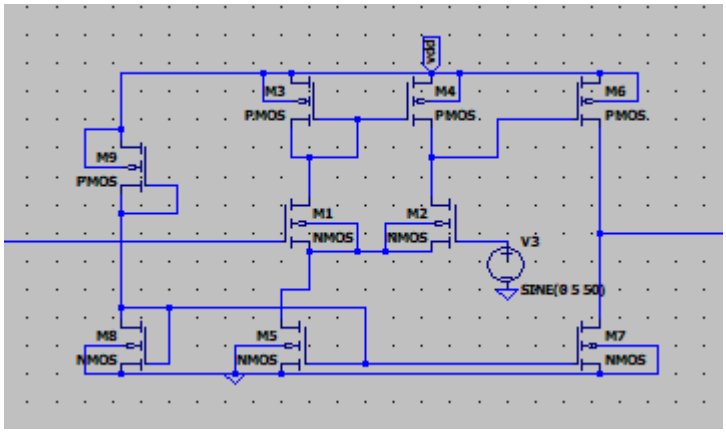
Realization of Operational Amplifier using CMOS Technology



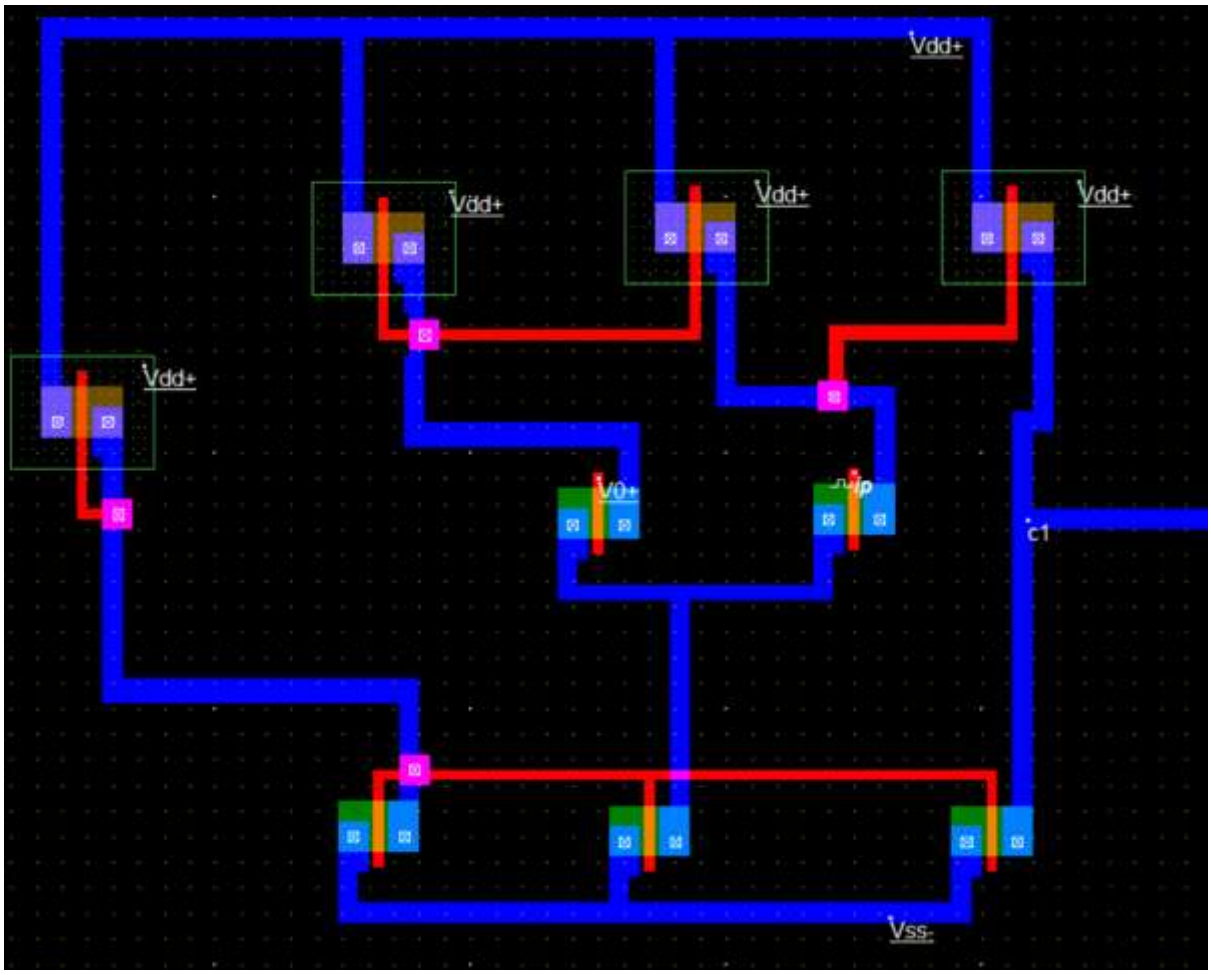
Simplification of above circuit using Pass Transistor Logic



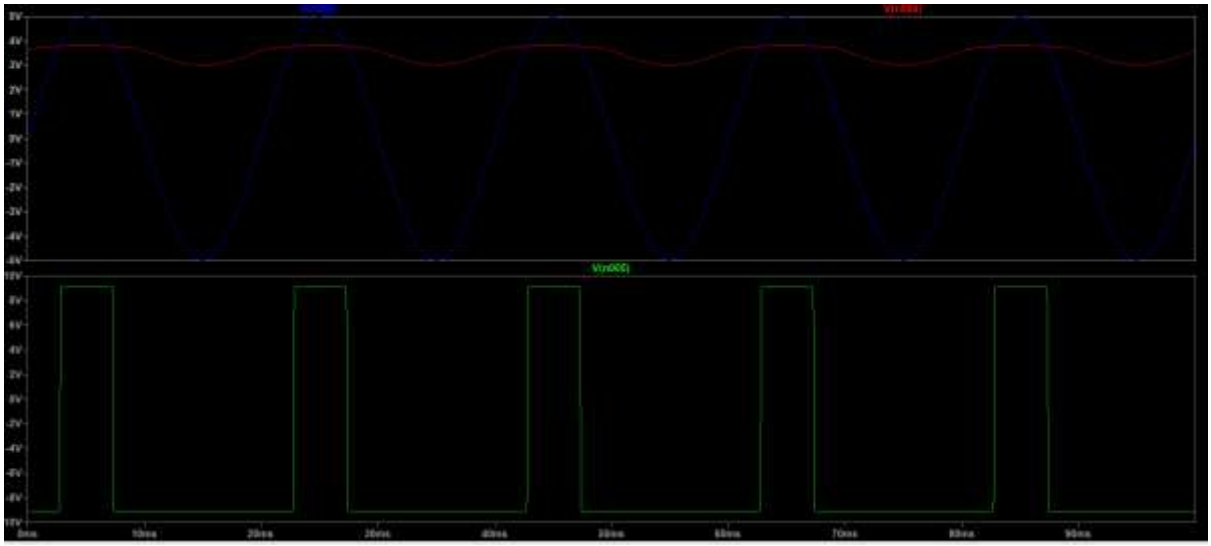
Novel Comparator Design



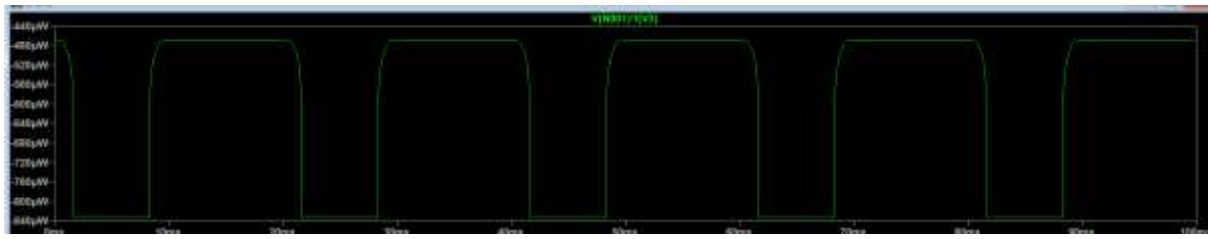
Novel Comparator Design in Microwind



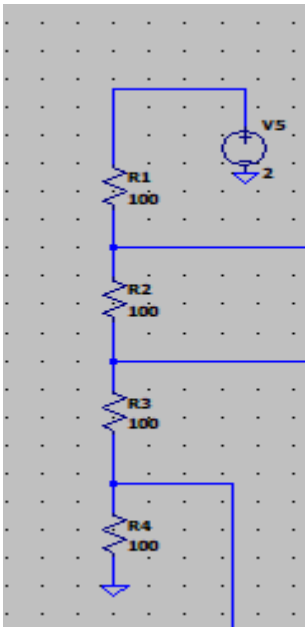
Comparator Output for given two inputs

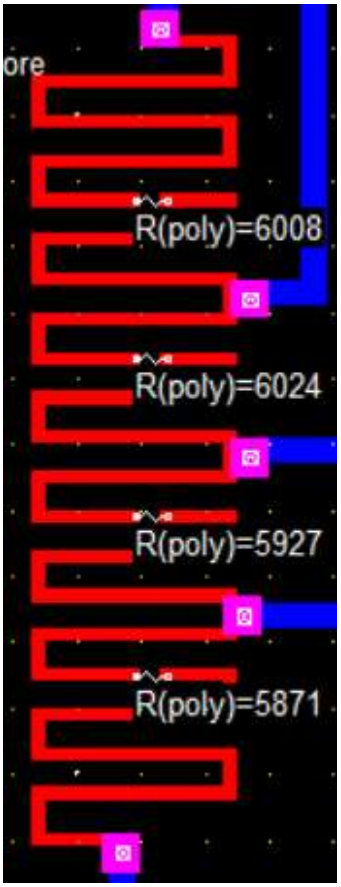


Power in Above Comparator

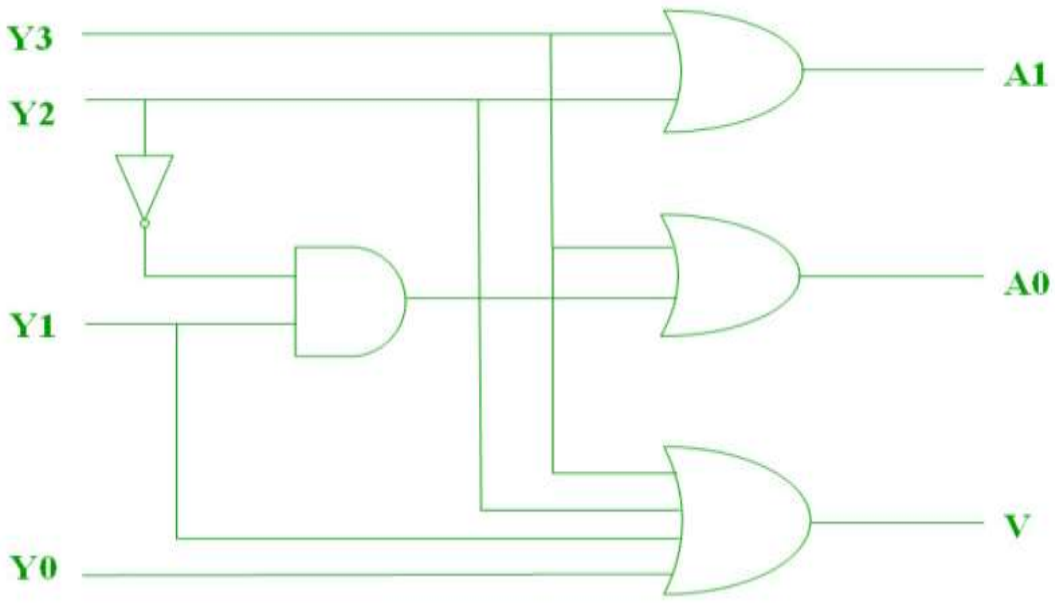


Voltage Divider Circuit in LTSpice and Microwind

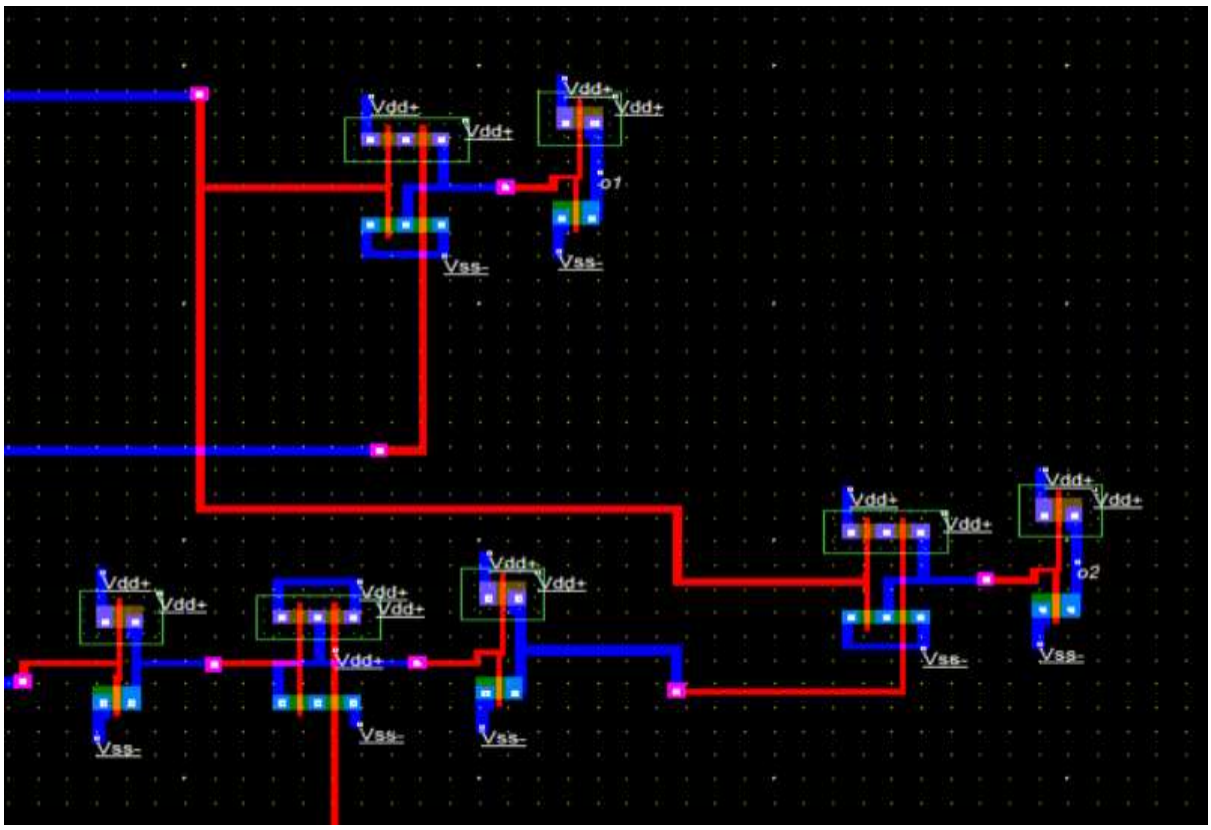




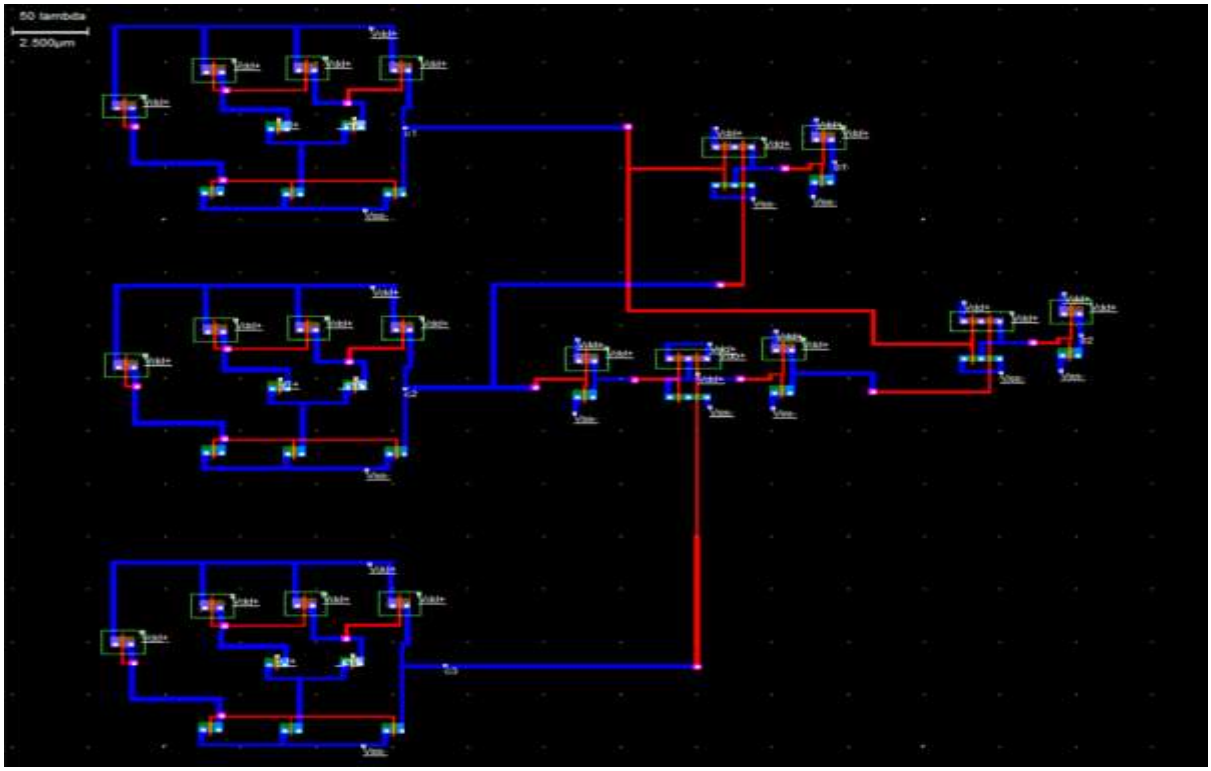
Priority Encoder using Gates



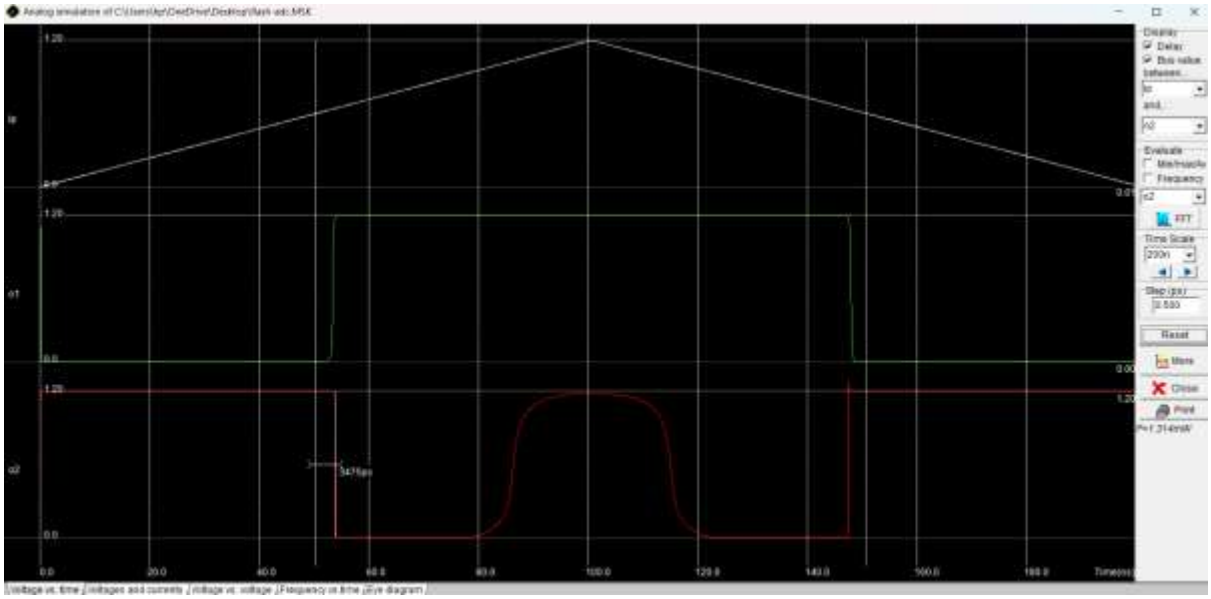
Priority Encoder realized using CMOS



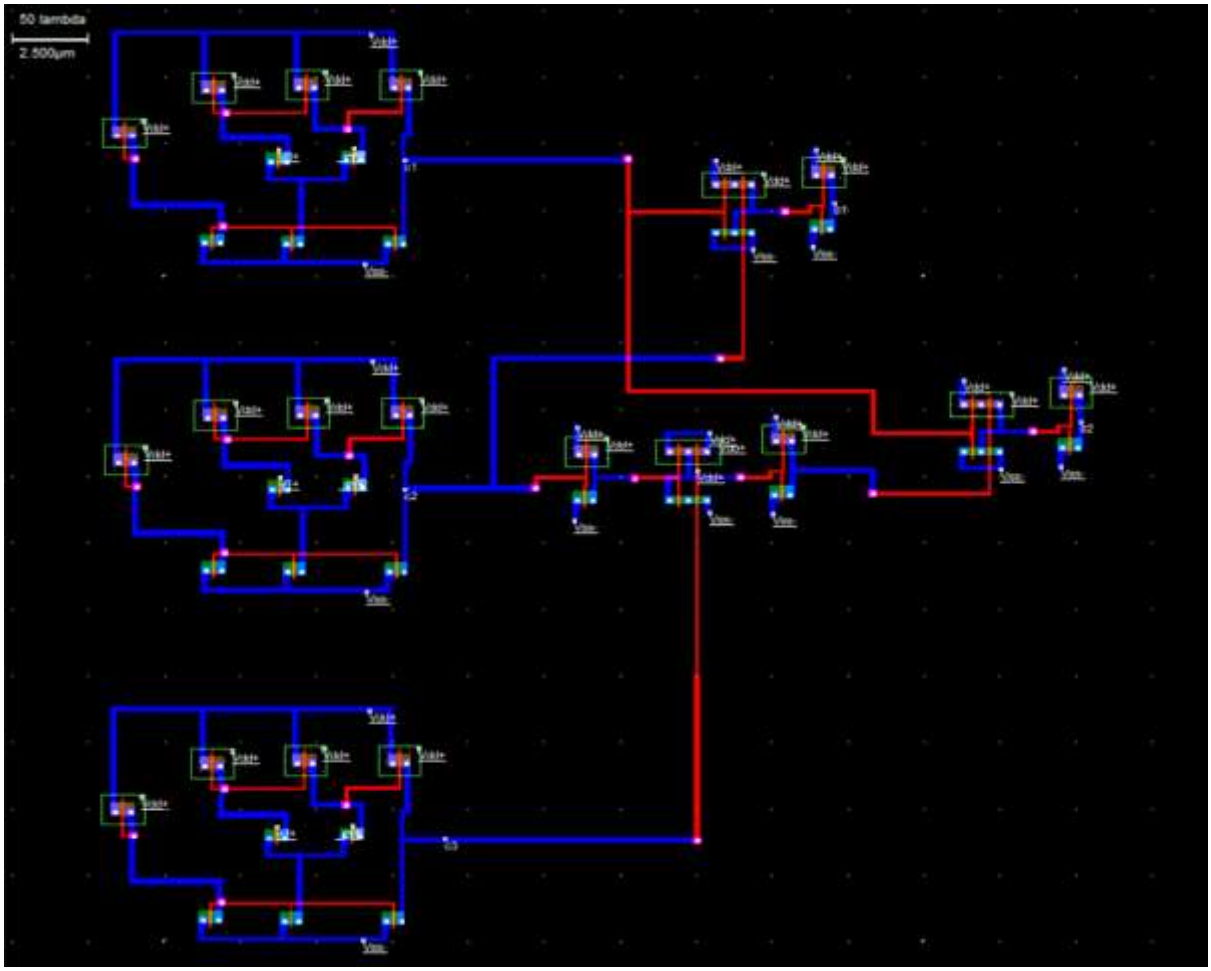
Full 2 Bit Flash ADC realized using CMOS in Microwind



Output of 2 Bit Flash ADC when input is a triangular wave



Full 2 Bit Flash ADC using Subthreshold Technique



Working Principle of 2 Bit Flash ADC

The working principle of the 2-bit Flash ADC is based on comparing the input voltage (V_i) to reference voltages. Depending on the range in which the input voltage falls, the output of the comparators is either high (positive saturation) or low (negative saturation).

- If the voltage at the non-inverting input terminal is higher than the voltage at inverting terminal the output is in a positive saturation state.
- Similarly, if the voltage at the non-inverting input terminal is lower than the voltage at inverting terminal the output is in a negative saturation state.
- When the analog input voltage is seen to be less than V/4, the voltage at non-inverting terminals of all three comparators will be less than their respective inverting input terminals. Thus, the output from comparator $C_1C_2C_3 = 000$ and the digital output will be $b_2b_1 = 00$
- When the analog input voltage is seen to be between V/4 and V/2, the output from comparator $C_1C_2C_3 = 100$, and the digital output will be $b_2b_1 = 01$.
- When the analog input voltage is seen to be between V/2 and 3V/4, the output from comparator $C_1C_2C_3 = 110$, and the digital output will be $b_2b_1 = 10$.
- When the analog input voltage is seen to be between 3V/4 and V, the output from comparator $C_1C_2C_3 = 111$, and the digital output will be $b_2b_1 = 11$.

2 Bit Flash ADC Encoding Technique

The following table shows the comparator and digital outputs for a 2-bit Flash Type A/D Converter.

Analog Input Voltage (Vi)	Comparator Output			Digital Output	
	C_1	C_2	C_3	b_2	b_1
$0 \le Vi \le V/4$	0	0	0	0	0
$V/4 < Vi \le V/2$	1	0	0	0	1
$V/2 < Vi \le 3V/4$	1	1	0	1	0
$3V/4 < Vi \le V$	1	1	1	1	1

- Four ranges of analog input voltages are present for a 2-bit Flash-type A/D converter. Thus, a 2-bit digital output (b_2b_1) needs to be coded.
- From the table it can be seen that b_2 is 1 for $C_1C_2C_3$ = 110 and $C_1C_2C_3$ = 111. Thus, the expression for b2 in terms of C_1, C_2, and C_3 is given as follows.

  $b_2=C_1C_2C_3 +C_1C_2C_3 =C_1C_2C_3 +C_3$

  $b_2=C_1C_2$
- It can be seen that b_1 is 1 for $C_1C_2C_3$= 100 and $C_1C_2C_3$ = 111. Thus, the expression for b1 in terms of C_1, C_2, and C_3 is given as follows.

  $b_1=C_1C_2C_3 +C_1C_2C_3 =C_1(C_2C_3 +C_2C_3)$

  $b_1=C_1(C_2C_3)$
- The LSB bit b_2 is obtained by the AND operation of comparator output C_1 and C_2. Thus an AND gate has to be used.
- The MSB bit b1 is obtained by the AND operation of comparator output C1 and XNOR of comparator output C_2 and C_3. Thus, one AND gate and one XNOR gate are required.
- Thus, the coding circuit can be formed by applying comparator outputs C2 and C1 through an AND gate to get the LSB bit and by applying comparator outputs C_2 and C_3 through an XNOR gate and then passing this output and comparator output C_1 through an AND gate to get the MSB bit.

Here C1, C2, C3 are outputs of Comparators and b1, b2 are outputs of Priority Encoder.

Advantages of Flash ADC

- High Speed: Flash ADCs are the fastest type of ADC due to their parallel structure. They can convert analog signals to digital values in a single step, making them ideal for real-time and high-frequency applications.
- Simple Operation: The concept of comparing input signals against predefined reference voltages is straightforward, resulting in reliable and efficient operation.
- Low Latency: With no need for intermediate steps or multiple clock cycles, Flash ADCs offer minimal latency in the conversion process.

Disadvantages of Flash ADC

- **High Power Consumption:** Flash ADCs require a large number of comparators, especially for higher resolution designs (e.g., an 8-bit Flash ADC requires 255 comparators). This increases power consumption significantly.
- **Large Size and Complexity:** The number of required components, especially comparators, grows exponentially with the resolution. For instance, a 10-bit Flash ADC would require 1023 comparators, making it impractical for certain applications where size or cost is a concern.
- **High Cost:** Due to the large number of components, the cost of manufacturing Flash ADCs can be higher compared to other types of ADCs.

Conclusion

A 2Bit Flash ADC was realised using CMOS technology, in this project and is improved using techniques like subthreshold. Power is reduced significantly through this technique.

Power Comparison of these techniques is shown in below table:

Device	180nm	45nm	Subthreshold Technique
2 Bit Flash ADC (Power)	0.935mW	0.961uW	0.950uW
Delay in Circuit	1865ps	3095ps	6070ps

Netlist of 2 Bit Flash ADC compatible with LTSpice

```
* C:\Users\hp\OneDrive\Desktop\2bit-flash-adc.asc
* Generated by LTspice 24.1.9 for Windows.
V1 vdd 0 5
R1 N001 N002 100
R2 N002 N009 100
R3 N009 N015 100
R4 N015 0 100
M10 N018 N009 N024 N024 NMOS
M11 N019 N025 N024 N024 NMOS
M12 vdd N018 N018 vdd PMOS
M13 vdd N018 N019 vdd PMOS
M14 N024 N022 0 0 NMOS
M15 vdd N019 N003 vdd PMOS
M16 N003 N022 0 0 NMOS
M17 N022 N022 0 0 NMOS
M18 vdd N022 N022 vdd PMOS
M19 N028 N015 N032 N032 NMOS
M20 N029 N033 N032 N032 NMOS
M21 vdd N028 N028 vdd PMOS
M22 vdd N028 N029 vdd PMOS
M23 N032 N031 0 0 NMOS
M24 vdd N029 N020 vdd PMOS
M25 N020 N031 0 0 NMOS
M26 N031 N031 0 0 NMOS
M27 vdd N031 N031 vdd PMOS
V5 N001 0 2
V6 N025 0 SINE(0 5 50)
V7 N033 0 SINE(0 5 50)
M50 vdd N003 N030 vdd PMOS
M51 vdd N020 N030 vdd PMOS
```

M52 vdd N030 A1 NC_01 PMOS

M53 N030 N020 N034 N034 NMOS

M54 N034 N003 0 0 NMOS

M55 A1 N030 0 0 NMOS

M1 N004 N002 N011 N011 NMOS

M2 N005 N013 N011 N011 NMOS

M3 vdd N004 N004 vdd PMOS

M4 vdd N004 N005 vdd PMOS

M5 N011 N007 0 0 NMOS

M6 vdd N005 N010 vdd PMOS

M7 N010 N007 0 0 NMOS

M8 N007 N007 0 0 NMOS

M9 vdd N007 N007 vdd PMOS

V3 N013 0 SINE(0 5 50)

M28 vdd N020 N023 vdd PMOS

M29 vdd N014 N023 vdd PMOS

M30 vdd N023 A0 NC_02 PMOS

M31 N023 N014 N027 N027 NMOS

M32 N027 N020 0 0 NMOS

M33 A0 N023 0 0 NMOS

M34 vdd N010 N006 vdd PMOS

M35 vdd N003 N006 vdd PMOS

M36 N006 N010 N008 N008 NMOS

M37 N008 N003 0 0 NMOS

M38 vdd N003 N017 vdd PMOS

M39 N017 N010 N026 N017 PMOS

M40 vdd N021 N012 vdd PMOS

M41 N026 N003 0 0 NMOS

M42 N026 N010 0 0 NMOS

M43 N012 N021 0 0 NMOS

M44 vdd N006 N014 NC_03 PMOS

```
M45 vdd N012 N014 NC_04 PMOS
M46 N014 N012 N016 NC_05 NMOS
M47 N016 N006 0 0 NMOS
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\hp\AppData\Local\LTspice\lib\cmp\standard.mos
.tran 100m
.backanno
.end
```

References

- Sanfoundry Article on Flash ADC - https://www.sanfoundry.com/flash-type-adc/#1
- Idc online Comparator Design - https://www.idc-online.com/technical_references/pdfs/electronic_engineering/2%20Bit%20Magnitude.pdf
- Architecture of 4 bit Flash ADC - https://jeffreyscomputer.github.io/pdfs/report_ADC.pdf
- Encoder Design using Gates - https://www.geeksforgeeks.org/digital-logic/encoder-in-digital-logic/
- Design and Analysis of Comparator - https://www.iject.org/vol72/25-neha.pdf