

# Experiment #4- Integrated System

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## 1-Integrated System

1.

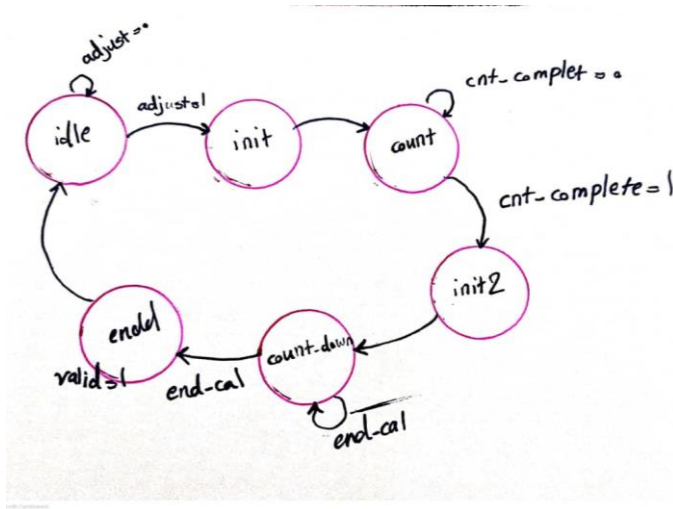


Fig1: state machine

2. testbench result in modelsim simulation software  
Input frequency = 100kHz



Fig2: n = 1 and frequency become 200 kHz

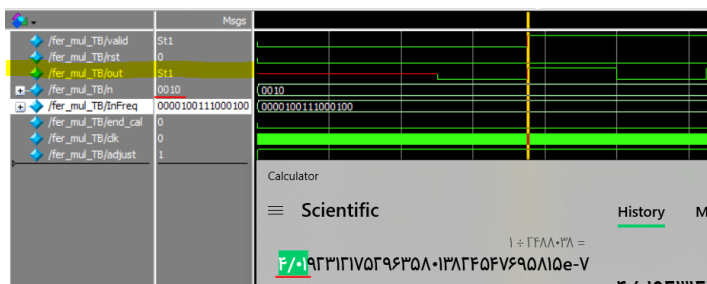


Fig3: n = 2 and frequency become 400 kHz

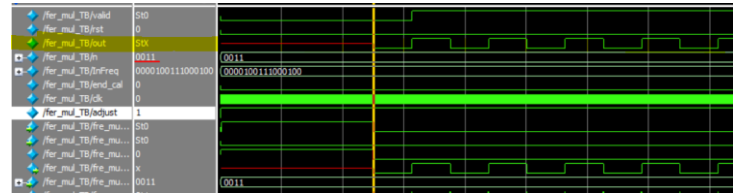
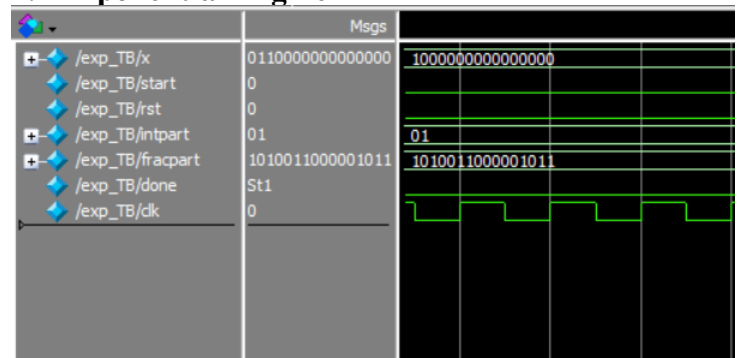


Fig 4: n = 3 and frequency become 800 kHz

## 2 Exponential Accelerator

### 2.1 Exponential Engine

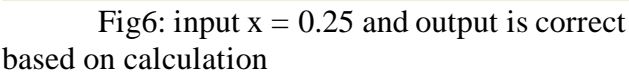


$$e^{0.5} = 1.6487212707001$$

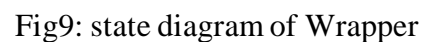
Enter decimal number

Binary number

Fig5: input x = 0.5 and output is correct based on calculation

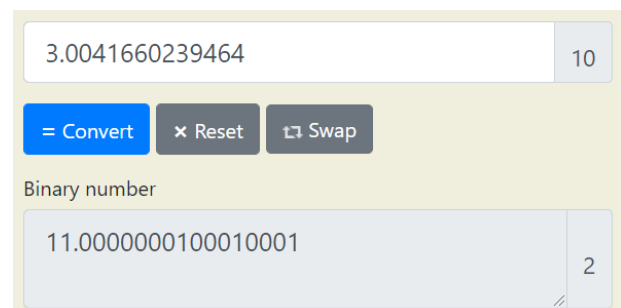


1-



4- Assume  $x = 1.1$

$$e^{1.1} = 3.0041660239464$$



$$e^{1.2} = 3.3201169227365$$

10

= Convert
✕ Reset
↔ Swap

Binary number

2

$$e^{1.4} = 4.0551999668447$$

10

= Convert
✕ Reset
↔ Swap

Binary number

2

$$e^{1.8} = 6.0496474644129$$

10

= Convert
✕ Reset
↔ Swap

Binary number

2

Fig11: expected value for n = 4





 [3]	0001000111001101010010	0001000111001101010010
 [2]	0000101111101110111100	0000101111101110111100
 [1]	0000100111000101001110	0000100111000101001110
 [0]	0000100011010111001110	0000100011010111001110

Fig12: achieved results.

- n = 0 → answer = 2.2
- n = 1 → answer = 2.4
- n = 2 → answer = 2.9
- n = 3 → answer = 4.22

It has difference with expected value because of approximation

Second example: x = 0.01

$$e^{0.08} = 1.083287067675$$

Enter binary number

2

= Convert
✕ Reset
↔ Swap

Decimal number

10

$$e^{0.04} = 1.0408107741924$$

Enter binary number

2

= Convert
✕ Reset
↔ Swap

Decimal number

10

$$e^{0.02} = 1.0202013400268$$

Enter binary number

2

= Convert
✕ Reset
↔ Swap

Decimal number

10

$$e^{0.01} = 1.0100501670842$$

Enter binary number

2

= Convert
✕ Reset
↔ Swap

Decimal number

10

Fig13: expected value for n = 4

Fig14: achieved results

$n = 0 \rightarrow \text{answer} = 1.009$

$n = 1 \rightarrow \text{answer} = 1.02$

$n = 2 \rightarrow \text{answer} = 1.04$

$n = 3 \rightarrow \text{answer} = 1.08$

6.

maximum frequency of this accelerator wrapper is 250MHz

### 3. Integrated Circuit

2-  $162 \cdot 10^6 / 200 \cdot 10^3 = 810 \rightarrow \lceil \log 810 \rceil = 9 \rightarrow n$  needs 4 bit

5-

The screenshot displays the 'Compilation Report - L04.q' window in Quartus II. The 'Summary' tab provides a high-level overview of the compilation process. It confirms that the compilation was successful on June 17, 2020, at 1:01 PM. The report details the utilization of resources: 251,048 logic elements (98.0% of the available 255,000), 28 registers (100% of 28), 28,000 flip-flops (9.0% of 300,000), and 0,210 I/O pins (2.0% of 10,500). The 'Flow Settings' section lists various configuration parameters such as flow, device, target device, and target family. The 'Task Messages' section shows a summary of the compilation tasks, including 'Compile Design', 'Analyze & Synthesize', 'Fit', 'Timing Analysis', and 'EDA Toolset Verification', all of which completed successfully.