Experiment #1-
Clock and Periodic Signal Generation

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1.1

1.10 ns

2. 2*N*$delay_{inverter}$ = 20ns

N = 5

$Delay_{inverter}$ = 2 ns

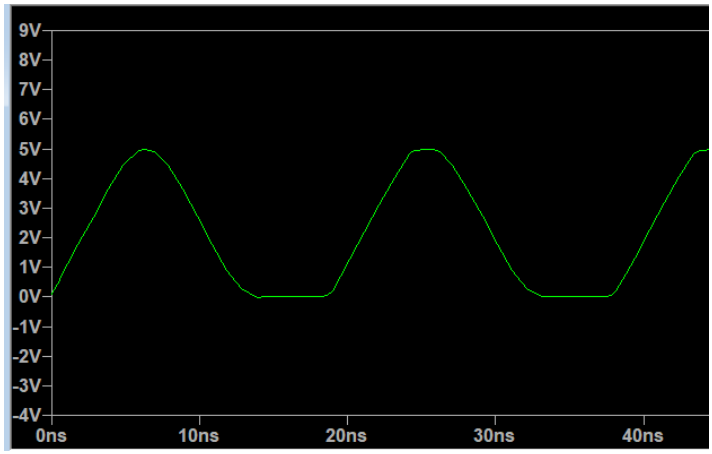


Fig. 1 delay of 5 inverter

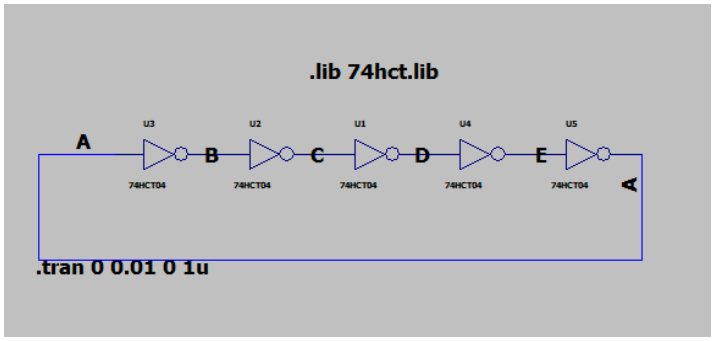
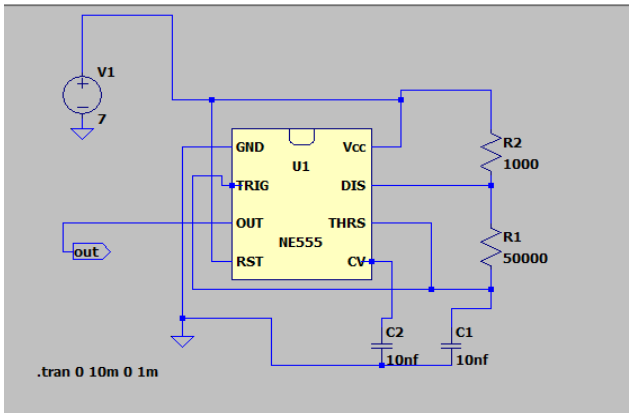


Fig. 2 ring oscillator in LTspice

1.2 LM555 timer



1-Fig. 3 LM555

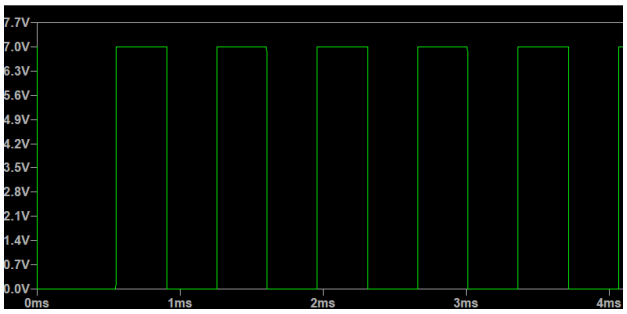


Fig. 4 waveform of the output

1-Clock frequency is: 0.693 ∗ (R1 + 2R2) ∗ C = 0.693*(101*10^3) *10*(10^ (-9)) = <u>0.69ms</u>

Duty cycle is:

(R1+R2)/(R1+2R2) = 51/101= <u>50.4%</u>

2-

If R_2 = 1kΩ:

Clock frequency is: 0.693 ∗ (R1 + 2R2) ∗ C = 0.693*(3*10^3) *10*(10 ^ (-9)) = <u>0.02079ms</u>

Duty cycle is:

(R1+R2)/(R1+2R2) = 2/3 = <u>66%</u>

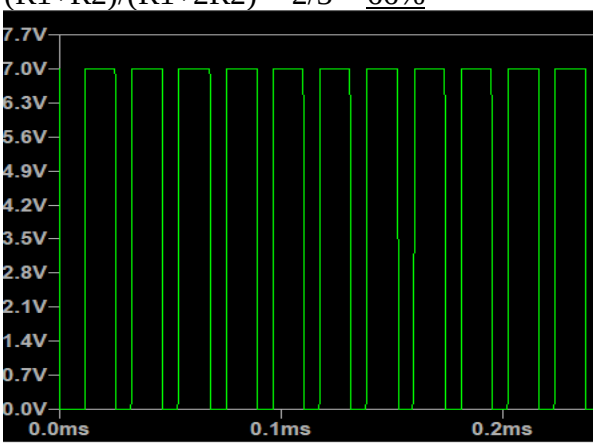


Fig. 5 When R_2 = 1kΩ

If R_2 = 10kΩ:
Clock frequency is: 0.693 ∗ (R1 + 2R2) ∗ C = 0.693*(21*10^3) *10*(10^ (-9)) = 0.14553 ms
Duty cycle is:
(R1+R2)/(R1+2R2) = 11/21= 52%

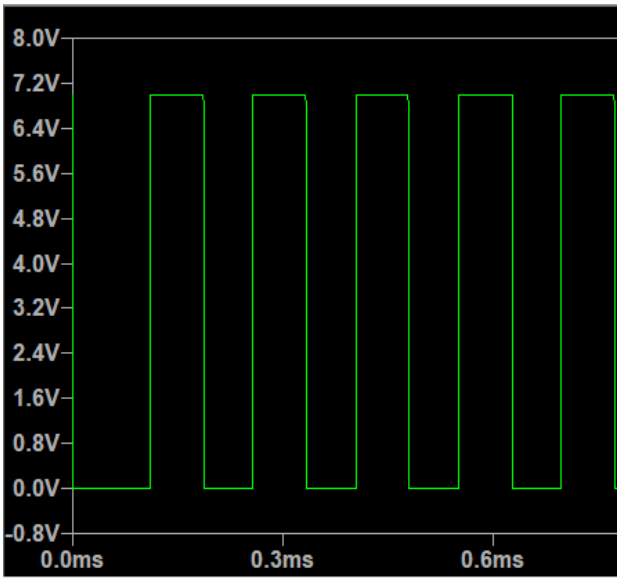


Fig. 6 When R_2 = 10kΩ

If R_2 = 100kΩ:
Clock frequency is: 0.693 ∗ (R1 + 2R2) ∗ C = 0.693*(201*10^3) *10*(10 ^ (-9)) = 1.39293ms
Duty cycle is:
(R1+R2)/(R1+2R2) = 51/201= 25%

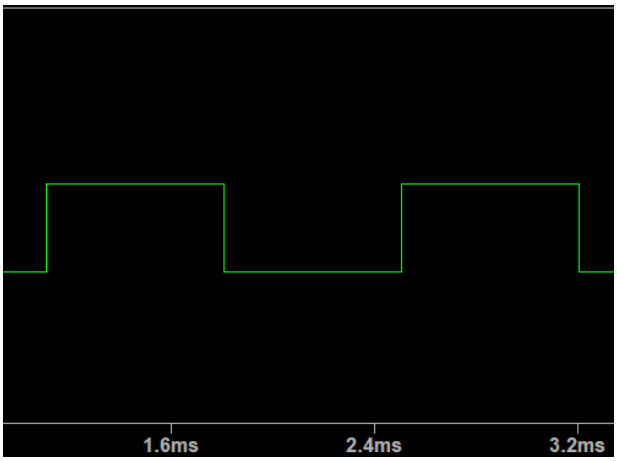


Fig. 7 When R_2 = 100kΩ

3.

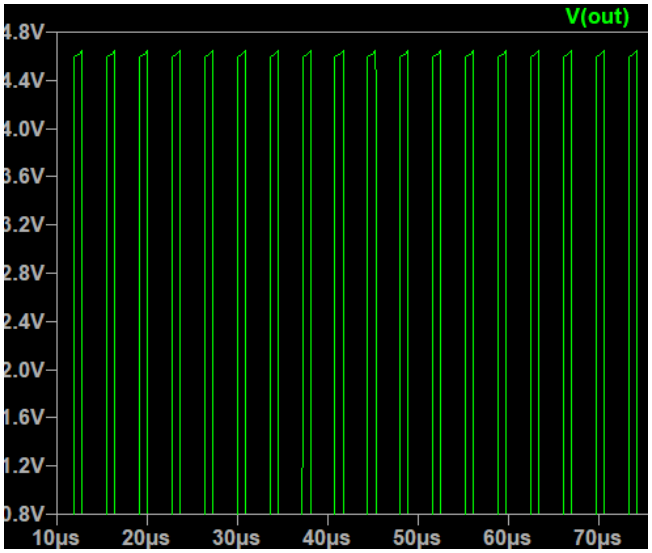


Fig. 8 When R = 470Ω

When R = 470Ω, T become 20/3 and f equal to 3/20, So a = 705*10^-9

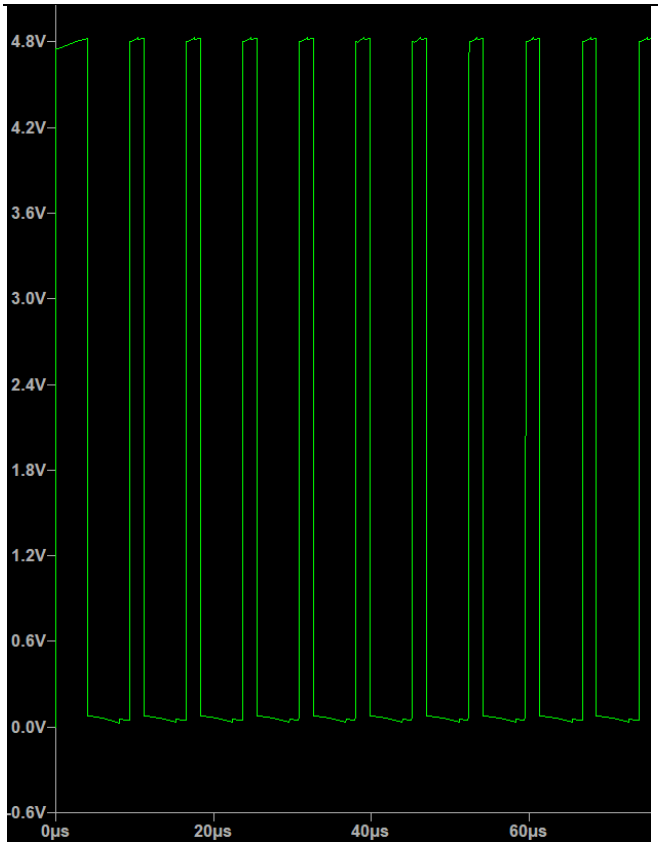


Fig. 9 When R = 1000 Ω

When R = 1000Ω, T become 60/8 and f equal to 2/15, So a = 2/15*10 ^ -5

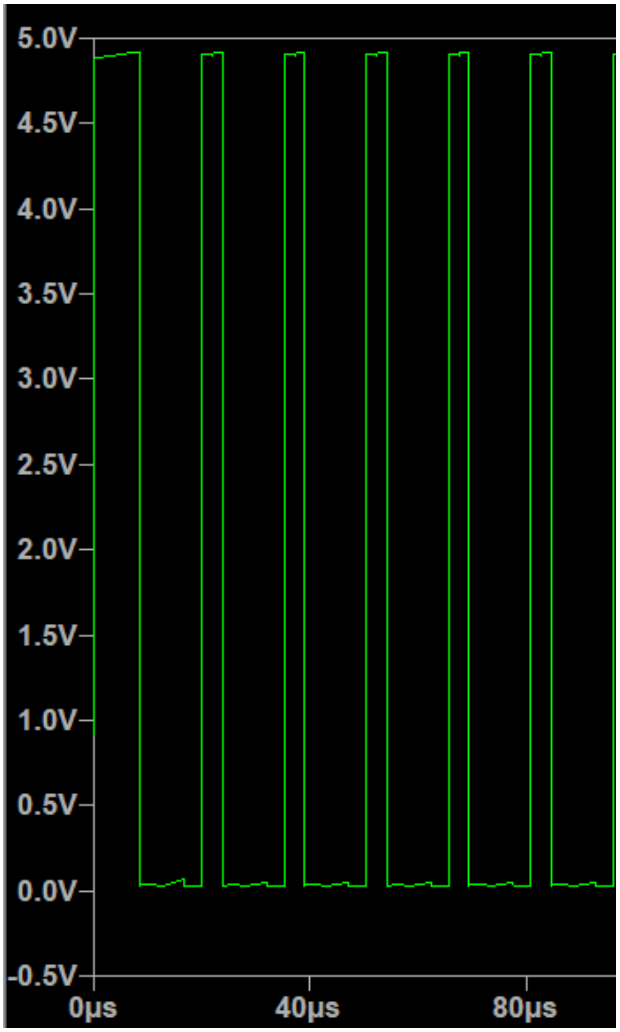


Fig. 10 When R = 2200 Ω

When R = 2200Ω, T become 16us and f equal to 1/16, So a = 1.375 * 10^(-6)

2. FPGA DESIGN

2.1.

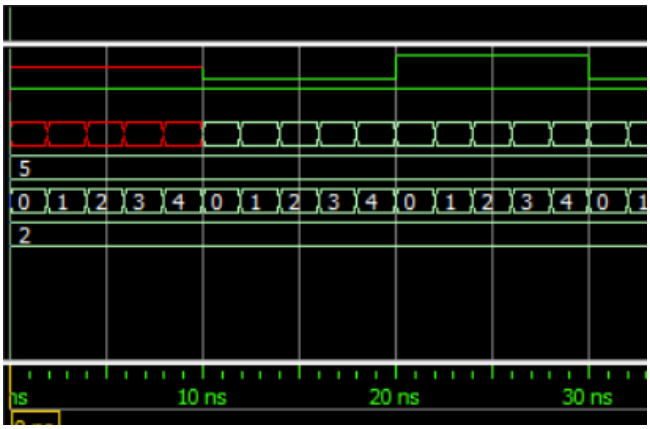


Fig. 11 waveform of 5 inverters

ring oscillator frequency = delay of inverter*2*N
= 2*5*delay = 20ns

2.2

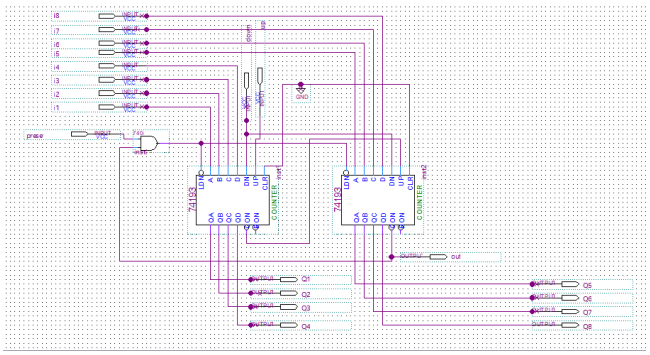


Fig. 12 frequency divider

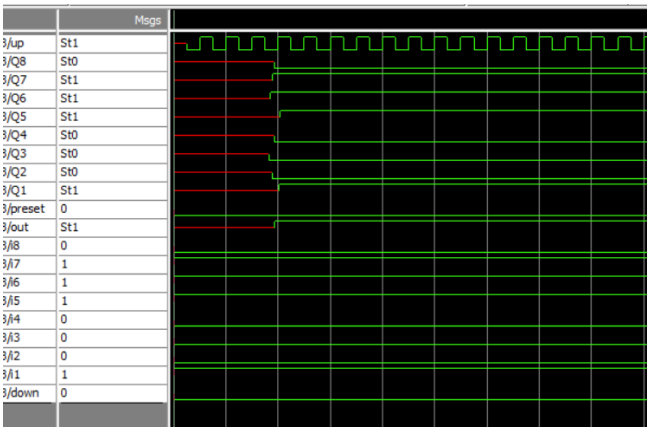


Fig. 13 output waveform.

Delay input of ring oscillator was 250ps so every 250ps the output is summed with one and frequency is 113*250 = 28.25ns

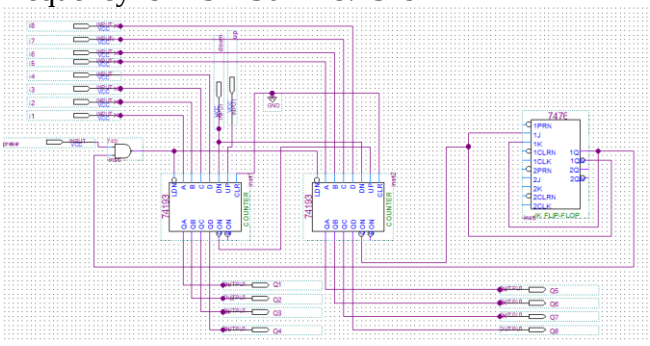


Fig. 14 circuit with T flip flop

3_
3.4-

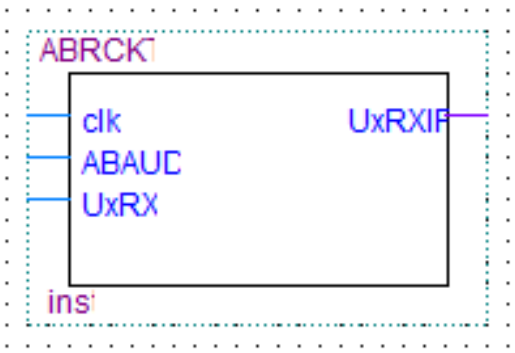


Fig. 15 schematic symbol for ABRCKT