Experiment #2-
Clock Adjusting and Monitoring

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1.Clock Adjusting Unit

1.1 Design and Synthesis:
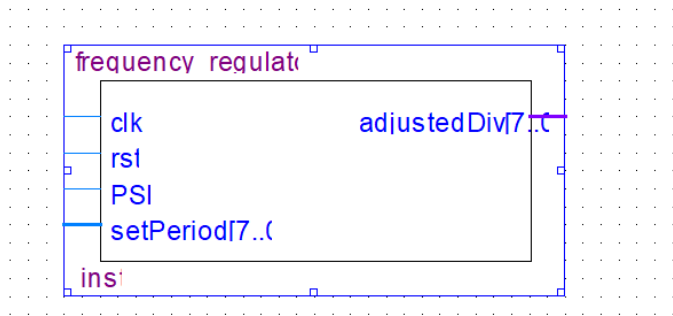
1.1.1:

Fig.1: symbol of Frequency Regulator
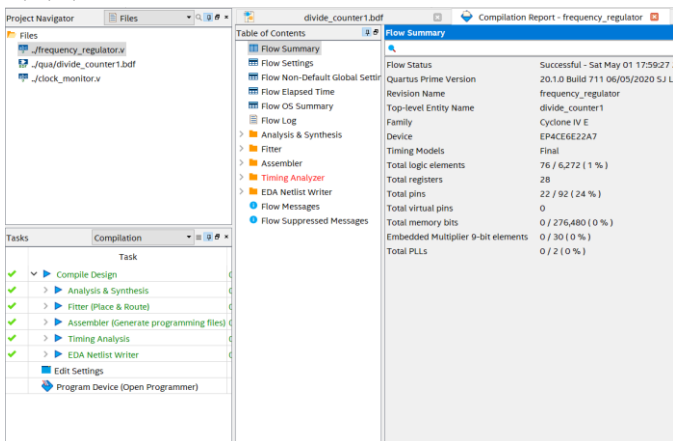
1.1.2:

Fig.2 : synthesis report

1.2: In below you can see two waves related to frequency regulator
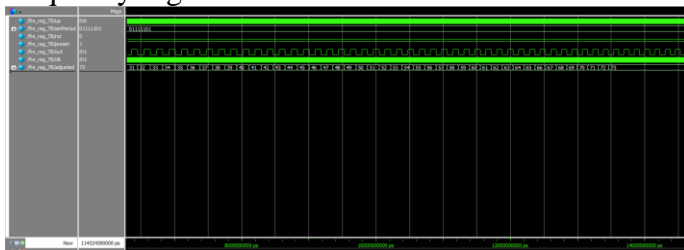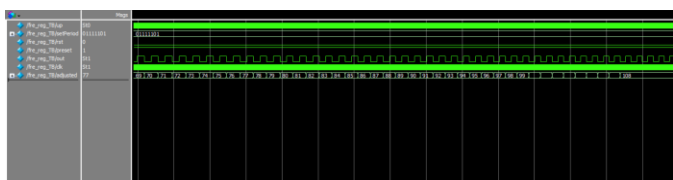

Fig2 : 19 MHz ring oscillator
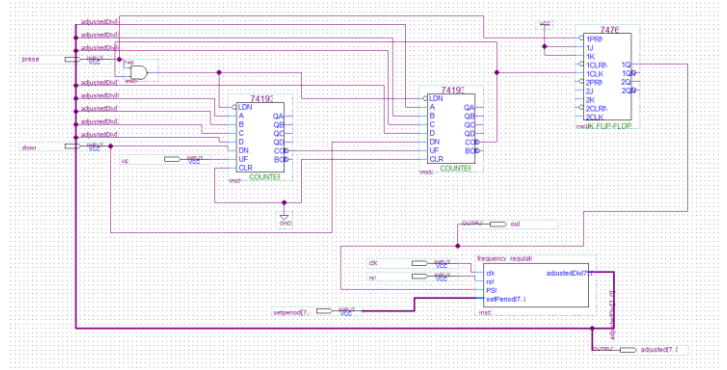

Fig2 : 23 MHz ring oscillator

Fig4: Frequency Divider Unit with Frequency divider
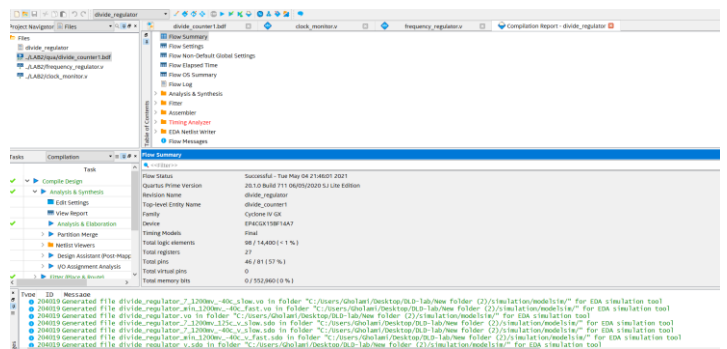
2. Clock Monitoring unit

2.1 Design and Synthesis

Fig5: synthesis report of Clock Monitoring unit

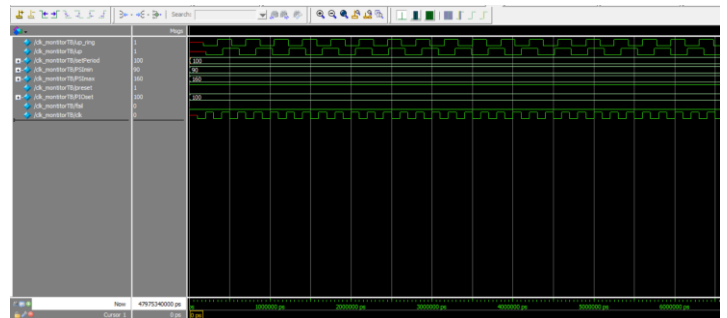### 2.2: Simulation in Model sim

Fig.6: Scenario 1

Fig8: fail flag

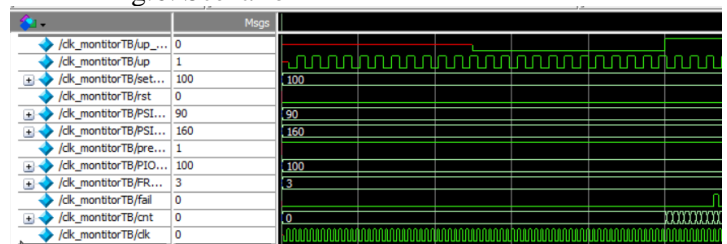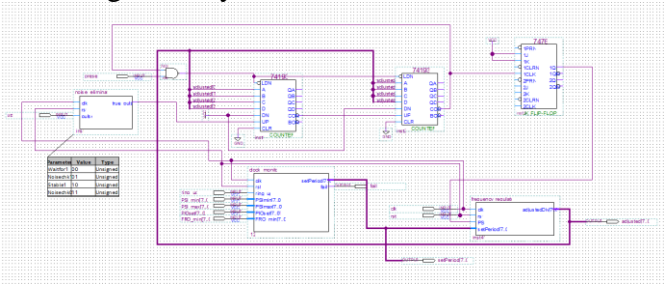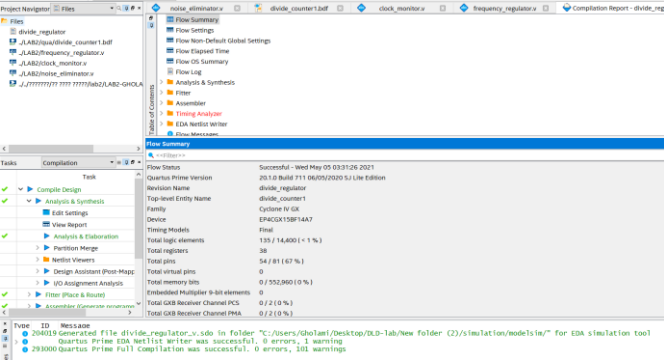# 3. Noise Eliminator unit

3.1 Design and Synthesis

Fig.7: total design

Fig8.Compile report for third part