Assignment on unit-IV

Short Answers

1) b) What is the importance of I/O interface?

* Input-Output interface provides a method for transferring information between internal Storage and external I/O devices

* Peripherals connected to a computer need Special communication links for interfacing them with the cpu.

* The purpose of the communication link is to resolve the differences that exists between the central computer and each peripherals

c) Classify modes of Data-transfer

Data Transfer between the central computer and I/O devices may be handled in one of these three modes

1. programmed I/O
2. Interrupt-driven I/O
3. Direct Memory Access

e) Distinguish Isolated and memory mapped I/O

As cpu needs to communicate with the various memory and input-output devices.

These are two approaches for communicating

1. Isolated I/O
2. Memory mapped I/O

Isolated I/O	Memory mapped I/O
→ Memory and I/O have seperate address space	→ Both have same address space.
→ Dataline, address lines are same for both cpu and I/O	→ Datalines, address line, control line (read, write) same for both.
→ More efficient due to seperate buses	→ less efficient
→ larger in size due to more buses	→ smaller in size

Long Answers

2) a) Describe functionality of static RAM and Dynamic RAM

SRAM:-

→ Data is stored in transistors and requires a constant power flow.

→ Because of continuous power, SRAM doesn't need to be refreshed to remember the data being stored.

→ SRAM is called static as no change (or) action

Advantage:-

Low power consumption and faster access speeds.

Disadvantage:-

Less memory capacity and high costs of manufacturing

DRAM:-

→ Data is stored in capacitors

→ capacitors that store data in DRAM gradually discharge energy no energy means the data has been lost.

→ So a periodic refresh of power is required in order to function.

→ DRAM is called dynamic as constant charge(or) actions.

Advantage:-

Low costs of manufacturing and great memory capacities.

Disadvantage:-

Slow access speed and high power consumption.

2) b) What is the problem with programmed I/O? Explain alternate for it

→ In programmed I/O the transfer is to and from a CPU register and Peripheral

→ The I/O device, transfer bytes of data one at a time as they are available.

→ when a byte of data is available, the device place it in the I/O bus and enables the data valid line and accepted line enable.

→ At that time, the interface sets flag register bit F=1

→ Now the device can disable the valid line, but it will not transfer another byte until the data accepted line is disabled by interface. This is the main problem.

The alternate for it is Interrupt driven I/O

→ This technique is used to overcome the limitations of programmed I/O.

→ In Interrupt driven I/O, instead of making the processor to verify the status of I/O module. It is the responsibility to intimate the processor by interrupt signal.

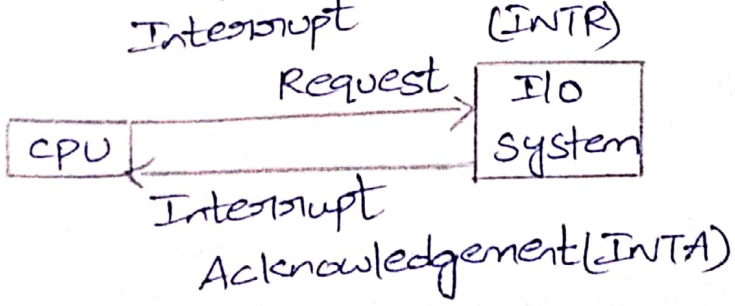
→ CPU responds to interrupt signals and stores the return address from the program counter into the memory stack and the control branches to a interrupt service Routine (ISR)

→ ISR processes the required I/O transfer.

→ After completion of executing Interrupt routine, CPU returns to previous program and continue what it was doing before.

* Interrupt:-

An interrupt (or) exception causes CPU to transfer the control temporarily to the current program to another program.



5) a) Describe virtual memory address translation method on the concept of fixed length page with a neat diagram.

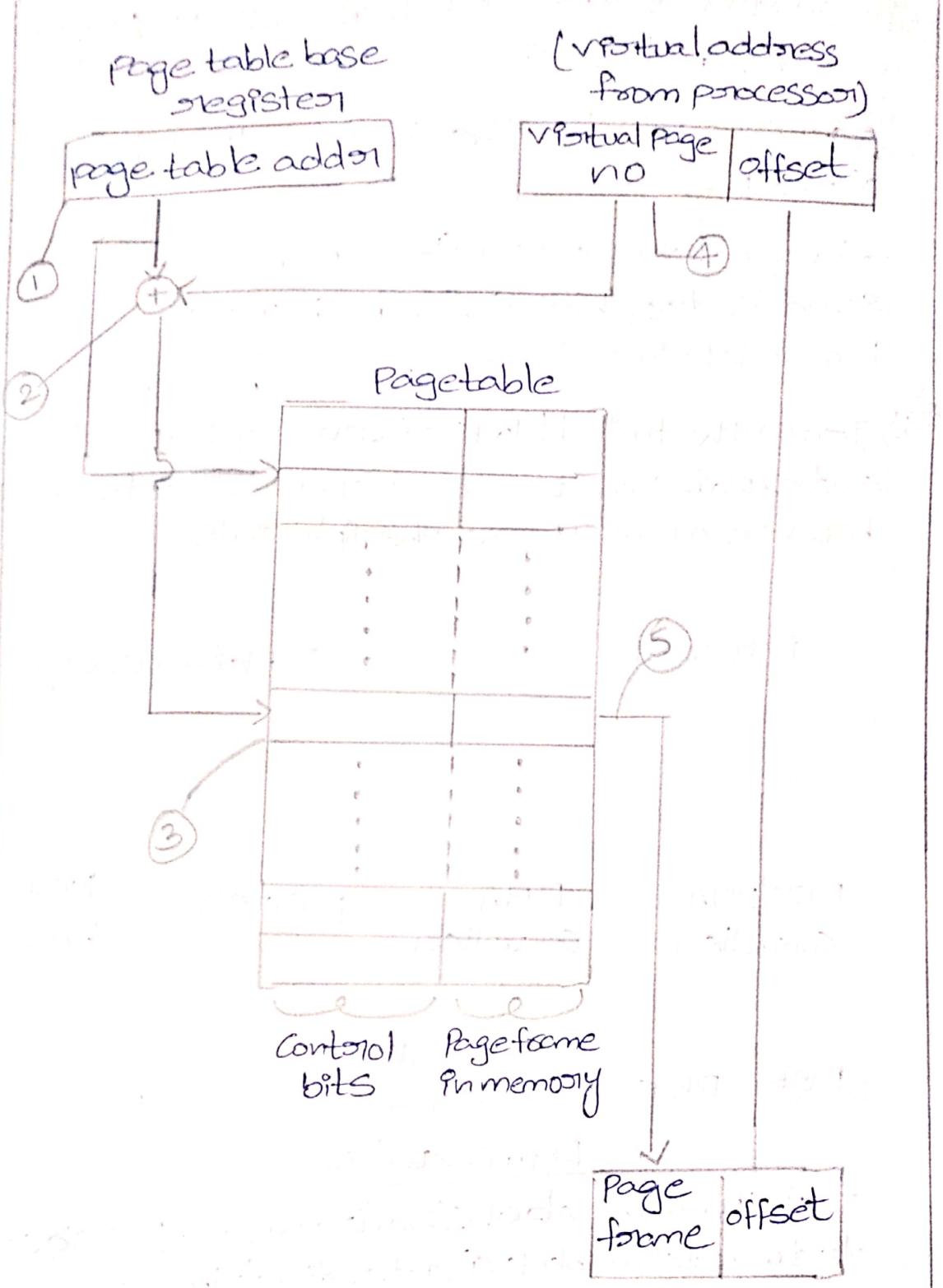
→ the virtual memory mechanism bridges the size and speed gaps between the main memory and secondary storage.

→ Assume that data and program are composed of fixed length units called pages.

→ A page contains a block of words that occupy contiguous locations in the main memory

→ A page is a basic unit of info that is transferred between main memory and secondary storage.

→ size of page commonly ranges from 2K to 16K bytes.



Address translation:-

(1) PTBR holds the address of the page table.

(2) PTBR + virtual page no. provides the entry of the page table.

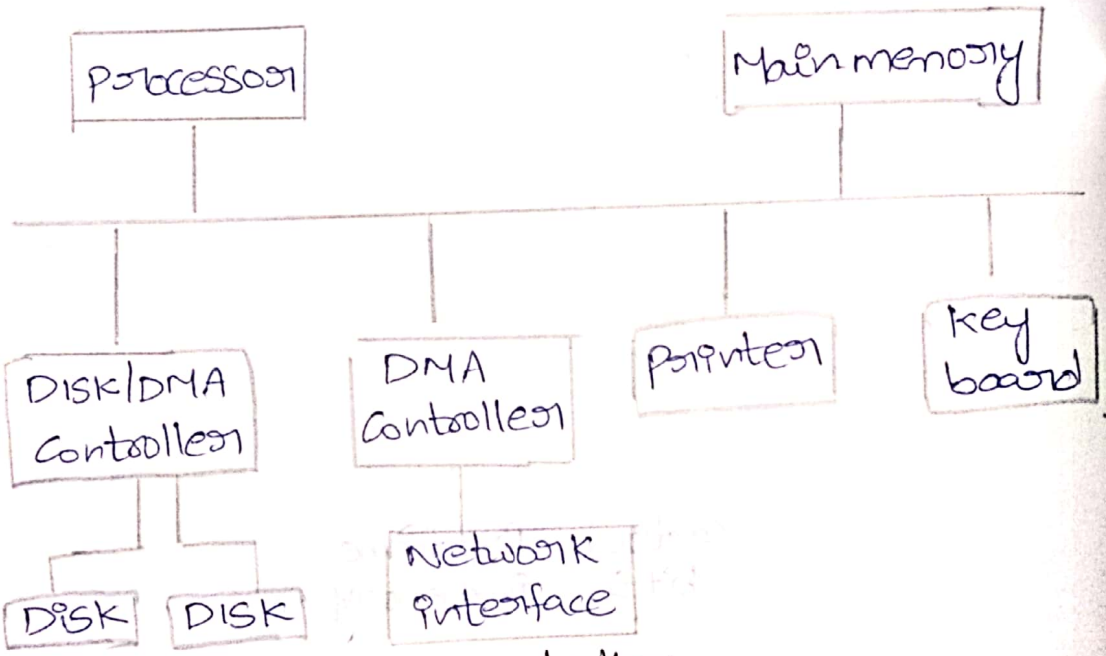
(3) Page table holds info about each page. This includes starting address of the page in main memory.

④ Virtual address is interpreted as Page number and offset

⑤ This entry has the starting location of the page.

→ Page table entry for a page also includes some control bits which indicates places of Page while it is in main memory.

5)b) Draw the typical block diagram of DMA Controller and explain how it is used for direct data transfer between memory and peripherals.



DMA controller

→ A special control circuit may be provided to transfer a block of data directly between I/O devices and the main memory without continuous intervention by the processor.

→ However, the operation of the DMA controller Unit must be under the control of a program executed by the processor. i.e: the processor must initiate the DMA transfer.

→ DMA controller connects a high speed network to the computer bus.

→ DMA controller connects two disks also has a DMA capability. It provides two DMA channel

→ DMA controller transfer the data block at a faster rate of data is directly accessed by I/O devices and is not required to pass through the processor which saves the clock cycles (time).