



Srinivasa Ramanujan Institute of Technology (AUTONOMOUS)

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II B. Tech II Sem – Semester End Examinations – Supplementary – Jun 2022

Subject Name: Computer Organization

Subject Code: 194GA05404

Name & Signature of the Examiner: M. Narasimhulu,

AY: 2021-22

Scheme of Evaluation

SRIT R19

PART-A

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|-----|--|----|
| 1a) | Types of Computers: Personal Computer, Workstation, MainFrames, Servers, Super Computers | 2M |
| 1b) | Any two differences between multi-computer and Multi-Processor | 2M |
| 1c) | Fetch, Decode, Operand-Evaluation, Execute and Store the result. | 2M |
| 1d) | An interrupt in computer architecture is a signal that requests the processor to suspend its current execution and service the occurred interrupt. To service the interrupt the processor executes the corresponding interrupt service routine (ISR). After the execution of the interrupt service routine, the processor resumes the execution of the suspended program. Interrupts can be of two types of hardware interrupts and software interrupts. | 2M |
| 1e) | The Register Transfer Language is the symbolic representation of notations used to specify the sequence of micro-operations. | 2M |
| 1f) | Control Memory is the storage in the microprogrammed control unit to store the microprogram. | 2M |
| 1g) | ROM, PROM, EPROM, EEPROM specifying these types. | 2M |
| 1h) | Addresses that are used by programmers are known as virtual addresses, and the set of such addresses is known as the address space. Space or spot where the address is saved in the main memory is referred to as location or physical address and the set of such locations is known as the memory space. | |
| 1i) | Single bus, Cross Bar Switches, Multi-Stage Networks, Hyper-Cube Networks, Mesh Networks, Tree Networks. | 2M |
| 1j) | Pipelining is a process of arrangement of hardware elements of the CPU such that its overall performance is increased. Simultaneous execution of more than one instruction takes place in a pipelined processor. | 2M |

PART-B

UNIT-1

- | | | |
|-----|---|----|
| 2a) | Classification of number systems(1M)
Explanation of each number system(2M) with Example (2M) | 5M |
| 2b) | Show Flow Chart of Division Algorithm(3M)
Implement it with A=01110 and B= 10001(2M) | 5M |

OR

- | | | |
|-----|---|----|
| 3a) | Specify 256 in BCD, Signed Magitute, 2's Complement and Hexa Decimal code. | 5M |
| 3b) | Addition and Subraction algorithm for signed Magnitude and signed 2's Complement (3M) | 5M |

4a) **BUN: (2M)**

5M

The Branch Unconditionally (BUN) instruction can send the instruction that is determined by the effective address. They understand that the address of the next instruction to be performed is held by the PC and it should be incremented by one to receive the address of the next instruction in the sequence. If the control needs to implement multiple instructions that are not next in the sequence, it can execute the BUN instruction.

BSA: (2M)

BSA stands for Branch and Save return Address. These instructions can branch a part of the program (known as subroutine or procedure). When this instruction is performed, BSA will store the address of the next instruction from the PC into a memory location that is determined by the effective address.

ADD: (1M)

The ADD instruction adds the content of the memory word that is denoted by the effective address to the value of the register.

4b)

5M

RISC	CISC
It is a Reduced Instruction Set Computer.	It is a Complex Instruction Set Computer.
It emphasizes on software to optimize the instruction set.	It emphasizes on hardware to optimize the instruction set.
It is a hard wired unit of programming in the RISC Processor.	Microprogramming unit in CISC Processor.
It requires multiple register sets to store the instruction.	It requires a single register set to store the instruction.
RISC has simple decoding of instruction.	CISC has complex decoding of instruction.
Uses of the pipeline are simple in RISC.	Uses of the pipeline are difficult in CISC.
It uses a limited number of instruction that requires less time to execute the instructions.	It uses a large number of instruction that requires more time to execute the instructions.
It uses LOAD and STORE that are independent instructions in the register-to-register a program's interaction.	It uses LOAD and STORE instruction in the memory-to-memory interaction of a program.
RISC has more transistors on memory registers.	CISC has transistors to store complex instructions.
Any 5 Differences	Any 5 Differences

OR

5a) T0: AR \leftarrow PC

5M

T1: IR \leftarrow M[AR], PC \leftarrow PC + 1

T2: D0, ..., D7 ← Decode IR(12-14), AR ← IR(0-11), I ← IR(15)

5b) Explanation about Arithmetic, Logical, and shift instructions 5M

UNIT-3

6a) Mention the block diagram with explanation 5M

6b) 4-bit adder diagram + Explanation about working principle(3M) 5M
Binary Adder-Subtractor diagram + Working Principle Explanation (2M)

(OR)

7a) Bus transfer diagram with four registers(2M) + State Table (2M) + Explanation (1M) 5M

7b) Explanation about Selective Set, Selective Complement, Selective Clear and Mask with suitable example. 5M

UNIT-4

8a) Memory Hierarchy Diagram+ Explanation about each role in the hierarchy. 5M

8b) Specifying diagrams of mapping 1) Associative mapping cache ii) Direct mapping cache iii) Block-set-associative mapping cache. (4M) + Explanation (1M) 5M

(OR)

9a) Programmed IO: CPU waits for several clock cycles before input and output available. Which leads to CPU utilization is zero. Alternative is Interrupt Driven IO. (2M) 5M

DMA Block Diagram (2M) + Explanation (1M)

9b) Interrupt Driven IO Flow Chart + Explanation (3+2) 5M

UNIT-5

10a) Arithmetic Pipeline will improve the performance of the system during calculation(1M) 5M
Pipe Line diagram for Addition and Subtraction (3M) + Explanation(1M)

10b) Need of Pipeline like improving execution in number of instruction during a particular amount of time(1M) 5M
Addition and Subtraction Pipeline Diagram(2M).
Working Principle of Pipeline Diagram(2M)

(OR)

11a) Definition of Vector (1M) + Vector Processing Explanation with suitable Diagram(4M) 5M

11b) Six-Segment Pipeline Diagram for Eight Tasks (3M) + Calculating and Specifying Execution Time (2M) 5M