Hall Ticket No.: | | | | | | | | | | |

**SRIT R19**

**SRINIVASA RAMANUJAN INSTITUTE OF TECHNOLOGY**
**(AUTONOMOUS)**
II B. Tech II Sem – Semester End Examinations – Supplementary – Feb 2023
**COMPUTER ORGANIZATION**
**[194GA05404]**
(Computer Science & Engineering)

**Time: 3 hours** **Max. Marks: 70**

## PART-A
(Compulsory Question)
***

1 Answer the following: (10 X 02 = 20 Marks)
- a) What is a memory unit?
- b) What are zero address instructions? Explain with the help of an example.
- c) Perform the arithmetic operation in binary using 2's complement representation. (i) (+42) + (-13) and (ii) (-42) – (-13).
- d) What are the four basic types of operations that need to be supported by an Instruction set?
- e) What are the symbols used for register transfer language?
- f) Define control memory.
- g) Define virtual memory.
- h) Compare PROM and EPROM.
- i) What is pipelining?
- j) Show the two approaches to bus arbitration.

## PART-B
(Answer all five units, 5 X 10 = 50 Marks)

### UNIT-1
2 a) What are the various ways of representing negative numbers? Explain with example. **[5M]**
b) Explain the different functional units of a computer. **[5M]**

(OR)

3 a) Distinguish between Fixed point and Floating point representation of a given number. **[5M]**
b) Explain Multiplication and Division algorithms. **[5M]**

### UNIT-2
4 a) Explain the purpose of registers available in basic computer. **[5M]**
b) Differentiate Direct, Indirect and Register addressing modes. **[5M]**

(OR)

5 a) Explain Data Transfer and Manipulation Instructions with examples. **[5M]**
b) Discuss about CISC processors. **[5M]**

### UNIT-3
6 a) Compare Hardwired and Microprogrammed control unit. **[5M]**
b) Draw bus and memory transfer for a 4X1 multiplexer. **[5M]**

(OR)

7 a) Explain arithmetic logical unit with a state table. **[5M]**
b) Discuss the Microprogram with an example. **[5M]**

### UNIT-4
8 a) What are Semiconductor Memories? Explain in detail. **[5M]**
b) Explain DMA with suitable diagram. **[5M]**

(OR)

9 a) Explain Programmed I/O in detail. **[5M]**
b) Describe the importance of memory hierarchy with a diagram. **[5M]**

**UNIT-5**

| | | | |
|---|---|---|---|
| 10 | a) | Explain arithmetic pipelining with a neat sketch. | **[5M]** |
| | b) | Describe Interprocess arbitration system in detail. | **[5M]** |

(OR)

| | | | |
|---|---|---|---|
| 11 | a) | Explain Interconnection Structure with an example. | **[5M]** |
| | b) | Illustrate RISC pipeline vector processing. | **[5M]** |

*****