DesHall Ticket No.: | | | | | | | | | | |

SRIT R19

SRINIVASA RAMANUJAN INSTITUTE OF TECHNOLOGY

(AUTONOMOUS)

II B. Tech II Sem – Semester End Examinations – Supplementary – Jun 2022

COMPUTER ORGANIZATION

[194GA05404]

(Computer Science & Engineering)

Time: 3 hours **Max. Marks: 70**

PART-A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

a) What are the different types of computers?
b) Differentiate Multiprocessor and Multicomputer.
c) Classify phases of an Instruction Cycle.
d) Define interrupt.
e) What is meant by RTL?
f) What is meant by control memory?
g) Classify types of ROM.
h) What is address space and memory space?
i) Classify interconnection structures.
j) Define pipelining.

PART-B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT-1

2 a) Explain various number systems and number representations used in system. **[5M]**

b) Dividend A=01110 Divisor B=10001. Explain flowchart for divide operation. **[5M]**

(OR)

3 a) Convert the $(256)_{10}$ into following codes **[5M]**

i) Binary Coded Decimal (BCD) ii) Signed magnitude
iii) Signed 2's complement iv) Hexa Decimal Code

b) Explain addition and subtraction algorithms for data represented in signed magnitude and signed 2's complement. **[5M]**

UNIT-2

4 a) Describe the purpose of the following Instructions with one example for each **[5M]**

i) BUN ii) BSA and iii) ADD

b) Distinguish the characteristics of CISC and RISC. **[5M]**

(OR)

5 a) Write register transfers statements for the fetch phase. **[5M]**

b) What are the three types of data manipulation instructions? **[5M]**

UNIT-3

6 a) Show the block diagram of hardware that implements the following register transfer statements: **[5M]**

$T2=R2 \leftarrow R1$, $R1 \leftarrow R2$

b) Explain the following with neat sketches i) 4 bit Binary adder ii) Binary Adder – Subtractor. **[5M]**

(OR)

7	a)	Design Bus System for four registers and briefly explain register transfer.	**[5M]**
	b)	Explain the following with respect to logic micro operations. i) Selective Set ii) Selective Complement iii) Selective Clear iv) Mask	**[5M]**

UNIT-4

8	a)	Explain the role of memory hierarchy in Computer Organization	**[5M]**
	b)	Explain the following mapping techniques used for cache mapping i) Associative mapping cache ii) Direct mapping cache iii) Block-set-associative mapping cache.	**[5M]**
		(OR)	
9	a)	What is the problem with programmed I/O? Explain the alternate for it. Also using block diagram explain DMA data transfer.	**[5M]**
	b)	Illustrate interrupt driven IO in Computer Organization.	**[5M]**

UNIT-5

10	a)	Identify the need for Arithmetic Pipeline and draw the pipeline for addition and subtraction.	**[5M]**
	b)	Identify the sequential steps involved in instruction pipe line and draw four-segment CPU pipeline.	**[5M]**
		(OR)	
11	a)	Explain Vector processing with example.	**[5M]**
	b)	Draw a space-time diagram for a six segment pipeline showing the time it takes to process eight tasks.	**[5M]**

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