



5 Schematics and Placement

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01_Revision_History.SchDoc

Rev.	Rel.	Date	Author	Description	Page(s)
V2.0		06/2020	H.D.	First new design for TC3xx	

AURIX™ Lite Kit V2

[No Variations]

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Variant	[No Variations]	Approved <Appr.:	
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A3	01_Revision_History.SchDoc	H.D.	V2.0
Author: H.D.		SVN Revision: Not in version control	
Date: 16.10.2020 Time: 13:15:09		© Infineon Technologies AG 2020. All Rights Reserved.	
		Sheet 1	of 5

Figure 8 Schematic: Project Overview

02_OCDS.SchDoc

OCDS

LEDs of OCDS

Signal Network Switches

USB Connector

FT232RL

DUAL HIGH SPEED USB UART / FIFO IC

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Size: A3

Document Name: 02_OCDS.SchDoc

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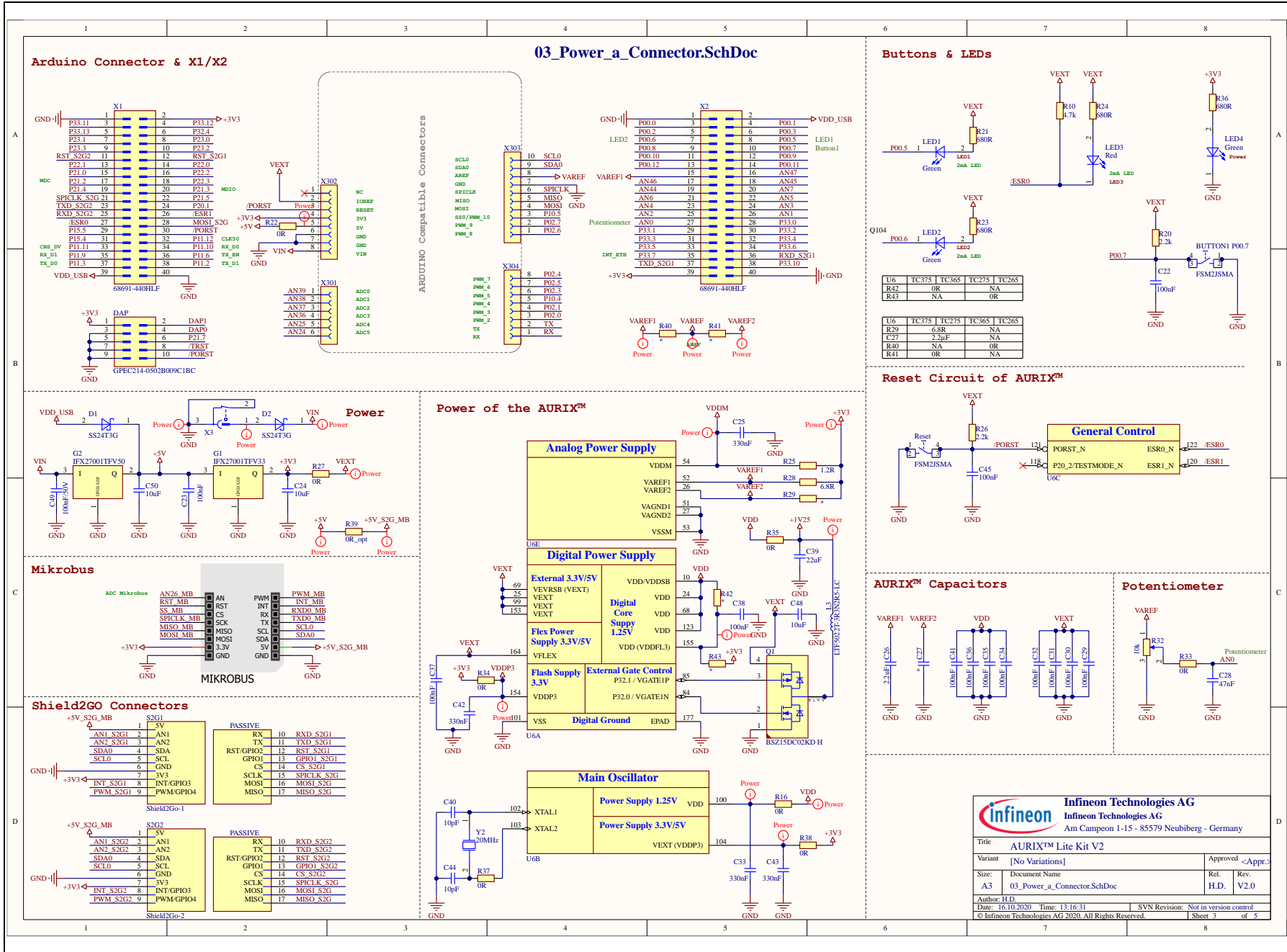
Sheet 2 of 5

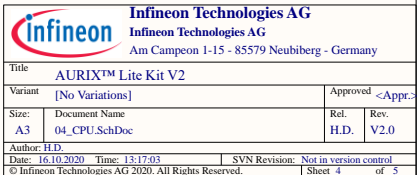
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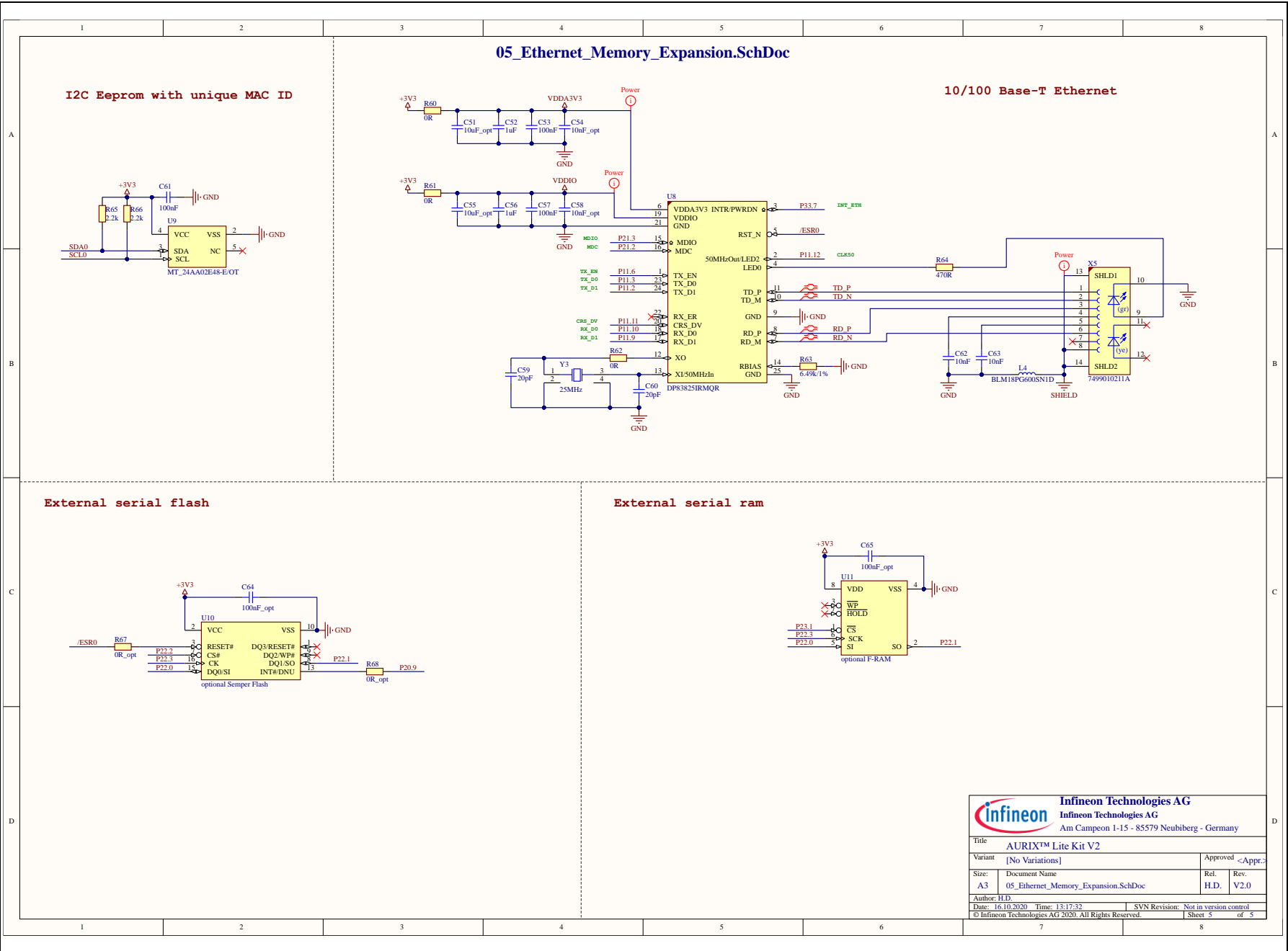
Rel. H.D.

Rev. V2.0

Figure 10 Schematic: Power and Connectors








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Title AURIX™ Lite Kit V2			
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Author: H.D.			
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Figure 12 Schematic: Ethernet and memory expansion

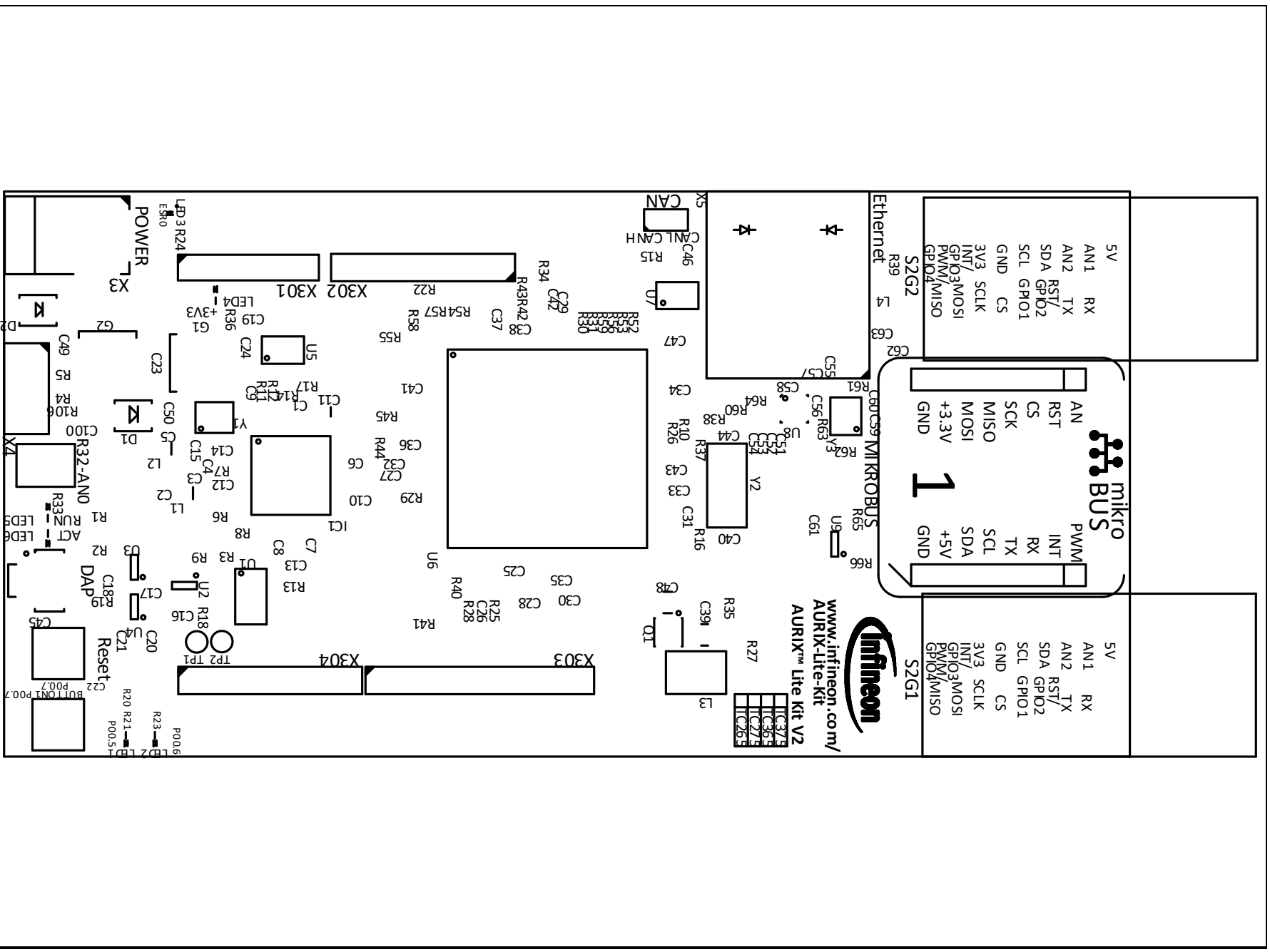
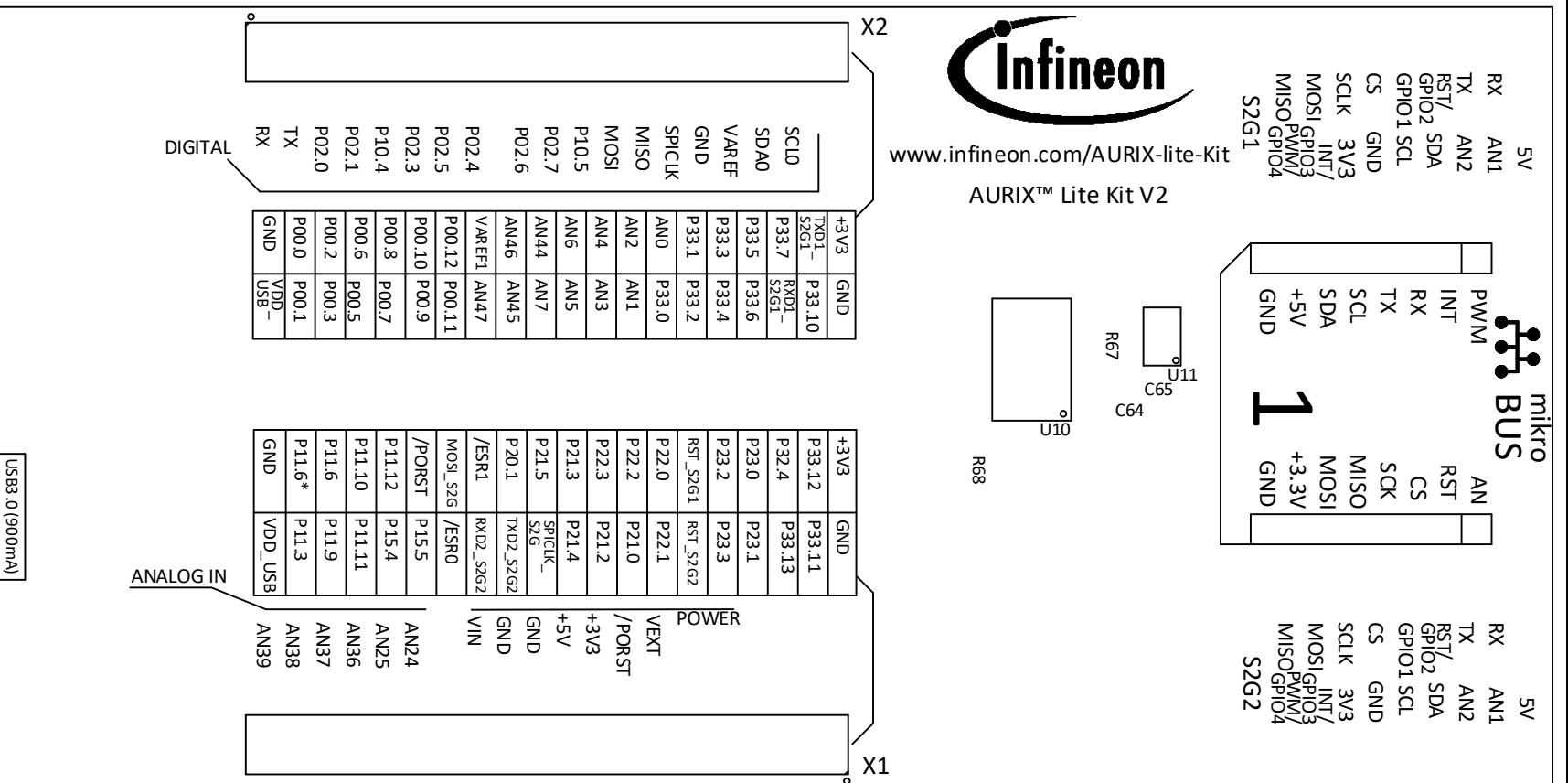


Figure 13 Placement: Top View



* Can be printed wrongly as P11.6, correct is P11.2

USB3.0 (900mA)

Figure 14 Placement: Bottom View