DIGITAL ELECTRONICS

TUTORIAL SHEET-1

1. Simplify using Boolean Algebra: A+B(C'+DE)'
2. Simplify the following expression: F= (X'+Y)(X+Y+Z)z'
3. Express x+yz as the sum of minterms
4. Find the value of X = A B C (A+D) if A=0; B=1; C=1 and D=1
5. Find the complement of x+yz
6. How will you use a 4 input NAND gate as a 2 input NAND gate?
7. Prove that (x1+x2).(x1'. x3'+x3) (x2' + x1.x3) =x1'x2
8. Show that the NAND gate is a universal building block
9. Using a K-Map, Simplify F= m (0-3, 12-15) + d (7, 11)
10. Simplify using K-map to obtain a minimum POS expression:

(A' + B'+C+D) (A+B'+C+D) (A+B+C+D')(A+B+C'+D') (A'+B+C'+D') (A+B+C'+D)

11. using a K-Map, Simplify F= m(0,4,8,12,3,7,11,15) + d(5)
12. Determine minimal SOP form

F(a,b,c,d) =_(0,2,4,6,8) + _d(10,11,12,13,14,15)

13. Find the SOP representation for

F(A,B,C,D,E) = m(1,4,6,10,20,22,24,26) + d (0,11,16,27) using K-Map method

14. Minimize using K-Map Y= M(3,5,8,9,10,14,15).d(0,1,2,10)
15. Minimize using K-Map Y= M(0,3,6,7,8,9).d(2,4,10,11,12,13,14)

TUTORIAL SHEET-2

1. Design the combinational circuit with 3 inputs and 1 output. The output is 1 when the binary value of the inputs is less than 3.The output is 0 otherwise.
2. Design a combinational circuit with 4 inputs and 1 output. The output is 1 iff input is even number.
3. What is a decoder and obtain the relation between the number of inputs ‘n’ and Outputs ‘m’ of a decoder? Distinguish between a decoder and a demultiplexer
4. What is multiplexer? Draw the logic diagram of 8 to 1 line multiplexer MUX
5. Implement the switching function F= _(0,1,3,4,7) using a 4 input MUX and explain
6. Explain how will build a 64 input MUX using nine 8 input MUXs
7. Implement the switching function F= m(0,1,3,4,12,14,15) using an 8 input MUX
8. Explain how will build a 16 input MUX using only 4 input MUXs
9. Implement the following using 3:8 line decoder:

S(A,B,C) = ∑ m(1,2,4,7)

C(A,B,C) = ∑m(3,5,6,7)

10. How many select lines are there for 30:1 Mux.
11. Design a full subtractor using one 3:8 decoder.
12. Design a 4 bit magnitude comparator to compare two 4 bit number

TUTORIAL SHEET-3

1. Find the hexadecimal equivalent of the decimal number 256
2. Find the octal equivalent of the decimal number 64
3. What is meant by weighted and non-weighted coding?
4. Convert A3BH and 2F3H into binary and octal respectively
5. Find the decimal equivalent of $(123)_9$
6. Find the octal equivalent of the hexadecimal number AB.CD
7. Find the hexadecimal equivalent of the octal number 153.4
8. Find the decimal equivalent of $(346)_7$
9. Convert the decimal number 214 to hexadecimal
10. how that the Excess – 3 code is self -complementing
11. Convert 231.3 4 to base 7
12. Encode the ten decimal digits in the 2 out of 5 code
13. Show that the Excess – 3 code is self –complementing
14. Explain how you will construct an (n+1) bit Gray code from an n bit Gray code
15. Construct a combinational circuit to convert given binary coded decimal number into an Excess 3 code for example when the input to the gate is 0110 then the circuit should generate output as 1001
16. How many parity bits are required to form Hamming code if message bits are 6?
17. How to find the location of parity bits in the Hamming code?
18. Generate the even parity Hamming codes for the following binary data 1101, 1001

TUTORIAL 4

Discuss Quiz 1

TUTORIAL SHEET-5

1. How many flip flops are required to count 16 clock pulses?
2. Give differences between latch and flip flops.
3. Give the excitation table of JK, T and D flip flop.
4. How synchronous counters differ from asynchronous counters?
5. What is race round condition? How can it be avoided?
6. Define Master slave flip flop
7. What is the primary disadvantage of an asynchronous counter?
8. Design a synchronous counter using T-flip flop to count the states : 0→5→6→3→7→4→1
9. Design MOD-5 asynchronous counter.
10. Design a JK synchronous counter that counts the sequence 0,2,3,5,6,0,2…

TUTORIAL 6

Discuss Assignment -1

TUTORIAL SHEET-7

1. A presettable counter has 8 flip flops. If the preset number is 125, what is the modulus?
2. What is the basic difference between counter and shift registers.
3. Distinguish between combinational and sequential logic circuits
4. Derive the characteristic equation of a D flip-flop, T flip flop and SR flip flop
5. Draw a 4 bit shift left register.
6. Design a synchronous counter using D flip flop to count the following states:
   1→3→5→7→11→13→1→3…All unused states fall to '1'.
7. List the applications of Shift registers.
8. What is the Mod of 6-bit counter?
9. Mod 8 counter counts from _____ to _____.
10. If the output frequency of mod-12 counter is 6 Khz, What is its input frequency?

TUTORIAL 8

Discuss Sess-1

TUTORIAL SHEET-9

Q1. Find the conversion time and conversion rate for a successive approximation A/D converter having 2MHz clock and a 5-bit binary ladder containing reference voltage of 8V.

Sol.) Conversion time: 2.5usec

Conversion rate: $4* 10^5$Conversion usec.

Q2. A 6-bit R-2R ladder D/A converter has reference voltage of 6.5V.It meets standard linearity. Calculate

1. Resolution in Volts and Percentage
2. Full Scale Voltage
3. Output for 011100
4. Range in output for (3)
5. Quantization error

Sol.)

1) Resolution in Volts=0.1V
   Resolution in Percentage=1.578%

2) 6.4 V
3) V out =2.84V
4) Range=2.84 +0.05V,2.84-0.05V
5) Q.E.=0.079%

Q3. An 4-bit D/A converter has an output range 0f '0' to '1.5 V'. Define its resolution.

Sol.) R=2^n =2^4=16

Thus, the output voltage can have 16 different values including zero.

R=0.1V

Q4. Calculate the step size and analog output for 8-bit ADC when input is 10000000.Reference Voltage , V r=+50V is given

Sol.) Resolution=0.196 V/LSB

Vo=50.176 V

Q5. Discuss the advantage of binary ladder network over a binary weighted resistor chain in D/A converter.

Q6. Find the output voltage from a 5-bit ladder that has a digital input of 11010.Assume that 0=0V and 1=+10V.

Sol.) V out=8.125 V

Q7. An 8-bit successive approximation converter (SAC) has a resolution of 15mV.What will its digital output be for an analog input of 2.65V.

Sol.) Digital output=$\frac{Analog\ input}{Resolution}$

= 10110000

Q8. Determine the resolution of the output from a DAC that has a 12-bit input.
Sol.) Resolution=2^{12}=4096

Q9. An A/D converter has the following characteristics: resolution=12 bits; relative Accuracy =0.03 percent full scale; and full scale output=+5V.

i. What is quantization error in volts?
ii. What is the possible error in volts?

Sol.)

i. +0.6mV,-0.6mV
ii. 1.5mV

Q10. On what factors does the percentage resolution of D/A converter depend?
Sol.) The percentage resolution of D/A converter is given by:

% Resolution=$\frac{Vofs}{2^n-1}$ * 100

So, it depends on the full scale output voltage Vofs and the number of bits used in DAC i.e. 'n'.

TUTORIAL SHEET-10

Q1. Which is the fastest ADC and why?

Sol.)

Flash type ADC is the fastest ADC. Its main advantage is that its conversation of analog to digital taken place simultaneously and not sequentially. Typically the conversion time of flash type ADC is 100ns or less. Hence it is the fastest ADC.

Q2. What is the advantage of the R-2R ladder DAC over the weighted resistor type DAC?

Sol.)

Advantages of R-2R Ladder:

1. R/2R ladder DAC need only two value of resistors whereas in weighted resistor DAC several resistors are required having different values.
2. Due to small resistance spread, the R/2R ladder DAC can be fabricated monolithically, with high accuracy and stability. In weighted type, it is difficult to achieve and maintain accuracy and resolution.
3. The number of bits can be increased in R/2R ladder DAC by adding more sections of same R/2R values whereas it is not possible in the weighted type DAC with same value resistors.

Q3. A counter type A/D converter contains a '4' bit binary ladder and is driven by a 2MHz clock, calculate:

1. Conversion time and conversion rate.
2. Resolution.

If Vr is reference voltage for ladder network and is 2V.

Sol.)

1. Conversion time=125* 10 raise to the power3 conversions/sec.

   Conversion time=8 u sec

2. Resolution, R=0.125V

Q4. Draw nMOS NAND gate

Q5. Draw pMOS not gate

Q6. Draw cMOS NOR gate

Q7. Compare performance of ECL with TTL.

Sol.)

ECL	TTL
1. Propagation delay in 500 ps. 2. Noise margin is 150 mV. 3. Power dissipation is 5 mW. 4. Fan-out is 25. 5. 0.5 pJ is figure of merit.	1. Propagation delay in 10ns. 2. Noise margin is 0.4V. 3. Power dissipation is 10 mW. 4. Fan-out is 10. 5. 100 pJ is figure of merit.

Q8. Define Fan-in, Fan-out, Propagation delay, Noise immunity, Noise margin.

TUTORIAL SHEET-11

Q1. Calculate the Fan-out if the following values of currents are given

IOL(max)=15mA IOH(max)=1 mA

IIL(max)=0.2mA IIH(max)=8uA

Sol.) Fan-out(low)=75

Fan-out(high)=125

Q2. Calculate the speed-power product for an IC family having average power dissipation of 5mw and propagation delay time of 6nsec.

Sol.) 30 pico Joules (pJ)

Q3. How many memory chips are required to design 4K-byte memory if the chip size of memory is 1K * 1.

Sol.) 32 chips

Q4. Obtain 16*8 memory using 16*4 memory IC's.

Sol.) Number of memory chips required =2chips.

Q5. How will you interface CMOS to TTL, using different power supplies, and same power supplies, explain.

Q6. What are the advantages of CMOS?

Q7. What is TSL?

Q8. Draw CMOS NAND Gate.

TUTORIAL SHEET-12

Discuss Quiz 2

TUTORIAL SHEET-13

Q1. If a memory is having 14 address lines and 10 data lines, then calculate the number of memory locations and word length.

Sol.) N=14

Number of memory locations is given by:2^N=16,384 memory locations.

Word length is of M bit and M is data lines.

M=10 bit.

Q2. Obtain 32* 4 memory using 16* 4 memory chips.

Sol.) Number of memory chips required=2 chips.

Q3. Implement the Boolean function using PAL

Y1=∑m (1, 3, 5, 7)

Y2=∑m (2, 4)

Q4. What is the difference between PAL and PLA?

Sol.)

PLA	PAL
6. In case of PLA i.e. programmable logic Array both AND and OR arrays are Programmable. 7. It is costlier as compared to PAL. 8. It is complex than PAL 9. It can't be easily programmed.	1. In case of PAL i.e. programmable array Logic OR arrays are fixed and AND arrays are programmable. 2. It is cheaper. 3. It is simple. 4. It is easy to program a PAL. 5. It is not possible using ROM.

Q5. Implement the function

F=$A'BC + ABC' + A'B'C + AC'$ using PLA.

Q6.The capacity of 2K * 16 PROM is to be expanded to 16K * 16.Find the number of PROM Chips required and the number of address lines in the expanded memory.

Sol.) Number of PROM chips required=8 chips.

$16384 = 2^{14}$

Address lines=14

Q7. What is programmable logic array? How it differs from ROM?

Sol.) Programmable logic array are those in which AND and OR arrays are programmable. The AND and OR gates are fixed by any PLA chip. It depends on the number of inputs and Outputs of PLA.

Difference between PLA and ROM is as shown in table:

PLA	ROM
1. PLA make use of ROM for its designing. 2. Using PLA the cost reduces. 3. Switching speed becomes high. 4. PLA is used for higher density. 5. Larger flexibility can be achieved using PLA.	1. It doesn't use PLA in it. 2. Costlier 3. Switching speed becomes slow. 4. Low density. 5. It is not possible using ROM.

Q8. The difference between static and dynamic memories.

Sol.)

Static Memory	Dynamic Memory
1. Static memory consists of flip-flops that make a cell. 2. Static memory does not require refreshing. 3. Cost is more. 4. Access time is less so considered as fastest memories.	1. In dynamic memory one MOSFET and Capacitor makes a unit. 2. Dynamic memory requires refreshing. 3. Cost is less. 4. Access time is more so considered As slower memories.

Q9. What is the exact number of bytes in a system that contains (a) 32K byte, (b) 64M bytes, and (c) 6.4G byte?

Q10. Compare static RAMs and dynamic RAMs

Q11. Define PLDs

Q12. Draw a neat sketch showing implementation of

Z1 = ab'd'e + a'b'c'e' + bc + de ,

Z2 = a'c'e,

Z3 = bc

+de+c'd'e'+bd and

Z4 = a'c'e +ce using a 5*8*4 PLA

TUTORIAL – 14
Discuss Assignment 2

TUTORIAL – 15
Discuss Sess-2