Class Test – II **Name: _____**

MCA 2nd Year 2nd Semester **Class Roll: _____**

Session: 2013-14

Date: 08/04/2014 **Marks Obtained: _____**

Full Marks: 30

Time: 50 minutes

Write proper justifications for all your answers

1. In a system, the page size is 16 and it uses LRU page replacement policy. Number of frames allocated to a process is 4. A process generates the following sequence of virtual addresses:
   0, 4, 8, 20, 24, 36, 44, 12, 68, 72, 80, 84, 28, 32, 88, 92
   How many page faults does this sequence cause? What are the page numbers of the pages present in the main memory at the end of the sequence?

2. Assume that we have a demand-paged memory. The page table is held in registers. It takes 8 milliseconds to service a page fault if an empty frame is available or if the replaced page is not modified and 20 milliseconds if the replaced page is modified. Memory-access time is 100 nanoseconds. Assume that the page to be replaced is modified 70 percent of the time. What is the maximum acceptable page-fault rate for an effective access time of no more than 200 nanoseconds?

3. Given five memory partitions of 100 KB, 500 KB, 200 KB, 300 KB, and 600 KB (in order), how would each of the first-fit, best-fit, and worst-fit algorithms place processes of 212 KB, 417 KB, 112 KB, and 426 KB (in order)? Which algorithm makes the most efficient use of memory?

4. A process uses 2-level page table for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual address is 32 bit wide and physical address is 30 bit wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache. Main memory access time is 10 ns, cache access time is 1 ns, and TLB access time is also 1 ns. Assume that no page faults occur, determine the minimum cache hit rate so that average time taken to access a virtual address is maximum 3.2 ns. Also determine the maximum number of bits that can be used for storing protection and other information in each page table entry.

7+8+7+8=30