Class Test – II **Name: _____**

MCA 2nd Year 2nd Semester **Class Roll: _____**

Session: 2016-17

Date: 24/10/2016 **Marks Obtained: _____**

Full Marks: 30

Time: 50 minutes

Write proper justifications for all your answers

1. Consider a paging system with 36 bit logical address and 32 bit physical address. Size of each page table entry is 4 bytes. Assume that you want to implement a multi level page table. Determine how many levels of page table is required if you need to store each page of the page table possibly in non contiguous frames. Compare the size of single level and multi level page table considering two cases where page sizes are 4 KB and 8 KB respectively. Also, determine the division of bits of the logical address that is required to address each levels of the multi level page table for both the cases.
2. In a system inverted page table is used. Size of the inverted page table is 16 MB. Each entry of the inverted page table stores pid, page number and some protection information. Logical address space is 32GB, physical memory size is 16 GB and page size is 4 KB. Process pid is represented by 8 bit. Determine the maximum number of bits that can be used for storing protection information in each entry of the inverted page table.
3. In a system, the page size is 64 and it uses LRU page replacement policy. Number of frames allocated to a process is 3. A process generates the following sequence of virtual addresses:
   80, 44, 128, 200, 204, 360, 244, 140, 68, 72, 280, 188, 192
   How many page faults does this sequence cause using each of the page replacement algorithms LRU and optimal?
4. Assume that we have a demand-paged memory. The page table is held in memory. It takes 10 milliseconds to service a page fault if an empty frame is available or if the page to be replaced is not modified and 25 milliseconds if the page to be replaced is modified. Memory-access time is 80 nanoseconds. Assume that the page to be replaced is modified 40 percent of the time. What is the maximum acceptable page-fault rate for an effective access time of no more than 240 nanoseconds?

12+6+6+6=30