Class Test – II **Name: _____**

MCA 2nd Year 2nd Semester **Class Roll: _____**

Session: 2015-16

Date: 04/11/2015 **Marks Obtained: _____**

Full Marks: 30

Time: 1 Hour

Write proper justifications for all your answers

1. In a system the sequence of logical addresses generated by a process are 10, 36, 68, 42, 72, 98, 162, 76, 48, 200, 100, and 230. The page size is 32 bytes. A process has been allocated 3 frames in physical memory. Determine the number of page faults that these references will generate using FIFO, LRU and Optimal page replacement policy.

2. Consider a paging system with 36 bit logical address and 32 bit physical address. Page size is 4 KB and size of each page table entry is 4 bytes. Determine the size of page table if single level page table is used. How many bits in each page table entry can be used for storing protection and other information?

   Now, assume that you want to implement a multi level page table. Determine how many levels of page table is required if you need to store each page of the page table possibly in non contiguous frames in physical memory. Determine the division of bits of the logical address that is required to address each levels of the multi level page table. Also determine the size of the multilevel page table.

   If physical memory access time is 10 nanoseconds, compare the effective memory access time of the single level and proposed multi level paging scheme.

3. In a system inverted page table is used. Each entry of the inverted page table stores pid and page number. Logical address is 36 bit, physical memory size is 16 GB and page size is 4 KB. Process pid is represented by 8 bit. Determine size of the inverted page table.

4. In a demand paging system memory access time is 10 ns and page fault service time is 25 ms. What should be maximum page fault rate so that performance does not degrade more than 20%?

5.
   a. Differentiate between compile time and load time address binding.
   b. What is the utility of dirty bit?

8+10+6+3+3=30