Class Test – II **Name: _____**

MCA 2nd Year 1st Semester **Class Roll: _____**

Session: 2018-19

Date: 14/11/2018 **Marks Obtained: _____**

Full Marks: 30

Time: 60 minutes

Write proper justifications for all your answers

1. What is the advantage of execution time address binding over load time address binding?

2. Consider a system with 30 bit logical address and 28 bit physical address. The system implements an inverted page table. It uses a page size of 8 KB and uses 15 bits as process id. What is the size of each entry in the inverted page table? Also, determine the size of the inverted page table.

3. What is the use of dirty bit in page replacement?

4. Consider a paging system with 32 bit logical address and 30 bit physical address. Page size is 4 KB and size of each page table entry is 4 bytes. Determine the size of page table if single level page table is used. Also, determine the maximum number of bits that can be used to store protection and other information in each entry of the page table. If memory access time is 100 ns, how much time a paged memory reference takes in average?

   Now, assume that a TLB with hit rate of 90% and access time 2 ns is introduced to cache most recently used page table entries. Calculate average memory reference time.

   Additionally you have been given a physically addressed cache memory with hit rate of 80% and access time 10 ns. Calculate average memory reference time.

5. In a computer the sequence of logical addresses generated by a process are 110, 140, 540, 130, 260, 400, 60, 540, 320, 648, 380, and 520. The page size is 128 bytes. Determine reference string for this process. Assume that the process has been allocated 3 frames in physical memory. Determine the number of page faults that these references will generate using LRU and Optimal page replacement policy.

2+6+2+10+10=30