Class test of MCA 1st year 2nd Semester
Session: 2020-21
Subject: Computer Organisation and Architecture
Time: 1hr (Before exam: 10 min for download) (After exam: 20 min for upload)
Full marks: 30
File name: MCA_COA_15 (If 15 is the last two digits of your roll number)
File type: PDF

Answer all
(Q1-Q22: 1mark for each)

Say true or false

1. A particular architecture may span many years and encompass a number of different computer models, its organization changing with changing technology.

2. All DRAMs require a refresh operation.

3. The disadvantage of using CAV is that individual blocks of data can only be directly addressed by track and sector.

4. SSD performance has a tendency to speed up as the device is used.

5. With a daisy chain the processor just picks the interrupt line with the highest priority.

6. An I/O channel has the ability to execute I/O instructions, which gives it complete control over I/O operations.

7. Cycle stealing is when the DMA module must force the processor to suspend operation temporarily. So this is like an interrupt to the CPU.

Fill in the blanks

8. When using the _____ technique all write operations made to main memory are made to the cache as well.

9. The key advantage of the _____ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit.

10. A _____ error is a random, nondestructive event that alters the contents of one or more memory cells without damaging the memory.

11. RAID level _____ has the highest disk overhead of all RAID types.

Choose the correct option

12. If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?

(a) Width of tag comparator

(b) Width of set index decoder
(c) Width of way selection multiplexor
(d) Width of processor to main memory data bus

13. Which of the following addressing mode is best suited to access elements of an array of contiguous memory locations?

(a) Indexed addressing mode
(b) Base Register addressing mode
(c) Relative address mode
(d) Displacement ode

14. Stack-organized computer uses:

A) Indirect addressing,
B) 1-address scheme
C) 0-address scheme
D) 2-address scheme

15. Memory access in RISC is limited to instructions:

(a) Call-Return
(b) Push-Pop
(c) Store and Load
(d) Mov-Jmp

16. Virtual memory is a concept of

(a) Extremely large main memory
(b) Extremely large secondary memory
(c) An illusion of extremely large memory
(d) Extremely large memory used in super-computers only

17. Which type of address is generated by CPU?

(a) Physical
(b) Logical
(c) Absolute
(d) Relative

18. Which one is false?

(a) Nanoprogrammed control unit takes less space in control memory
(b) Microprogrammed control unit is flexible in updating the operations and behaviour.
(c) Hardwired control unit follows an ad-hoc technique.
(d) All the above are false

19. _____ addressing mode is most suitable to change the normal sequence of execution of instructions.
(a) Relative

(b) Indirect
(c) Index with Offset
(d) Immediate

20. Which representation is most efficient to perform arithmetic operations on the numbers?

(a) Sign-magnitude
(b) 1's complement
(c) 2'S complement
(d) All of the above

21. In memory-mapped I/O _____

(a) The I/O devices and the memory share the same address space
(b) The I/O devices have a separate address space
(c) The memory and I/O devices have an associated address space
(d) A part of the memory is specifically set aside for the I/O operation

22) In the memory hierarchy which one does not fit?

a) Main memory
b) Control memory
c) Cache memory
d) External memory

23) A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. What is the number of bits for the TAG field? **(Marks: 2)**

24) A processor that has carry, overflow and sign flag bits as part of its program status word (PSW) performs addition of the following two 2's complement numbers 01001101 and 11101001. After the execution of this addition operation, what will be the status of the carry, overflow and sign flags? **(Marks: 3)**

25) Suppose your 4-digit class roll number is 1244. Add 5 zeros like this: 100204004. Now add the last digit at the 1st position, and the number becomes 4100204004. Consider this as the reference string. Show how many page faults you come across when you use 3 frames and policies of page replacement from cache to main memory is LRU (*if your roll number is even*) or FIFO (*if your roll number is odd*). **(Marks: 3)**