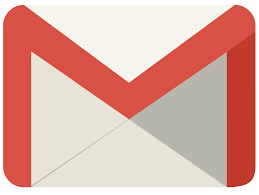
**Nishant Shukla**

16th July 1997



[nashukla@gmail.com](file:///C:\Users\Priya\AppData\Roaming\Microsoft\Word\nashukla@gmail.com) +91 9408761514 Karnataka, INDIA

**Objective**

To explore new possibilities in VLSI industry advancement and to obtain a position that challenges me and provides me the opportunity to reach my full potential professionally.

**Experience**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Organization** | **Designation** | **Job Profile** | **Year Of Joining** | **Total Working Experience** |
| L & T Technology Services | Senior Engineer | Post silicon validation | 2021 | 3.7 years (Currently working) |

**Core Competencies:**

|  |  |
| --- | --- |
| * Functional validation * System level debug * Performance stress testing * Digital design * Python and C language | * HDL: Verilog, System Verilog * I2C, UART Protocol * AMBA BUS Protocols (APB, AHB, AXI) * Git * BKC Regression testing |

**Tools used**: Post silicon validation flows | Functional Performance testing tools | Bug tracking tool | JIRA | CPU Power management tool | Verdi | Questa Sim| SIMVISION | VCS compiler| Windows| Linux| Microsoft office

**Projects:**

**Client Project (AMD)**  April 2025 – Till now

**Description**: Data center validation project. Worked on BIOS regression checks

* Understanding of BIOS recipe components like SMU, ACPI, NBIO and Morden standby.
* Involved in activity to bring up the system with latest BIOS version for the regression checks for different components.
* Ramped up on Jira and PowerBi reporting mechanism for the triage and debug activity.

**Client Project (Intel)**  March 2023 – February 2025

**Description**: Functional validation of the server grade SoC, involved in functional performance testing validating multiple IPs and thermal parameters. Stressing IIO, RAS, Accelerators, Virtualization, Core, Power management IPs and debugging at system level as well as IP level with help of BIOS and SW teams.

* Understanding of SoC at high level integrating at board level configuring with different IO devices like PCIe, CXL, DDR5 memory.
* Created and maintained test documentation to ensure traceability and automate test cases to reduce timeline for silicon stepping.
* Utilized functional performance tool, thermal stress tool and core stress tool to execute manual and automated testcases.
* Collaborated with BIOS, OS and IP level teams to debug the failures and improve the debug resolution timeline via applying top-down and bottom-up approach as per the failure signatures.
* Worked as front-end developer to design a tool for client having AI capabilities to reduce time to market by mitigating all redundant testcases and optimize test patterns.
* Update python scripts according to test requirements of the silicon and debug the failure scenarios.
* Planned 600+ testcases throughout post silicon cycle with having functional coverage goal and executed around 150 testcases manually to validate IP level sanity.
* Debug core throttling via collaborating with PM, virtualization and tools team via modifying test script and core counts reduction from BIOS and validate the functionality as per the spec documents.
* Lead performance testing team and carried out client discussion and identify clear deliverables and guide the team for in time delivery of the project.
* Adopted hardware debug flow with combination of top-down and bottom-up approach to debug functional and environmental bugs in timely resolution.
* Bucketized failures in the automation flow and debug functional bugs via control register checks and system state capture logs.
* Maintained bug/failure tickets with technical findings and proper justifications. Maintained functional coverage data in the client given format to make test plans and test cases for different stages of the silicon.
* Generate PowerBI reports and communicate it to client in the efficient manner for the team.

**Client Project (Intel)**  March 2022 – January 2023

**Description**: IP Design verification project, involved in verification tasks of I2C, I3C and UART protocols. Involved in GLS activity for the violation checks.

* Understanding 7 nm SoC architecture for verification planning of peripheral protocols.
* Developed read/write transaction testcases for peripheral protocols in UVM environment with C language.
* Developed sequence, generator units for I2C and UART protocol checks.
* Developed interrupt routine testcase for I2C and I3C master IP.
* Debug failure testcases with the help of Verdi tool waveform and backtracking it to RTL codes.

**Training Project** December 2021 – February 2022

**Description:** Verification of AMBA AHB protocol using UVM methodology, develop UVM based SV testbench for AMBA AHB protocol.

* Understanding the AMBA AHB protocol specifications.
* Developed UVM based SV test bench architecture.
* Developed top, test, environment, sequencer, driver, monitor, sequence item and sequence for the same.
* Prepared the test bench plan and verified different test cases using UVM.

**Education Qualification**

|  |  |  |  |
| --- | --- | --- | --- |
| **Qualification** | **Institute** | **Year Of Passing** | **CPI/Percentage (%)** |
| M.Tech (Electrical Power System) | Nirma University | 2021 | 8.15 |
| B.Tech (Electrical Engineering) | Pandit Deendayal Petroleum University | 2019 | 6.7 |

**Internship**

* Analysis and design of a high frequency asymmetrical half-bridge flyback converter for space application, SAC ISRO July 1, 2020 – May 1, 2021
* Internship, Adani power limited June 2017 – July 2017

**Co-Curricular Achievements**

* Certified in Python
* Certified in JIRA, PowerBI
* Certified in Kanban

**Achievements**

* Star of the Month in November 2024.
* Nomination for Rising Star Award during Estrella’s 24

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| **Name** | **Nishant Shukla** |
| **Languages Known** | **English, Hindi, Gujarati** |
| **Permanent Address** | **Shri Ramkrishna, Amrut Nagar society – 2, Near Crystal Mall, Kalawad Road, Rajkot, Gujarat, 360005** |

**Personal Information**

The information provided above is true to the best of my knowledge.