CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
ITT203	DIGITAL SYSTEM DESIGN	PCC	3	1	0	4

Preamble: The syllabus is prepared with the view of preparing the Engineering Graduates capable of understanding the basic digital logic design and implementation. All students of computing should acquire some understanding and appreciation of a computer system's functional components, their characteristics, their performance, and their interactions.

Prerequisite: NIL

Course Outcomes: After the completion of the course, the student will be able

CO No.	Course Outcome(CO)	Bloom's Category
CO 1	To perform base conversion and arithmetic operations in various number systems.	Apply
CO 2	To design digital circuits using simplified Boolean functions	Create
CO 3	To develop simple design of combinational circuits	Apply
CO 4	To develop simple design of sequential circuits	Apply
CO 5	To interpret the generalization of synchronous and asynchronous sequential circuits	Understand

Mapping of course outcomes with program outcomes

COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3			3	-	-	-	-	-	-	-	2
CO 2	3	3	3	3	-	-	-	-	-	-	-	2
CO 3	3	3	3	3	-	2	-	1	-	-	-	2
CO 4	3			3	-	-	-	-	-	-	-	2
CO 5	3	3	3	3	2	2	-	1	-	-	-	2

3/2/1: high/medium/low

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination Marks
	Test 1 (Marks)	Test 2 (Marks)	
Remember	10	5	20
Understand	15	10	20
Apply	10	10	25
Analyse	10	10	15
Evaluate	5	10	10
Create		5	10

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
150	50	100	4 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): To understand the basic concepts of Number systems

1. Convert the given number from decimal number system to binary, octal, and hexadecimal number system.
2. Perform Arithmetic operations on different number system.
3. Represent the different coding schemes.

Course Outcome 2 (CO2): To design digital circuits using simplified Boolean functions

1. Simplify the given expression using Postulates of Boolean algebra.

2. Convert a given expression to standard and canonical forms.
3. Simplify the given expression using Karnaugh Map or Quine –McClusky minimization technique.

Course Outcome 3 (CO3): To analyze and design combinational circuits

1. Analyse a given circuit and explain the results obtained by the circuit.
2. Design a Ccarry look ahead adder.
3. Design a four-bit magnitude comparator.

Course Outcome 4 (CO4): To understand the basics of sequential circuits

1. Understand the functioning of Latches and Flip Flops.
2. Design Master-Slave Flip Flops.
3. Understand the basics of different types of Flip Flops.

Course Outcome 5(CO5): To analyze and design synchronous and asynchronous sequential circuits

1. Analyse a given circuit and explain the results obtained by the circuit.
2. Implement a serial adder using a shift register.
3. Design and construct a 4-bit ring counter with only one flip-flop is clear at any particular time and all other flip-flops are set. Give its timing diagram.
4. Using an example, show the Race-Free State Assignment in an asynchronous sequential circuit.

Model Question Paper

Course Code: ITT203
Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A
Answer all questions, each carries 3 marks.

1. Convert $(76.75)_{10}$ to binary, octal and hexadecimal.
2. Determine the base of the numbers in the operation; $\mathbf{58/4}$= 15.
3. Simplify the Boolean expression to minimum number of literals.
   $\boldsymbol{F=BC+AB+ABC+ABCD+\bar{A}BCD+ABCD}$
4. Find the complement of the Boolean function $\boldsymbol{F=\bar{A}+ABC}$.And prove that $\boldsymbol{F+\bar{F}=1}$and $\boldsymbol{F.\bar{F}=0}$.
5. Design a 4-to-2 line priority encoder.

6. Explain the difference between a latch and a flip-flop.

7. Give the characteristics equations for D, JK and T flip-flops.

8. Discuss in detail about Race condition.

9. With a neat diagram, discuss about SISO.

10. Design a 4-bit ring counter.

PART B
Answer all questions, each carries 14 marks.

11. a) Using Booth algorithm, perform multiplication of (-14) and (-7). (5)

b) Represent the unsigned decimal numbers 572.36 and 382.71 in BCD. Show the necessary steps to form their sum and difference. (9)

OR

12. a) (i) Find the decimal equivalent of $(A40F)_{16}$
(ii) Find the 16's complement of $(A40F)_{16}$
(iii) Convert to binary $(A40F)_{16}$
(iv) Finds the 2's complement of the result in (iii) (8)

b) Perform addition, subtraction, multiplication, and division of the following binary numbers without converting them to decimal : 1000110 and 110. (6)

13. a) For the Boolean function
F = w′xy′+ xy′z + x′y′z + w′xy + wx′y + wxy

(i) Draw the logic diagram, using the original Boolean expression.
(ii) Simplify the Boolean algebra to a minimum number of literals.
(iii) Obtain the truth table of the function from the simplified expression and show that it is the same as the original Boolean expression. (9)

b) Prove that $A+\bar{A}B = A + B$ using Boolean postulates. (5)

OR

14. a) Simplify the following functions using Quine- McClusky method :
f (a,b,c,d) = Σm (2, 3, 4, 5, 13, 15) + Σd (8, 9, 10, 11). (7)

b) Using K-map simplify following Boolean expression & give implementation of same using gates F(A,B,C,D) =Σ (2,4,8,15)+ ΣD(0,3,9,12) (7)

15. a) Design a combinational circuit to implement a 4-bit carry look-ahead adder. (7)

b) Design a 4-bit code-converter to convert BCD to gray code. (7)

OR

16. a) Implement the Boolean function f(w,x,y,z) = Σm(0,1,5,6,7,9,12,15) using 8-to-1 multiplexer. (7)
    b) Implement a 2-bit Magnitude comparator and write down its design procedure. (7)

17. a) For the following state table

Present State	Next State		Output	
	x=0	x=1	x=0	x=1
a	b	c	0	0
b	d	f	1	0
c	b	e	0	0
d	f	h	1	0
e	b	e	0	0
f	g	a	1	1
g	a	h	0	0
h	g	e	1	1

i. Draw the corresponding state diagram.
ii. Tabulate the reduced state table.
iii. Draw the state diagram corresponding to the reduced state table.
iv. Design the sequential circuit using flip-flops. [Hint:Unused states may be considered, as don't cares.] (9)

b) Design D Flip Flop by using SR Flip Flop and draw the timing diagram. (5)

OR

18. a) Explain the state reduction in the sequential circuits using an example. (9)

    b) Draw the circuit of JK flip flop using NAND gates and explain its operation. (5)

19. a) Implement a four-bit universal shift register. Explain its design. (7)

    b) What do you mean by ripple counter? Design and implement a BCD ripple counter. (7)

OR

20. a) Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the numbers of product terms.
    $A(x, y, z) = \Sigma_m(1, 3, 5, 6)$
    $B(x, y, z) = \Sigma_m(0, 1, 6, 7)$
    $C(x, y, z) = \Sigma_m(3, 5)$
    $D(x, y, z) = \Sigma_m(1, 2, 4, 5, 7)$ (9)

    b) What are the operations that can be performed on a RAM? (5)

Syllabus

Module 1: NUMBER SYSTEM (9 Hours)
Number Systems – Decimal, Binary, Octal, Hexadecimal - conversion from one system to another – Representation of negative numbers using 2's compliment. Arithmetic Operations – Addition, Subtraction, Multiplication, Division of Binary numbers, Booths algorithm for multiplication, Representation of negative numbers, Representation of floating point numbers. Representation of BCD numbers, BCD Addition, Binary Codes – Gray codes – excess 3 code- Character Coding Schemes – ASCII, EBCDIC.
Module 2: BOOLEAN ALGEBRA & LOGIC GATES (9 Hours)
Boolean Algebra - Postulates of Boolean algebra - Canonical and Standard Forms - Simplification of Boolean Functions using Karnaugh Map - Product-of-Sums Simplification — Don't-Care Conditions – Quine –McClusky minimization technique – Basic Gates- Universal Gates.
Module 3: COMBINATIONAL LOGIC (9 Hours)
Combinational Circuits – Analysis and Design Procedures - Binary Adder-Sub tractor (Half & Full) - Carry look ahead adder, BCD adder, code converter, - Magnitude Comparator - Decoders – Encoders Parity Generator– Multiplexers – DE multiplexers – Implementation of Boolean functions using MUX.
Module 4: SEQUENTIAL LOGIC CIRCUITS (9 Hours)
Sequential Circuits - Storage Elements: Latches , Flip-Flops – RS, JK, D, T, Triggering of flip-flops, Master-Slave- Analysis of Clocked Sequential Circuits - Design Procedure-using JK,D & T.
Module 5: COUTERS AND SHIFT REGISTERS (9 Hours)
Registers - Shift Registers – SISO, PIPO, SIPO, PISO- Universal shift registers, Counters- Design of Counters- Synchronous & Asynchronous Counters — up-down counter, Decade counter, BCD counter, Johnson counter, Ring counter ,Memory & Programmable logic- RAM, ROM, PLA,PAL

Text Books

1. Mano M. M. and Michael D. Ciletti, *Digital Design*, 4/e, Pearson Education, 2013.
2. Thomas L. Floyd, *Digital Fundamentals*, 11th Edition, Pearson Education, 2015.
3. N. N. Biswas, *"Minimization of Boolean Functions,"* in *IEEE Transactions on Computers*, vol. C-20, no. 8, pp. 925-929, Aug. 1971. doi: 10.1109/T-C.1971.223373

Reference Books

1. Charles H Roth ,Jr, Lizy Kurian John, *Digital System Design using VHDL*,2/e, Cengage Learning
2. Mano M. M. and Michael D. Ciletti, Digital Design with an Introduction to the Verilog HDL, 5/e, Pearson Education, 2013.
3. Tokheim R. L., Digital Electronics Principles and Applications, 7/e, Tata McGraw Hill, 2007.
4. Rajaraman V. and T. Radhakrishnan, *An Introduction to Digital Computer Design*, 5/e, Prentice Hall India Private Limited, 2012.
5. Leach D, Malvino A P, Saha G, *Digital Principles and Applications*, 8/e, McGraw Hill Education, 2015.
6. M. Morris Mano, *Computer System Architecture*, 3/e, Pearson Education, 2007.

7. Harris D. M. and, S. L. Harris, *Digital Design and Computer Architecture*, 2/e, Morgan Kaufmann Publishers, 2013

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**NUMBER SYSTEM**	**9 Hours**
1.1	Number Systems – Decimal, Binary, Octal, Hexadecimal - conversion from one system to another – Representation of negative numbers using 2's compliment.	3 hours
1.2	Arithmetic Operations – Addition, Subtraction, Multiplication, Division of Binary numbers, Booths algorithm for multiplication, representation of negative numbers, Representation of floating point numbers.	4 Hours
1.3	Representation of BCD numbers , BCD Addition Binary Codes – Gray codes – excess 3 code- Character Coding Schemes – ASCII, EBCDIC	2 Hours
2	**BOOLEAN ALGEBRA & LOGIC GATES**	**9 Hours**
2.1	Boolean Algebra - Postulates of Boolean algebra - Canonical and Standard Forms	2 Hours
2.2	Simplification of Boolean Functions using Karnaugh Map - Product-of-Sums Simplification — Don't-Care Conditions	2 Hours
2.3	Quine –McClusky minimization technique	2 Hours
2.4	Basic Gates-Universal Gates.	3 Hours
3	**COMBINATIONAL LOGIC**	**9 Hours**
3.1	Combinational Circuits – Analysis and Design Procedures - Binary Adder-Subtractor - Carry look ahead adder, BCD adder	3 Hours
3.2	Code converter, - Magnitude Comparator - Decoders – Encoders – Multiplexers	3 Hours
3.3	Parity Generator– Multiplexers – DE multiplexers – Implementation of Boolean functions using MUX.	3 Hours
4	**SEQUENTIAL LOGIC CIRCUITS**	**9 Hours**
4.1	Sequential Circuits - Storage Elements: Latches , Flip-Flops – RS, JK, D, T, Triggering of flip-flops, race condition- Master-Slave	3 Hours
4.2	Analysis of Clocked Sequential Circuits	3 Hours
4.3	State Reduction and Assignment - Design Procedure- using JK,D & T	3 Hours
5	**COUTERS AND SHIFT REGISTERS**	**9 Hours**
5.1	Registers - Shift Registers – SISO, PIPO, SIPO, PISO- Universal shift registers	2 Hours
5.2	Design of Counters- Synchronous & Asynchronous Counters — up-down counter.	3 Hours
5.3	Counters-, Decade counter, BCD counter, Johnson counter, Ring counter	2 Hours
5.4	Memory & Programmable logic-RAM, ROM, PLA,PAL	2 Hour