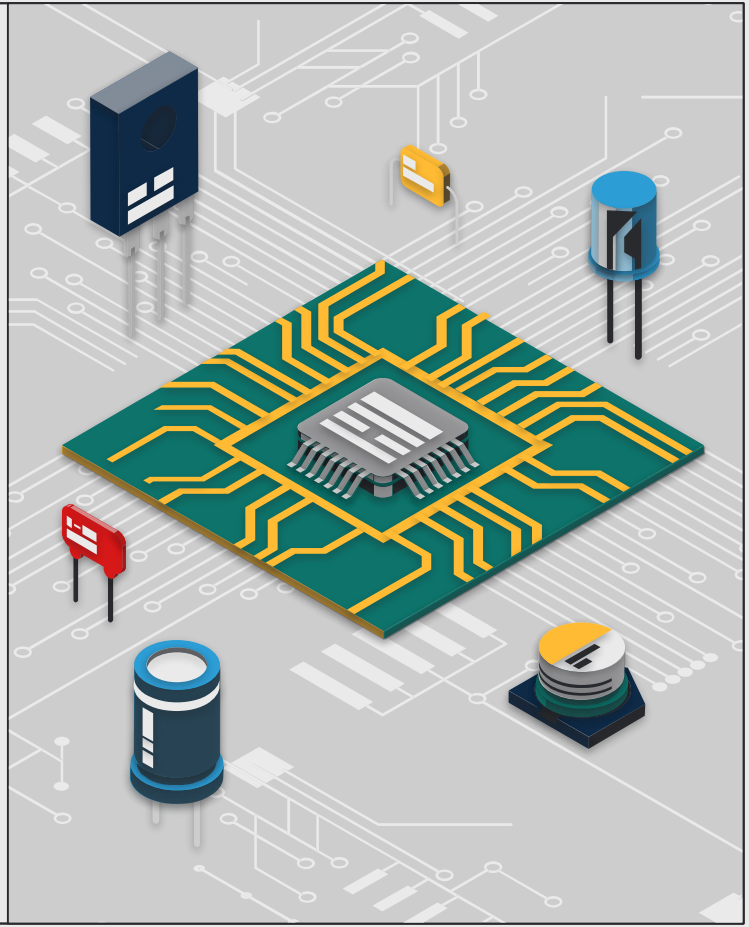
Project: Full Chip Design of an Automated Toll Booth System

EEE 4232
VLSI II Lab



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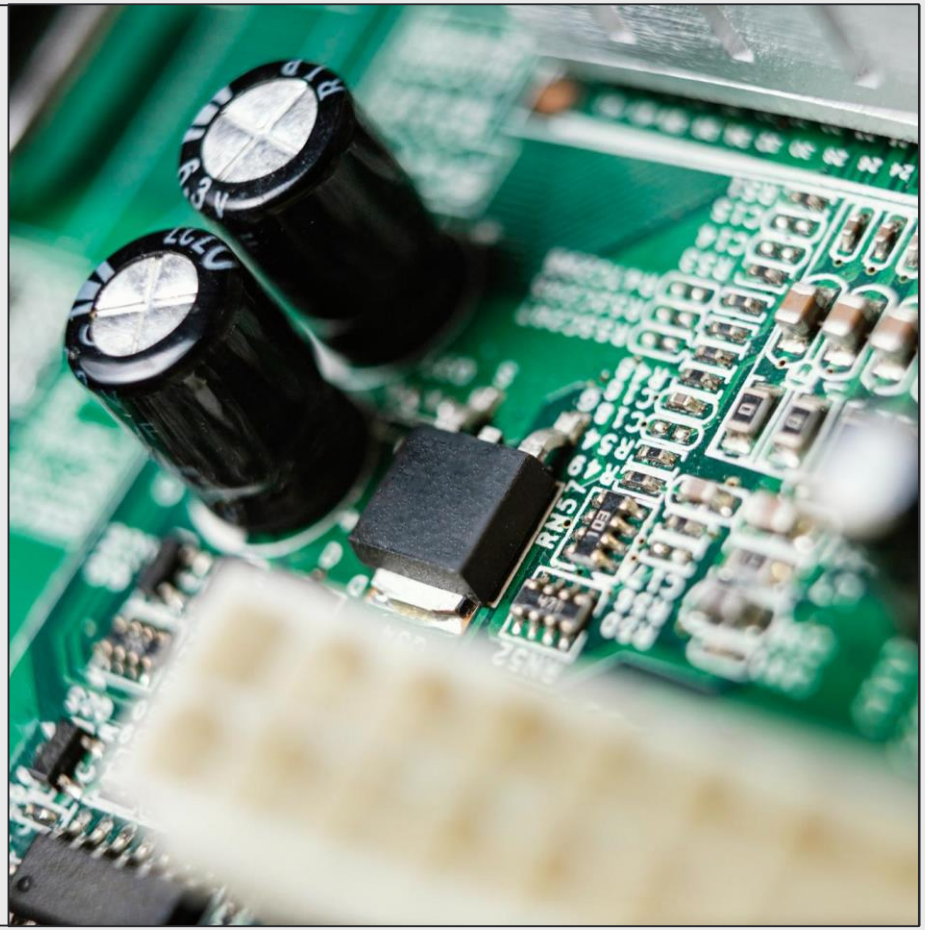
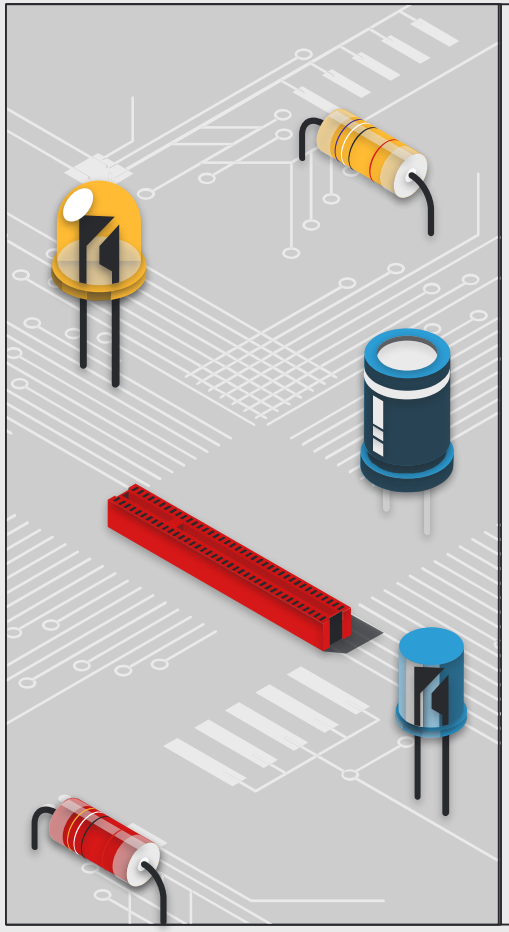
Introduction

Currently, toll booths in Bangladesh are operated manually, leading to inefficiencies and delays. Our project aims to develop **an automated toll booth system** to streamline toll collection with **minimal human involvement**. The system classifies vehicles, calculates the correct toll using a state machine model, and ensures accurate payment before granting access. Utilizing RTL design, synthesis, and physical design with tools like Quartus Prime II and Cadence, this system promises improved efficiency, accuracy, and scalability for toll collection in Bangladesh.





1: Design Specifications

- The automated toll booth system follows some specific design specifications based on **vehicle type and payment** categories in Bangladeshi Taka (BDT).
- Toll charges for different vehicle types:

1. Bike: 30 BDT
2. Private car: 50 BDT
3. Large car: 80 BDT
4. Bus/Truck: 100 BDT

- The system is modeled using a **state machine** to ensure correct toll collection.
- Vehicles follow a rotating system of states based on the **amount of money paid**.
- Payments can only be made in increments of 10, 20, 50, or 100 BDT.

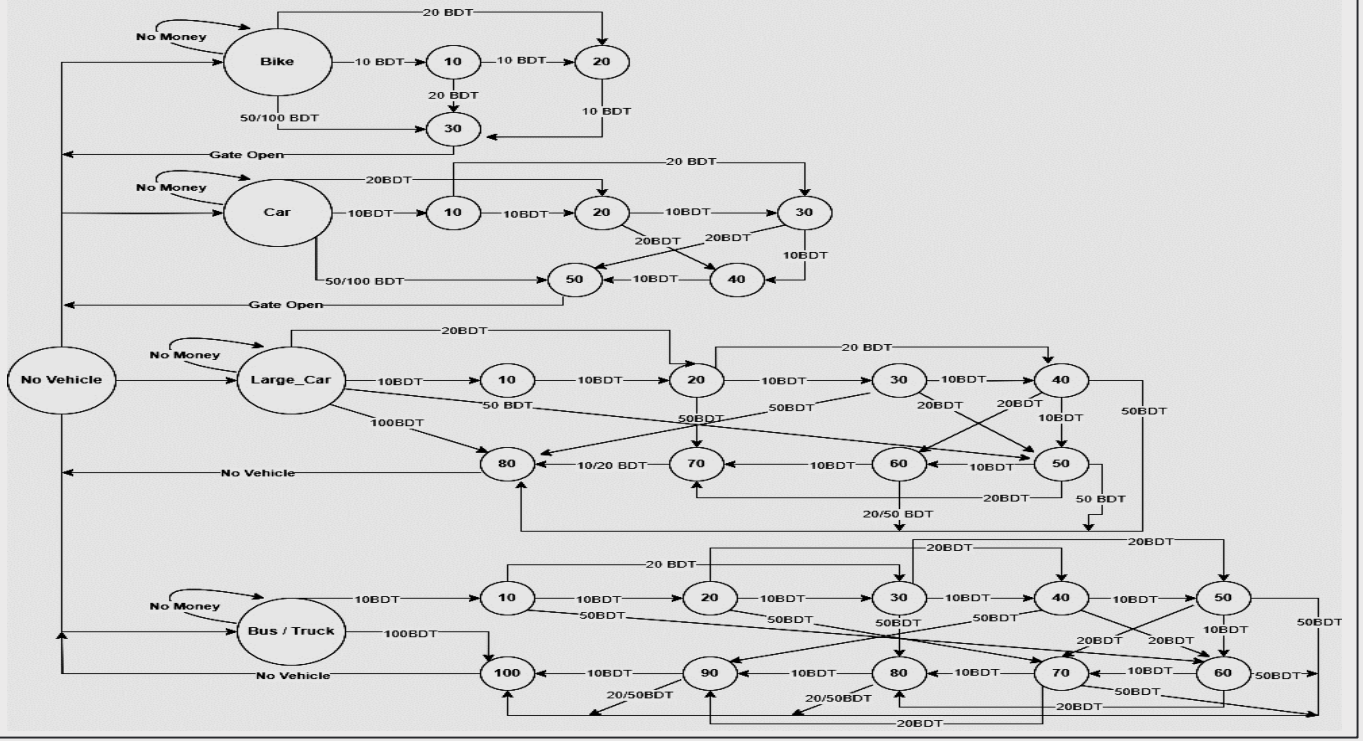
2: FSM

Toll Booth	
Bike	30 BDT
Car	50 BDT
Large Car	80 BDT
Bus/Truck	100 BDT

Rules:

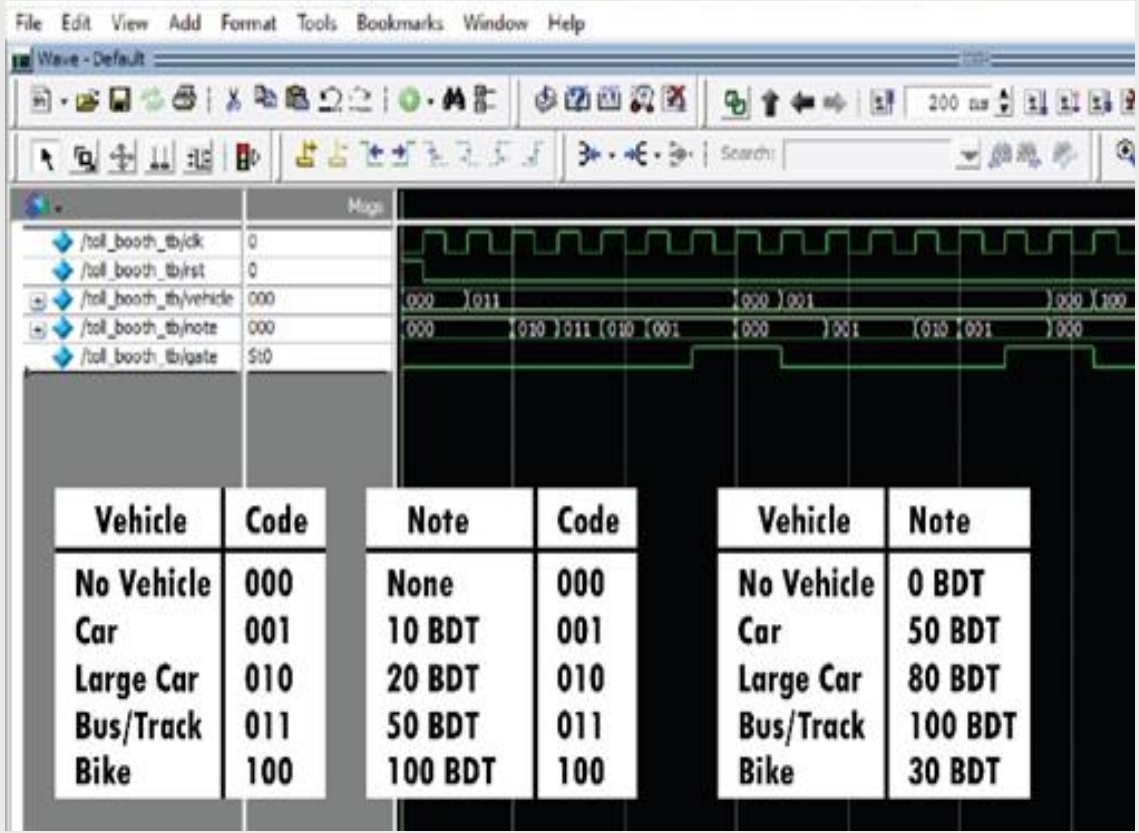
.Only Allow:
10 BDT
20 BDT
50 BDT
100 BDT

- Gate must close after vehicle leaves
- No change given
- No backing out

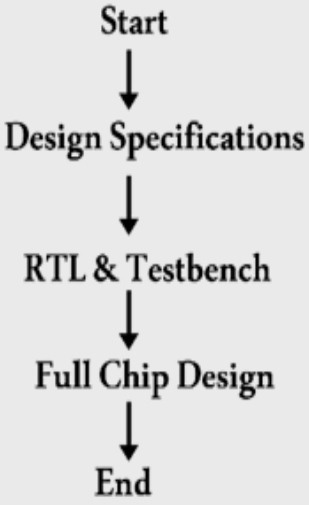


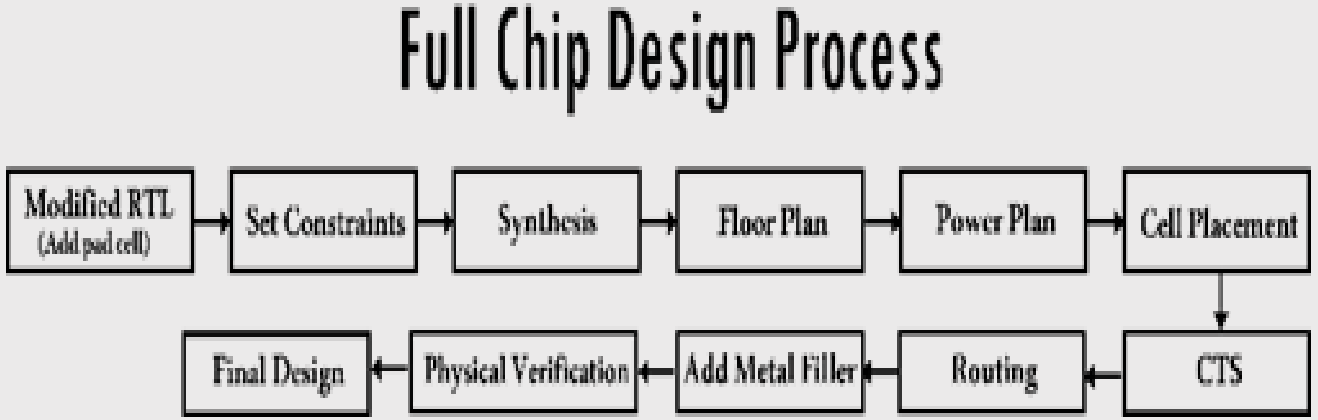
3: RTL & Testbench Design

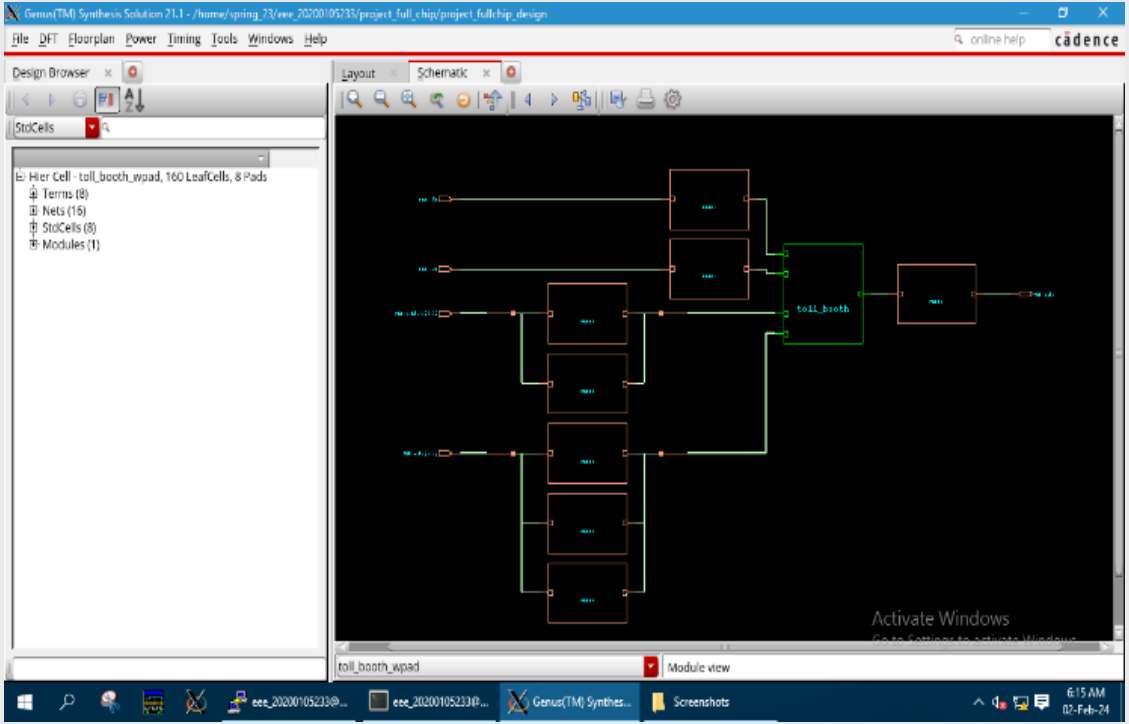
- RTL design in **Verilog** for vehicle classification and toll collection.
- System transitions states based on payment.
- Testbench verifies behavior and functionality.
- Ensures accurate toll collection for each vehicle.



4: Methodology Overview





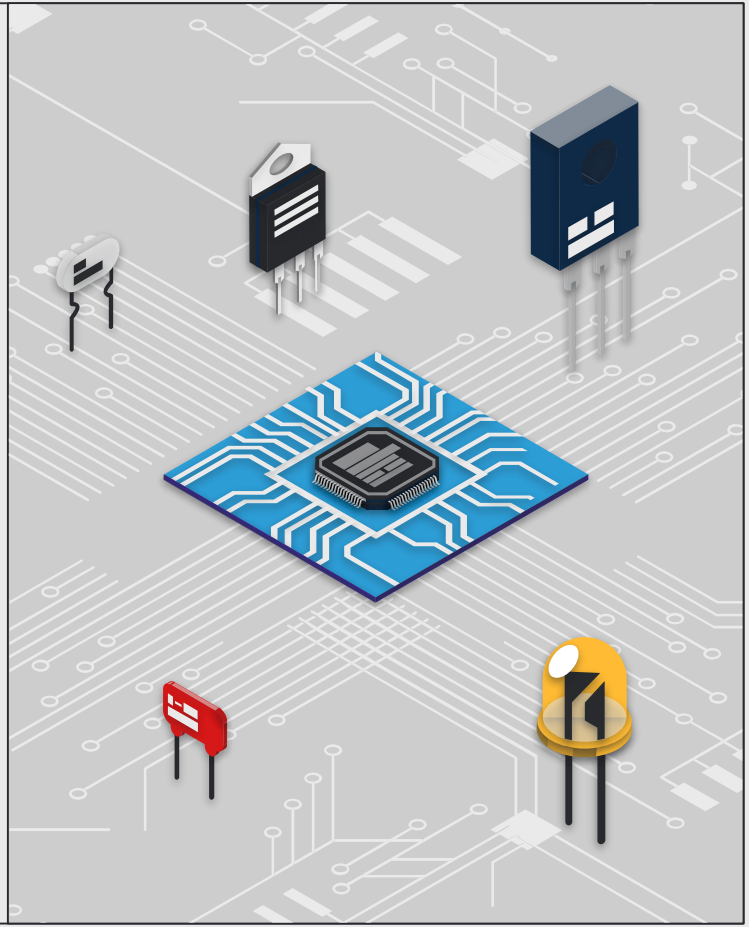


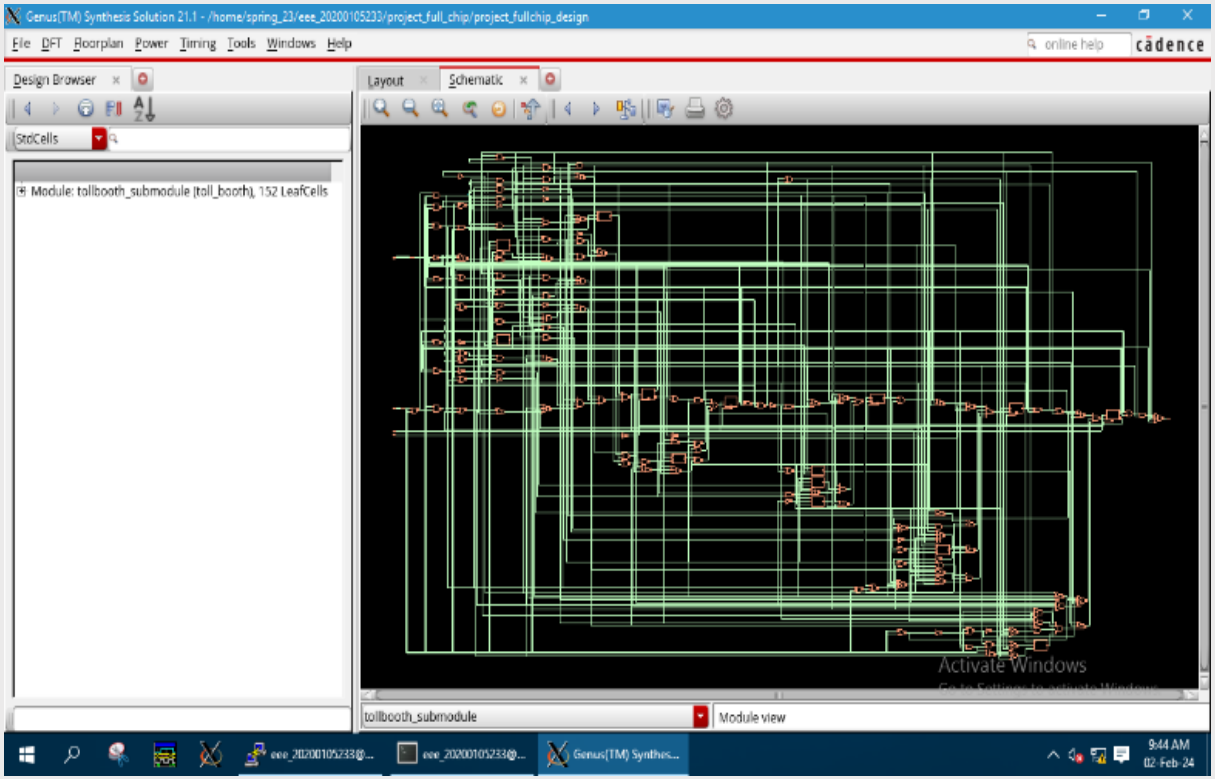
5: Modified RTL Design

- Modified RTL design introduces pad cells for communication between **internal logic** and **external interfaces** (power, ground, signal I/O).
- **Pad cells** ensure reliable electrical connections and protect internal circuits.

6: Set Constraints

- System follows SDC (Standard Design Constraints) for performance and timing.
- Clock frequency: 200 MHz for high-speed operation.
- Maximum transition time: 0.7 ns to prevent glitches.
- Driving cell: BUFX4 for strong signal drive.
- Input delay: 2 ns
- Output delay: 2.5 ns.
- Maximum fanout: 9 to maintain timing integrity.



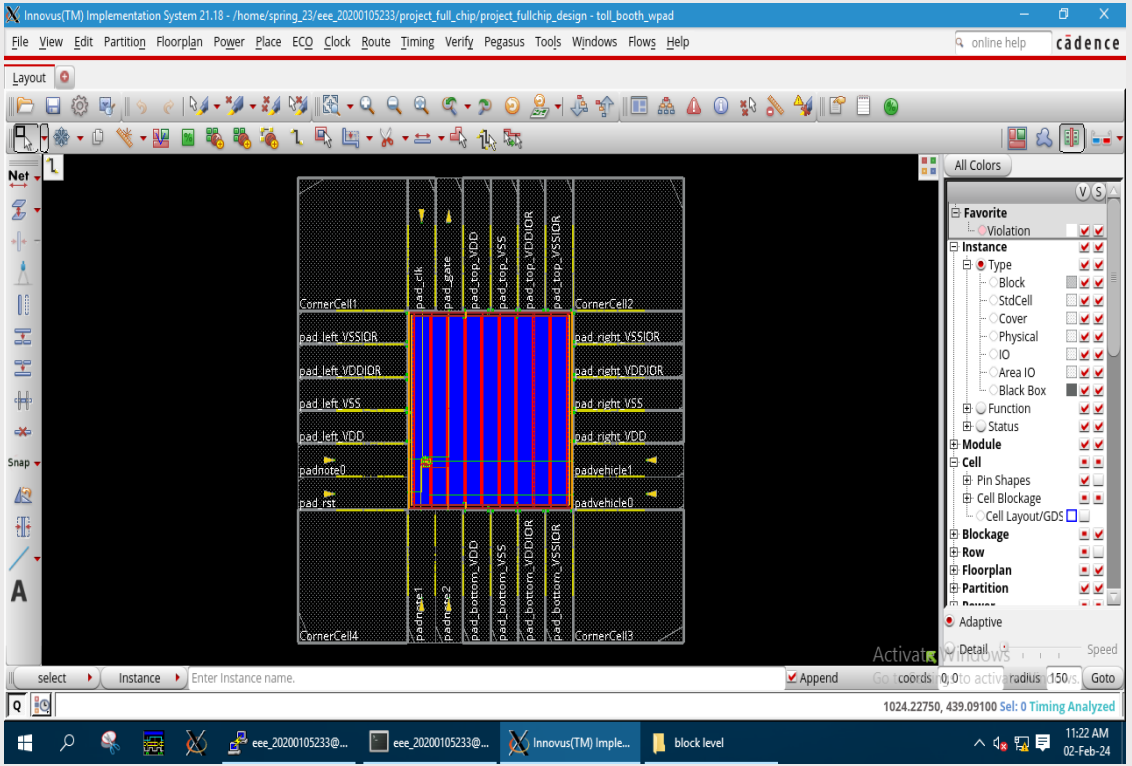


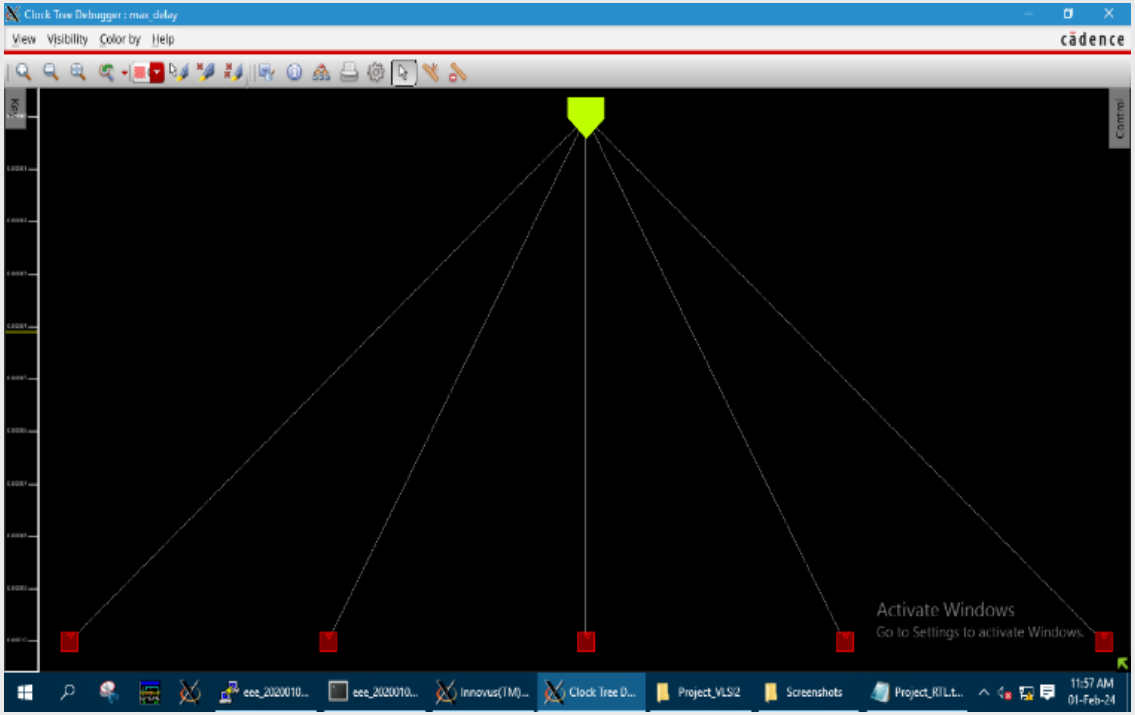
7: Synthesis

- RTL code for vehicle classification and toll collection is synthesized into a gate-level netlist.
- Tools like **'Cadence Genus'** convert Verilog into logic gates forming the chip's functional blocks.

8: Floor planning, Power Planning & Cell Placement

- Physical layout planning ensures performance goals while minimizing area.
- Power planning ensures efficient power distribution and reliability.
- Power and ground rails provide stable power to all chip parts.
- Cell placement arranges logic gates to minimize signal delay and maximize performance.
- Design meets area and power constraints.



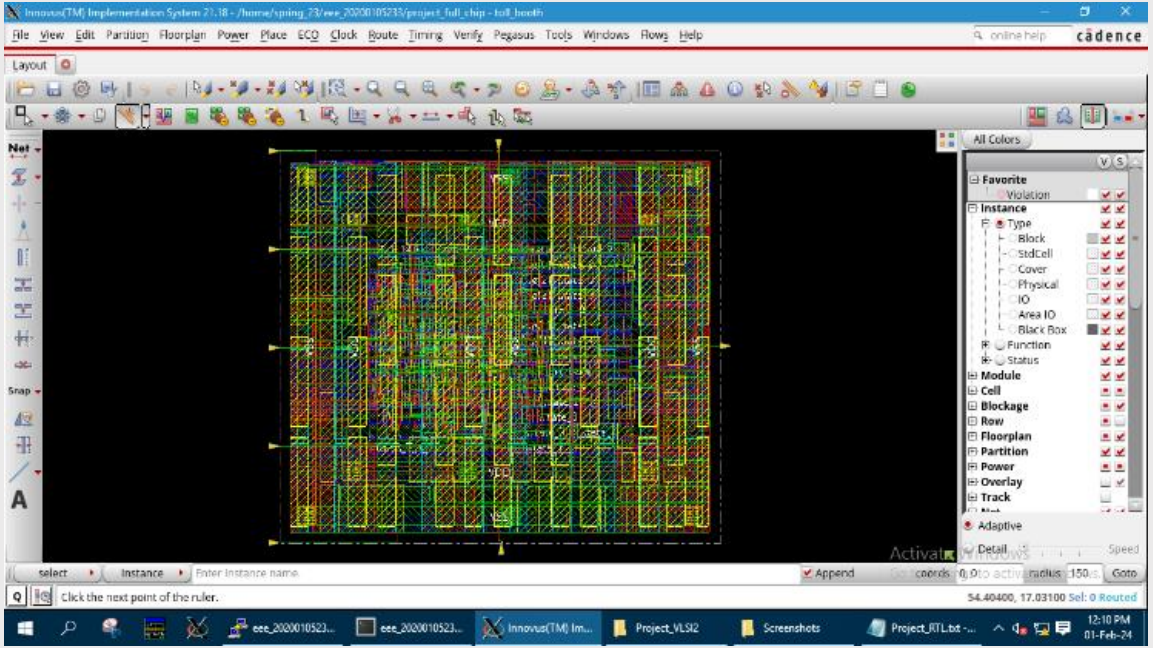


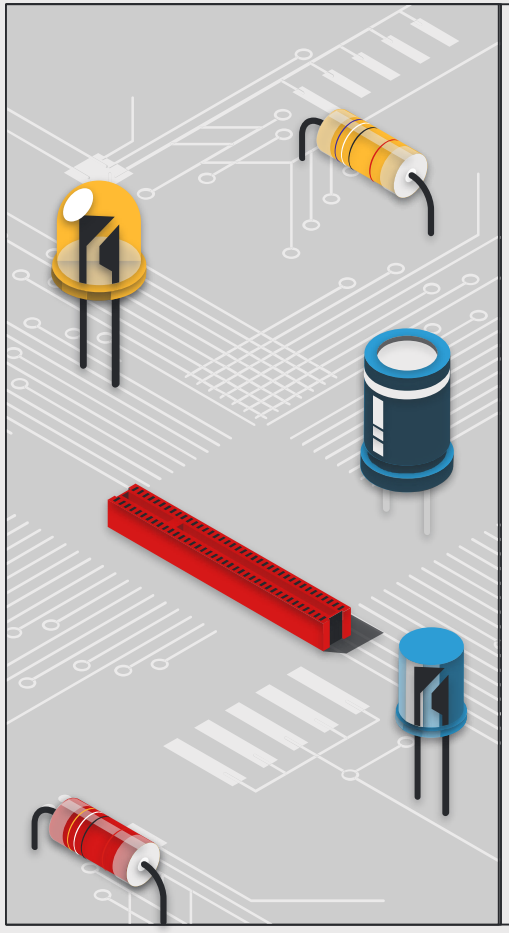
9: Clock Tree Synthesis (CTS)

- Clock Tree Synthesis (CTS) distributes the **clock signal** across the chip.
- Goal: Minimize clock skew and **ensure simultaneous clock signal** delivery to all parts.

10: Routing & Metal Filler

- Routing connects placed cells with metal wires to establish signal paths.
- Ensures physical connections between logic gates, clock signals, and power supplies.
- Design meets timing, power, and area constraints.
- Metal fillers are added to maintain uniform metal density and prevent fabrication issues.





11: Physical Verification

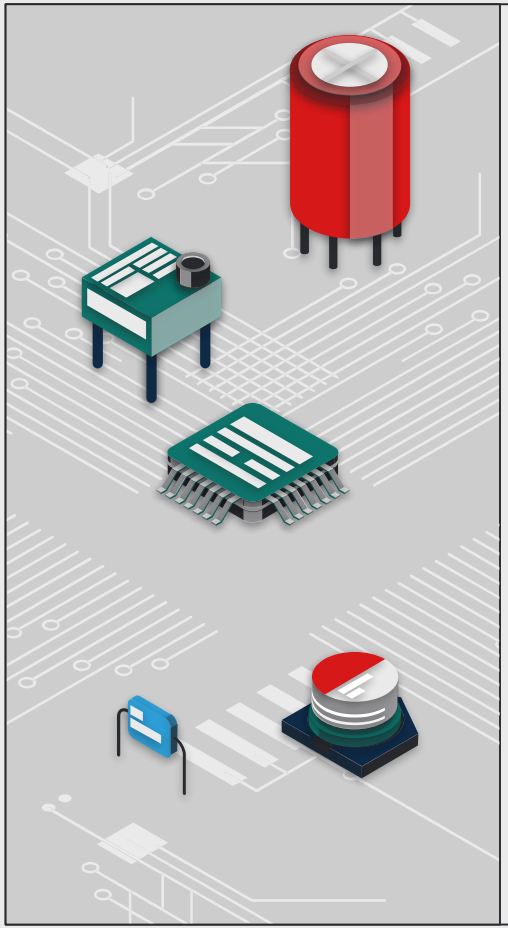
- Physical verification ensures chip manufacturability and functionality.
- Design Rule Check (DRC) confirms proper layout spacing and dimensions.
- Connectivity verification ensures no open or short circuits.
- Process Antenna Checks prevent fabrication damage.
- Power/Ground Short Checks ensure no shorts in power/ground networks.
- Power Via and Stacked Via Verification ensure correct placement and current capacity.
- These steps ensure the chip is ready for reliable fabrication.

12: Final Design

13: Result Parameters

- Final design achieved 100% density, efficiently utilizing available space.
- 329 cells placed, with zero DRC violations and no power/ground shorts.
- Power via and stacked via checks showed no issues.
- Design is well-optimized and ready for final submission.

Parameter	Value
Final density	100%
Total placed cells	329
DRC Violations	0 violation.
PG Short	0 short.
Power Via	No problem found.
Stacked Via	No problem found.



14: Drawbacks

- **No refund mechanism** for overpayments.
- **Inefficient power** consumption.
- **Limited scalability** for larger traffic volumes.
- **Timing performance issues** with complex toll mechanisms.

15: Future Enhancements

Enhance system with **RFID** for cashless, contactless toll payments, reducing wait times.

Implement dynamic toll pricing based on **real-time traffic conditions** for better revenue and traffic management.

Expand system coverage to include **more vehicle types** and **centralize toll booth monitoring** and data analytics.

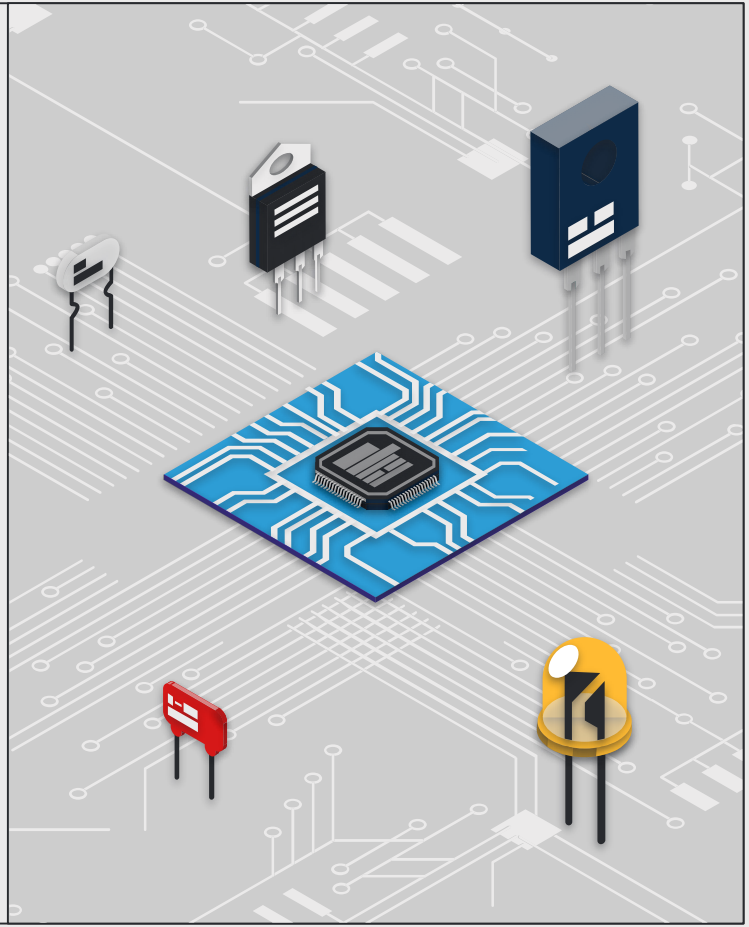
15: Future Enhancements

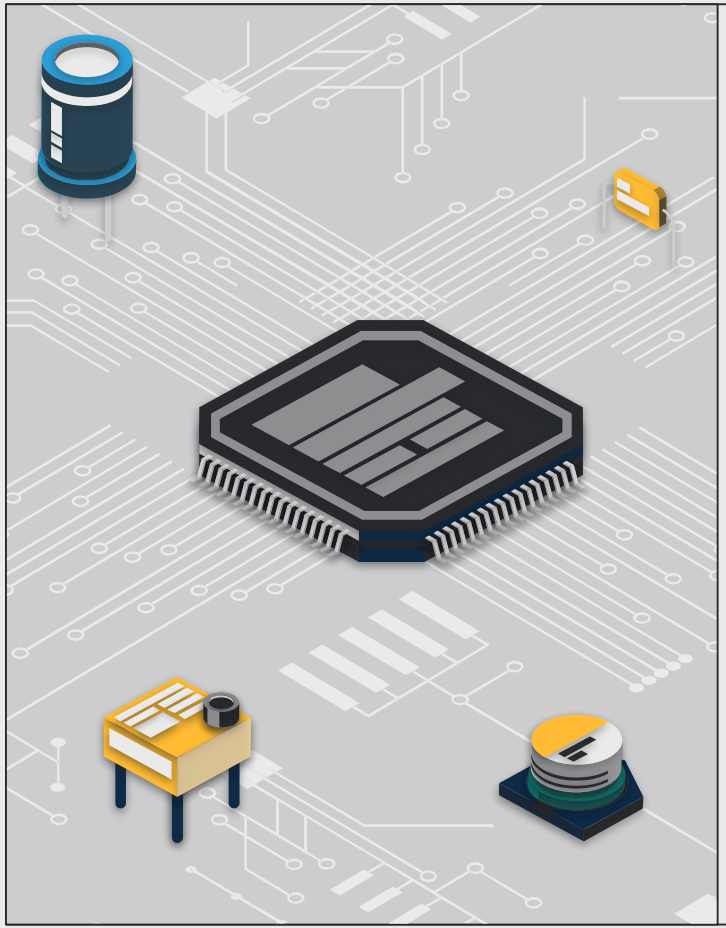
Improved system will be **versatile**, user-oriented, and resourceful.

Integrate mobile payment options for seamless transactions via **smartphones** or **digital wallets**.

CONCLUSION

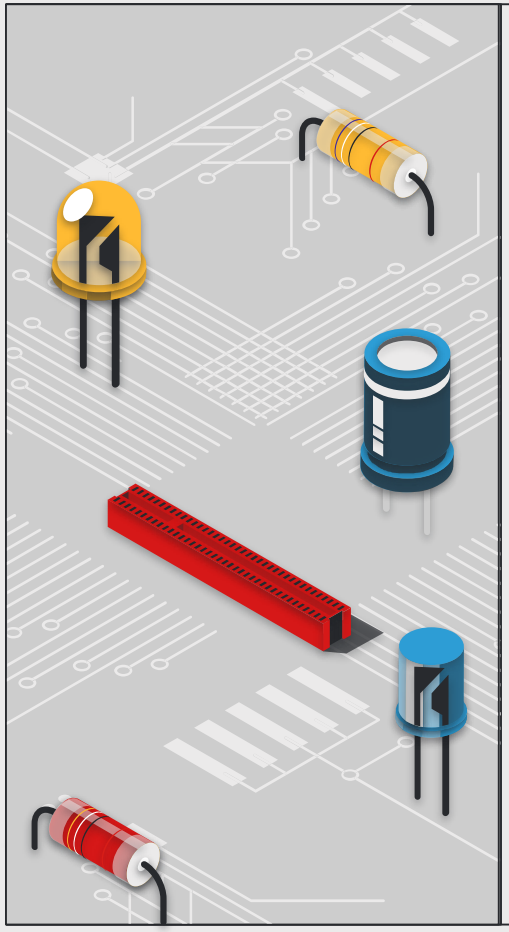
The automated toll booth system efficiently handles toll collection and vehicle classification with minimal human input using a state machine model. Optimized through RTL design, synthesis, and verification checks, it is ready for real-world use. Though efficient, enhancements like RFID for contactless payments, dynamic pricing, and refund mechanisms would improve user experience and power efficiency. Overall, the project demonstrates a functional IC chip that meets modern toll booth needs.





"Innovation is the ability to see change as an opportunity, not a threat."

– Steve Jobs



Thanks!