Full Chip Design of Automated Toll Booth System

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***Abstract*— This study explains the construction and operation of a completely fully automated toll booth system aimed at reducing congestion on highways and improving the processes of toll administration. The system employs a state machine classification model to place vehicles into categories such as private cars, large vehicles, buses and bikes, all of which have distinct toll attributes. The automated tolling system uses the classification of vehicle types to ascertain the appropriate toll fee that adjoins easy state transitions and makes sure tolls are collected before access to the road is permitted. RTL design and verification were carried out, then proceeded to modular block level design and test to ensure the process worked without any bugs or defects. Full chip design was done employing primary tools such as Quartus Prime II for RTL and testbench creation, Cadence Genus for synthesis and Cadence Innovus for physical design and optimization. There are improvements in the efficiency, accuracy, expandability, and security of the system in the tolling process.**

Keywords*— *Automated toll booth, Vehicle classification, State machine model, RTL design, Synthesis, Physical design.

I. METHODOLOGY

The design and implementation of the automated toll booth system follow a structured methodology encompassing various stages, from design specifications to full chip integration, as shown in the Figure I. The primary goal was to create an efficient and scalable system for vehicle classification and toll collection with minimal human intervention.

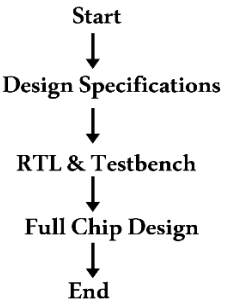


Figure I: Work-Flow diagram of automated toll booth system.

- *Design Specifications*

The automated toll booth system has several design specifications as per the expenditure of each vehicle type with respect to payment evolution categories for Bangladeshi Taka (BDT). This system charges for the different vehicle types as follows; bike type 30 BDT, private car type 50, large car type 80 and bus or truck type 100 BDT. The system is as well modeled using the state machine to ensure the tolls are collected appropriately. Each of the vehicle types has to go through the rotating system of states pattern depending on the amount of money paid, which again can only be in 10, 20, 50, or 100 BDT increments.

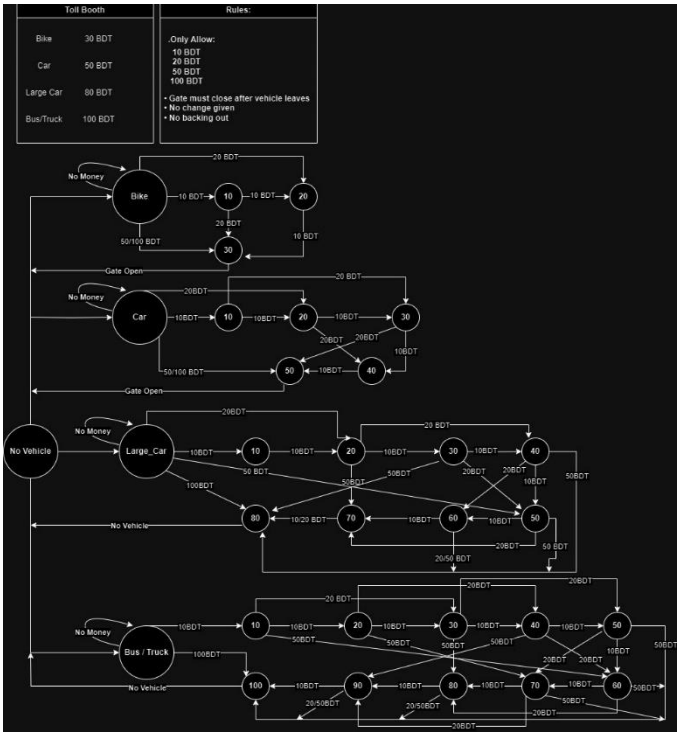


Figure II: FSM diagram of automated toll booth system.

In Figure II FSM (Finite State Machine) diagram integrates the full working of the process for each vehicle type. For example, if a bike arrives at the toll booth, the system expects payment of 30 BDT. This can be achieved with a combination of 10 and 20 BDT payments. Similarly, for a car, 50 BDT is required, and for larger vehicles or buses, payments are made in stages depending on the total required toll. The FSM ensures that the toll booth gate only opens when the correct amount is collected, and it does not allow underpayment or change issuance. The system is also designed to close the gate after the vehicle leaves to ensure security and prevent toll evasion. The state transitions are determined by the amount paid, and the system moves to a "Gate Open" state once the total toll amount is collected.

- *RTL & Testbench Design:*

Register Transfer Level (RTL) design is implemented in Verilog where describe the logic of the system responsible for vehicle classification and toll collection. Each vehicle type has its specific states, and the system transitions through states depending on the payment received. A testbench is created to verify the system's behavior, ensuring that the design function works perfectly. The testbench verifies state transitions, ensuring accurate toll collection for each vehicle category.

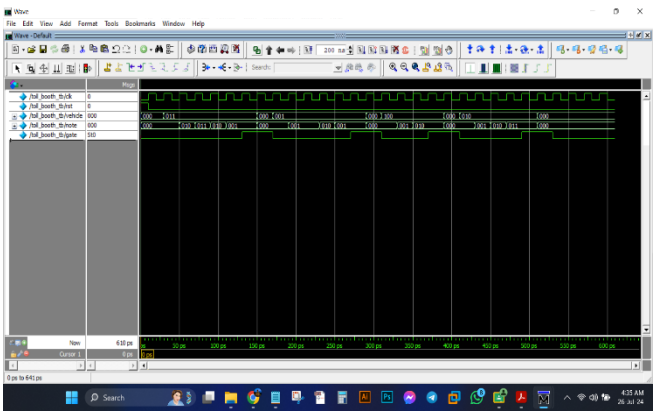


Figure III: Testbench results for check functionality.

- *Full chip design:*

Full chip design of the automated toll booth system follows a comprehensive and well-defined structure. The design flow encompasses several critical stages and each contributing to the functionality for better performance and reliability of the final chip. These stages are outlined as follows:

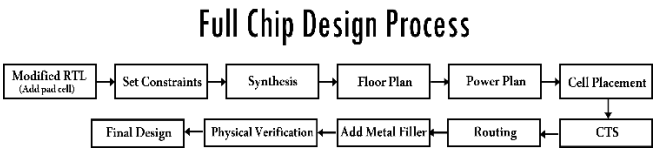


Figure IV: Full chip design process.

A. *Modified RTL*

In the modified RTL design for the automated toll booth system, pad cells are introduced to facilitate communication between the internal chip logic and external interfaces such as power, ground, and signal I/O. Pad cells play a crucial role in interfacing the core logic of the chip with the outside world and ensuring reliable electrical connections and protection for the internal circuits.

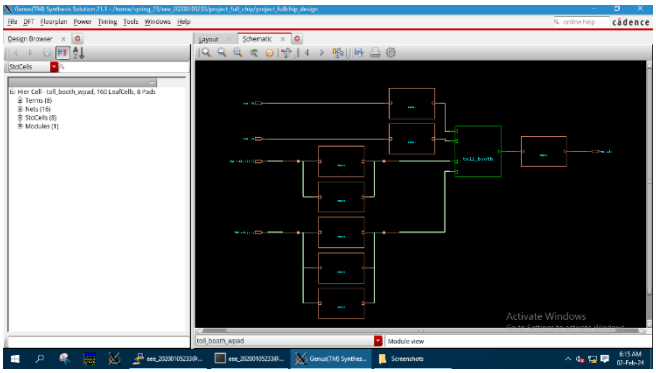
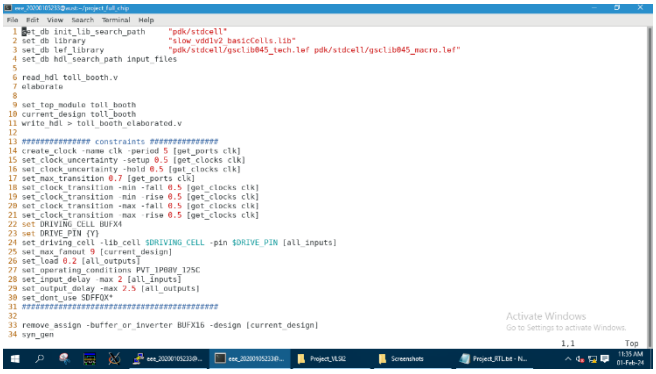


Figure V: Add Pad Cell in Design.

B. *Set Constraints*

Our system follows specific SDC (Synopsys Design Constraints) to meet performance and timing goals. The clock frequency is 200 MHz to ensure high-speed operation. A maximum transition time of 0.7 ns limits signal changes to prevent glitches. The driving cell chosen is BUFX4, ensuring strong signal drive. Input delay is set to 2 ns, and output delay to 2.5 ns to manage signal propagation times. The maximum fanout is 9 to control loading and maintain timing integrity. These constraints are necessary for performance and reliability.



```
set_db init_lib_search_path      "pdk/stdcell"
set_db library                   "slow_vdd1v2_basicCells.lib"
set_db lef_library               "pdk/stdcell/gsclib045_tech.lef pdk/stdcell/gsclib045_macro.lef"
set_db hdl_search_path input_files

read_hdl toll_booth.v
elaborate

set_top_module toll_booth
current_design toll_booth
write_hdl > toll_booth_elaborated.v

############### constraints ###############
create_clock -name clk -period 5 [get_ports clk]
set_clock_uncertainty -setup 0.5 [get_clocks clk]
set_clock_uncertainty -hold 0.5 [get_clocks clk]
set_max_transition 0.7 [get_ports clk]
set_clock_transition -min -fall 0.5 [get_clocks clk]
set_clock_transition -min -rise 0.5 [get_clocks clk]
set_clock_transition -max -fall 0.5 [get_clocks clk]
set_clock_transition -max -rise 0.5 [get_clocks clk]
set DRIVING_CELL BUFX4
set DRIVE_PIN {Y}
set_driving_cell -lib_cell $DRIVING_CELL -pin $DRIVE_PIN [all_inputs]
set_max_fanout 9 [current_design]
set_load 0.2 [all_outputs]
set_operating_conditions PVT_1P08V_125C
set_input_delay -max 2 [all_inputs]
set_output_delay -max 2.5 [all_outputs]
set_dont_use SDFFQX*
###########################################
remove_assign -buffer_or_inverter BUFX16 -design [current_design]
syn_gen
```

Figure VI: Set SDC. (Synopsys Design Constraints)

C. *Synthesis*

The RTL code that implements the system and control logic for vehicle classification and toll collection is first synthesized into a gate-level netlist using tools such as 'Cadence Genus'. This process converts the high-level Verilog description into actual logic gates that form the functional blocks of the chip.

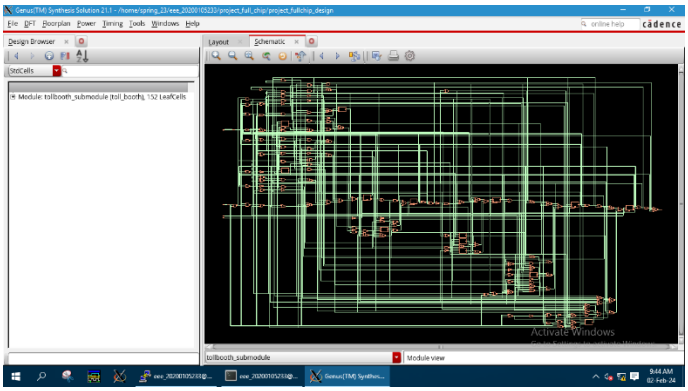


Figure VII: Synthesis Result of the system.

D. *Floor planning, Power Planning & Cell Placement*

In this phase, the physical layout of the chip is planned. Proper floor planning is crucial to ensure that the chip meets performance goals while minimizing area usage. Power planning in the full chip design ensures efficient distribution of power across the chip while minimizing power loss and ensuring reliability. It involves creating power and ground rails that deliver a stable power supply to all parts of the chip. In cell placement, where synthesized logic gates (cells) are arranged within the predefined floorplan. The objective is to place cells in an optimized manner that minimizes signal delay and maximizes performance, while also ensuring the design meets area and power constraints.

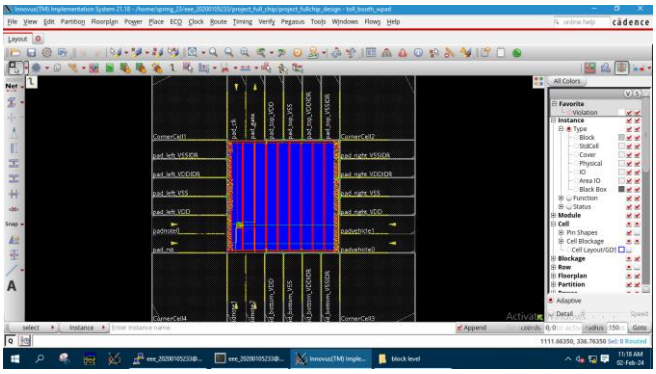


Figure VIII: Floor Planning, Power planning & Cell Placement.

E. *Clock Tree Synthesis (CTS)*

Clock Tree Synthesis (CTS) is performed to distribute the clock signal efficiently across the chip. The goal of CTS is to minimize clock skew and ensure that the clock signal reaches all parts of the chip simultaneously.

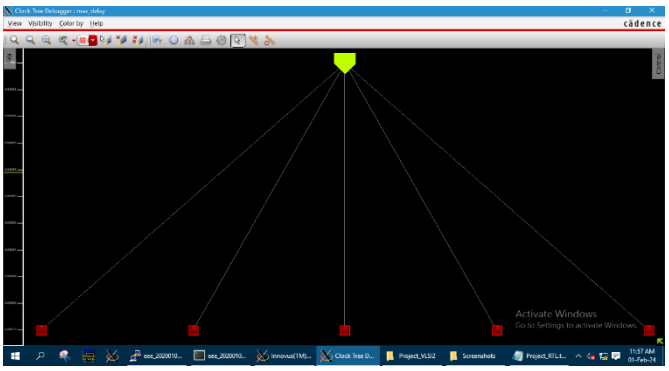


Figure IX: Clock Tree Synthesis (CTS) of system.

F. *Routing & Metal Filler*

Routing is the process of connecting the placed cells with metal wires to establish the signal paths required for communication within the chip. During this step, the physical connections between logic gates, clock signals, and power supplies are made, ensuring the design meets timing, power, and area constraints. After routing, metal fillers are added to maintain a uniform metal density across the chip. These filler cells are placed in empty spaces between wires to prevent issues like uneven etching or metal thinning during the fabrication process.

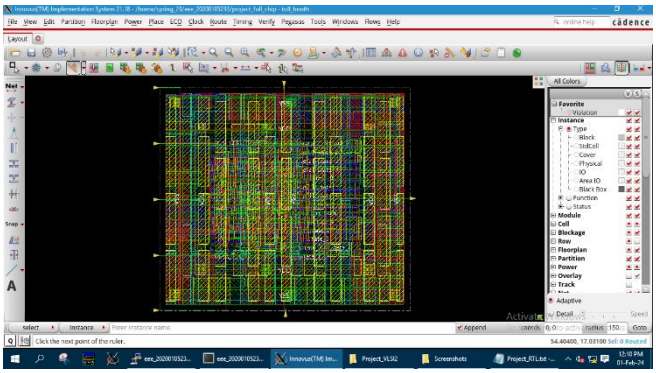


Figure X: After routing and add metal filler.

G. *Physical Verification*

In the physical verification phase, several key checks were performed to ensure the chip's manufacturability and functionality. Design Rule Check (DRC) verified that the layout adhered to the foundry's rules, ensuring proper spacing and dimensions. Connectivity verification confirmed that all connections were correctly routed with no open or short circuits. Process Antenna Checks were conducted to prevent damage during fabrication by detecting potential antenna effects. Power/Ground Short Checks ensured there were no shorts between power and ground networks. Power Via Verification validated the correct placement of via, ensuring adequate current-carrying capacity, while stacked via verification checked that stacked via were correctly placed to maintain the integrity of vertical connections. These steps collectively ensured that the chip design was ready for fabrication with reliability and robustness.

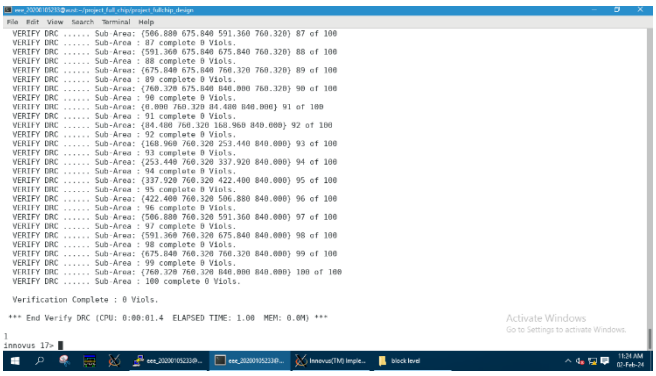


Figure XI: Verify DRC.

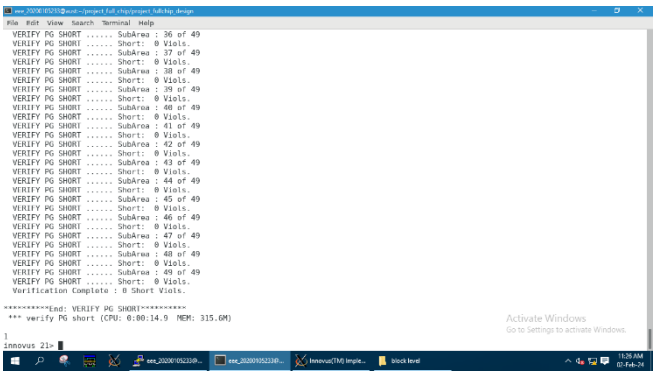


Figure XII: Verify PG Short.

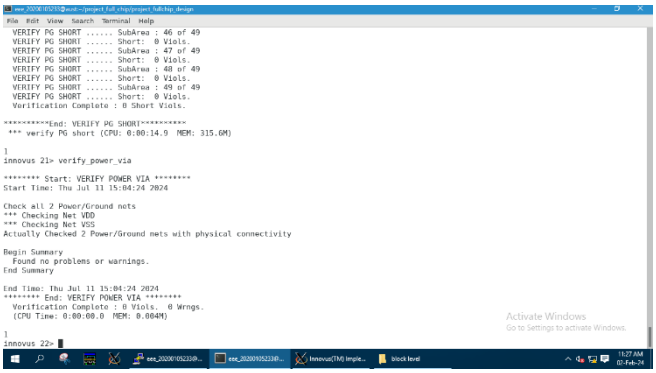


Figure XIII: Verify Power Via.

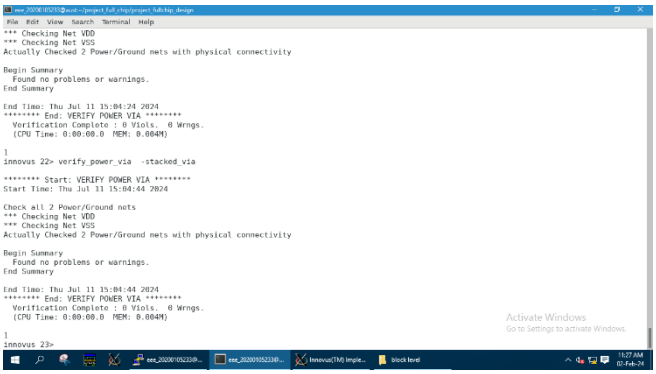


Figure XIV: Verify Stacked Via.

H. Final Design

After completing all the design steps, including synthesis, placement, routing, clock tree synthesis, power planning, and physical verification, the final chip design is ready for submission. The entire design is converted into 'GDSII' (Graphic Database System II) format. GDSII is the standard format used for transferring the physical design to the foundry for manufacturing. Once the design is converted to GDSII, it undergoes a final check to ensure that it meets all design specifications, and then the file is submitted to the foundry for tape-out and eventual production.

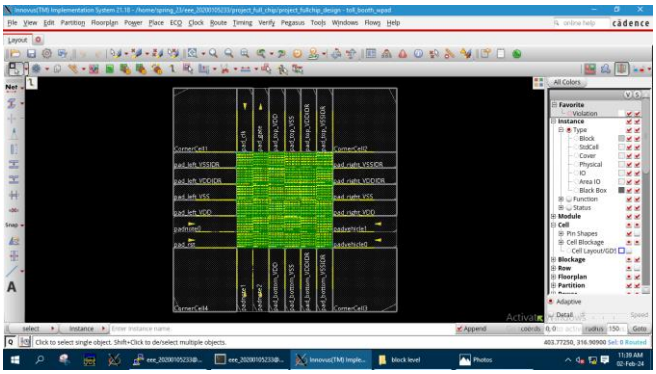


Figure XV: Final Design.

II. Result Analysis

Figure XVI represents the functionality of the system. The clock signal synchronizes state transitions, and the reset signal resets the FSM when activated. The 3-bit vehicle signal represents different vehicle types: 000 for no vehicle, 001 for a car, 010 for a large car, 011 for a bus/track, and 100 for a bike. Similarly, the note signal represents payment amounts: 000 for no payment, 001 for 10 BDT, 010 for 20 BDT, 011 for 50 BDT, and 100 for 100 BDT. The gate signal, which controls whether the toll gate opens or stays closed, is based on whether the correct payment threshold is met for each vehicle type. For example, the waveform shows the state changes for different vehicles and payments, ensuring that the gate opens only when the necessary toll amount is paid (e.g., 50 BDT for a car, 80 BDT for a large car, etc.). The figure summarizes the operation of the FSM, including the encoding for vehicles and payments, as well as the conditions for opening the gate.

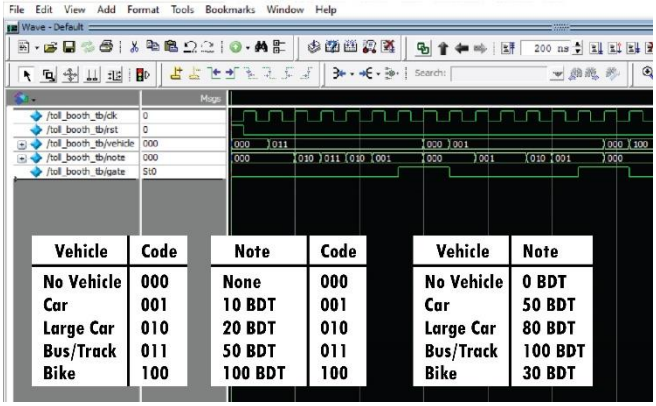


Figure XVI: Functionality analysis.

In Figure XVI, for example, no vehicle is present (`vehicle = 3'b000`), but then a bus arrives (`vehicle = 3'b011`). The bus begins inserting money, first 20 BDT (`note = 3'b010`), followed by 50 BDT (`note = 3'b011`), then another 20 BDT (`note = 3'b010`), and finally 10 BDT (`note = 3'b001`). This sequence of payments simulates the bus making incremental payments, and once the correct total is inserted, the gate is open, allowing the bus to pass. The testbench monitors the `gate` signal to ensure the system responds correctly after the full payment is made.

Table I summarizes the key results of the verification process. The final design achieved 100% density, meaning all available space was efficiently utilized. A total of 329 cells were placed, and the verification process reported zero DRC violations and no power/ground shorts, indicating that the design adheres to manufacturing rules. Additionally, the checks for power vias and stacked vias showed no issues, confirming that the power distribution network and vertical connections between layers are robust and free from errors. This indicates the design is well-optimized and ready for further steps toward final submission

Table I: Result Parameters.

Parameter	Value
Final density	100%
Total placed cells	329
DRC Violations	0 violation.
PG Short	0 short.
Power Via	No problem found.
Stacked Via	No problem found.

The final design is highly optimized and ready for tape-out with strong reliability and manufacturability.

III. Future Enhancements and Key Areas for Improvement

- *Future Enhancements*

Further enhancements in the automated toll booth system should include the usage of RFID technology which enables non cash, non-contact and hassle free toll counter usage thus reducing customers waiting time and making the users experience more interesting. Furthermore for maximizing revenue as well as proper management of traffic dynamic toll pricing mechanism could be used depending on the existing conditions of traffic which operates in real time. Further advancements might include the widening of entity's coverage to allow more levels of vehicles and centralizing the systems of several toll booths with respect to monitoring and data analytics. More specifically this improved transport would become versatile, user-oriented, as well as resourceful.

- *Areas for Improvement*

One critical area for improvement is the system's lack of a refund mechanism. Currently, there is no option to return excess payments, which could lead to user dissatisfaction. Implementing a refund feature to return overpaid amounts in specific cases, such as incorrect toll payments, is essential for improving user convenience. Additionally, power consumption could be optimized through advanced techniques like clock gating. Timing performance and scalability can be enhanced to support larger traffic volumes and more complex toll mechanisms. Addressing these areas would improve the overall robustness and user-friendliness of the system.

IV. Pictorial Representation

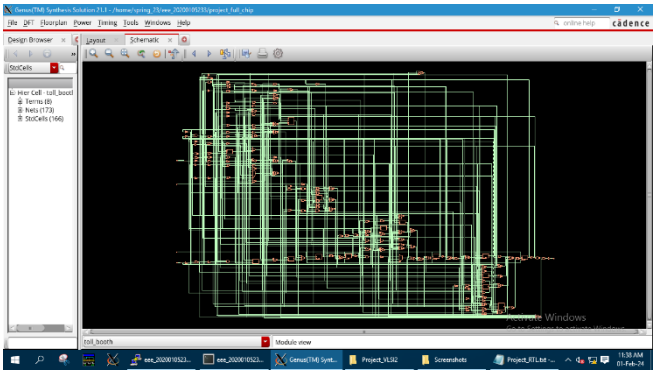


Figure XVI: Synthesis result.

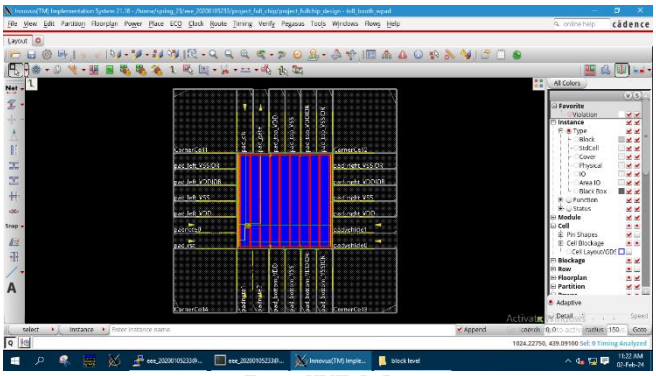


Figure XVII: PnR output.

Figure XVIII: STA reports before violation and cleaning.

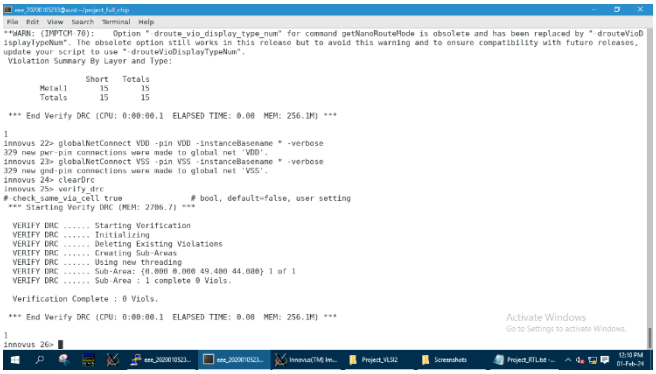


Figure XVIII: STA reports after violation and cleaning.

V. Conclusion

The automated toll booth system designed in this project successfully meets the demands of simultaneous toll collection and vehicle classification. A state machine model for vehicle categorization and calculating toll dues was also implemented, which guarantees that eventually, all payment is collected with very little human participation. The use of RTL design, synthesis and full chip design techniques enabled optimization of the system for performance, power and area on a chip for real application. Important verification procedures such as DRC, power and via checks proved the design to be sound and ready for mass production. Although the existing design is very efficient, improvements in design can be achieved by attaching RFID chips for payment without physical contact and dynamic diagrams imposition of tolls to improve user interaction and operations of the system. Covering aspects such as the mechanism of refunds and enhancement of power requirements will make the system more user oriented and also cater for higher atrocious congestion. All in all, the lessons learnt in this project illustrate an accomplishment of a complete functional IC chip that undertakes the modern day needs of a toll booth application.