Mohammad Nasim Imtiaz Khan

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Summary

• Available for 2018 Fall, 2019 Spring/Summer internship.
• Ph.D. (3^{rd} year) research on efficient circuit design for secured emerging non-volatile memory.
• Experienced in hardware security threats and countermeasures.
• Hands on experience in experimental validation of attack model on commercial/test chip; test chip characterization using Logic Analyzer.
• Patent(s): 2, Book Chapter(s): 2, Journal(s): 3, Conference Paper(s): 10.

Education

Pennsylvania State University, University Park, USA *August 2016 - December 2019*
Ph.D. Candidate in EECS. Specialization: NVM design & security.
CGPA 3.87/4.00. Advisor: Prof. Swaroop Ghosh.

University of South Florida, Tampa, USA (Transfer) *January 2016 - August 2016*
Ph.D. Candidate in CSE. CGPA 4.00/4.00.

Bangladesh University of Engineering & Tech. (BUET), Dhaka, Bangladesh *July 2014*
B.Sc. in EEE. Graduated with honors; CGPA 3.85/4.00.

Technical Skills & Strengths

- **Circuit Simulation/Device Modeling:** HSPICE, Cadence Virtuoso, Sentaurus, QuantumWise.
- **FPGA Design:** XILINX (ISE and Vivado), ALTERA (Quartus).
- **Hardware Description Language:** VHDL, Verilog.
- **Numerical Analysis, DSP and Modeling:** MATLAB.
- **Programming Languages:** C, Python, Assembly.

Work Experience

Pennsylvania State University, University Park, USA *August 2016 - Present*
Research Assistant

- Proposed homogeneous IoT architecture resilient against data corruption attack.
- Experimental validation of Side Channel attack and Row Hammer attack on emerging non-volatile memory interfaced with FPGA.
- Patent(s): 1, Book Chapter(s): 2, Journal(s): 2, Conference Paper(s): 6.

University of South Florida, Tampa, USA *January 2016 - August 2016*
Research Assistant

- Analysis of Magnetic attack and Thermal attack on spintronic memory.
- Proposed novel nano-shielding against Magnetic attack.
- Patent(s): 1, Conference Paper(s): 1.

Daffodil International University, Bangladesh *June 2015 - December 2015*
Lecturer, Electrical and Electronic Engineering
Instructed theory and lab on Microprocessor and Interfacing undergrad course.

Halliburton Int. Inc., Bangladesh *September 2014 - June 2015*
Associate Maintenance Professional
Debugged and solved hardware failure of sophisticated oil/gas down-hole survey tools.

Samsung R&D Institute, Bangladesh *October 2013 - January 2014*
Intern
Worked on White-box and Black-box testing of commercial software designed for Windows operating system.

Research Experience

- **Multi-bit Write/Read in RTD-MTJ Crossbar Array,** Funded by SRC-NSF, 2017 – 18:
  - Proposed RTD-MTJ crossbar array capable of writing/reading multiple bits simultaneously. Achieved $2X$ bandwidth, $1.5X$ area improvement.
- **Energy/Area Efficient Amplifier with RRAM (Design & Layout),** 2017 – 18:
  - Implementing RRAM based ECG detector with 8-bit Analog to Digital Converter using $0.5\mu m$ technology.
- **Side Channel Analysis of Emerging Memories,** Funded by SRC-NSF, 2017:
  - Extracted full 16 byte key from STTRAM and SRAM exploiting side channel signature.
  - Validated proposed attack on MRAM chip experimentally (extracted first byte of key in only 15 traces).
- **Row Hammer Attack on STTRAM,** Funded by SRC-NSF, 2017:
  - Launched Row Hammer attack to corrupt stored data exploiting ground bounce.
  - Observed $130mV$ ground bounce from $1T-1R$ test chip (STTRAM realized with resistance).
- **Charge-Trap Based Camouflaged Gates for Reverse Engineering Prevention,** Funded by DAPRA , 2017:
  - Proposed Charge-Trap based camouflaged gate resilient to backside probing and optical reverse engineering.
- **Novel Magnetic Burn-In for Retention & Magnetic Tolerance Testing of STTRAM,** Funded by SRC-NSF, 2016:
  - Achieved 1.97x10^{14}X retention test time reduction at 220Oe and 125°C with a novel magnetic burn-in.

Selected Publications

[$P1$] **M. N. I. Khan**, et. al., "Row Hammer Attack on STTRAM", September, 2017. (Patent filed)
[$P2$] S. Ghosh, **M. N. I. Khan**, et. al., "Strap Region Exploit Mu-Metal Nano-Shielding from Magnetic Field Attack on STTRAM", **U.S. Patent** Application 62/450,796, January, 2017. (Patent Pending)
[$B1$] R. Govindaraj, **M. N. I. Khan**, et. al., "Spin-Torque-Transfer RAM and Domain Wall Memory Devices", Security Opportunities in Nano Devices and Emerging Technologies, To appear in **CRC Press**, December, 2017.
[$J1$] **M. N. I. Khan**, et. al., "Novel Magnetic Burn-In for Retention and Magnetic Tolerance Testing of STTRAM", **TVLSI**, 2018.
[$J2$] A. De, **M. N. I. Khan**, et. al., "Replacing eFlash with STTRAM in IoTs: Security Challenges and Solutions", **HASS**, 2017.
[$C1$] **M. N. I. Khan**, et. al., "Fault Injection Attacks on Emerging Non-Volatile Memories", **HASP**, 2018.
[$C2$] **M. N. I. Khan**, et. al., "Information Leakage Attacks on Emerging Non-Volatile Memories", **ISLPED**, 2018.
[$C3$] A. De., A. Iyengar, **M. N. I. Khan**, et. al., "CTCG: Charge-Trap Based Camouflaged Gates for Reverse Engineering Preventions", **HOST**, 2018.
[$C4$] **M. N. I. Khan**, et. al., "Test Challenges and Solutions of Emerging Non-Volatile Memories", **VTS**, 2018.
[$C5$] **M. N. I. Khan**, et. al., "Side-Channel Attack on STTRAM based Cache for Cryptographic Application", **ICCD**, 2017.
[$C6$] **M. N. I. Khan**, et. al., "Novel Magnetic Burn-In for Retention Testing of STTRAM", **DATE**, 2017.
[$C7$] **M. N. I. Khan**, et. al., "Analysis of Raw Hammer Attack on STTRAM", **TECHCON**, 2017.
[$C8$] S. Ghosh, **M. N. I. Khan**, et. al., "Security and privacy threats to on-chip non-volatile memories and countermeasures", **ICCAD**, 2016.

Honors and Awards

- **Milton and Albertha Langdon Memorial Graduate Fellowship** for 2016 – 17 academic year.
- **Richard Newton Young Fellow Award**, Design Automation Conference (DAC), 2016.
- **Best Presenter Award** in IEEE International Conference on Informatics, Electronics & Visions (ICIEV), 2013.
- 1^{st} (96.1%) in Technical Training Program (TTP), Cairo, Egypt, 2015.
- Luna Worldwide Campaign Award, NASA Fourth Annual Lunabotics Mining Competition, 2013.
- Dean's List Award and University Merit Scholarship, BUET, 2010 – 14.
- 2^{nd} in Physics Olympiad, Notre Dame Science Club, Bangladesh, 2007.

Graduate Courses

Advanced VLSI, Information Security and Privacy, Digital Integrated Circuit, Linear Integrated (Analog) Circuit, Semiconductor Device, Field-Effect Device, Operating System.

Professional Activities

Reviewer of (i) Journal on Emerging Technologies in Computing Systems; (ii) Integration, the VLSI Journal, (iii) Transactions on Architecture and Code Optimization.