MES College of Engineering
Department of Computer Science and Engineering

Assignment 2 - Digital Fundamentals of Computer Architecture (DFCA)

Q4. Draw a single datapath representation for R-type instruction

Introduction:
A datapath is the hardware structure within a CPU that performs arithmetic, logic, and data transfer operations. An R-type instruction in RISC architectures (e.g., MIPS) performs operations between registers such as ADD, SUB, AND, OR.

R-Type Instruction Format:
Opcode (6 bits), rs (5 bits), rt (5 bits), rd (5 bits), shamt (5 bits), funct (6 bits)

Datapath Components Used:
Program Counter (PC), Instruction Memory, Register File, ALU, Control Unit, Multiplexers, Sign Extend.

Operation Steps:
1. Fetch: Instruction fetched using PC.
2. Decode: Registers rs and rt are read.
3. Execute: ALU performs operation as per funct field.
4. Write Back: Result stored in rd.

Control Signals: RegDst=1, ALUSrc=0, RegWrite=1, MemRead=0, MemWrite=0, ALUOp=10.

Diagram Description:
PC → Instruction Memory → Register File → ALU → Write Back

Conclusion:
R-type instructions use only registers, and the datapath executes all operations in a single cycle efficiently.

Q5. With a neat diagram, explain the operation of DMA controllers in a computer system

Introduction:
Direct Memory Access (DMA) allows peripherals to transfer data directly to/from main memory without CPU involvement, improving performance.

Need for DMA:
Without DMA, CPU must move each byte manually. DMA automates this, freeing CPU resources.

Components:
DMA Controller, Address Register, Count Register, Control Logic, Data Bus Interface, Interrupt Line.

Operation Steps:
1. CPU initializes DMA with source, destination, and count.
2. Device sends DMA Request (DREQ).
3. DMA Controller requests bus from CPU (BR/BG).
4. Data transferred directly between I/O and memory.
5. DMA sends interrupt upon completion.

Modes of Operation:
- Burst Mode
- Cycle Stealing Mode
- Transparent Mode

Diagram Description:
I/O Device ↔ DMA Controller ↔ Memory ↔ CPU

Advantages: Faster data transfer, low CPU overhead.
Disadvantages: Complex hardware.

Conclusion:
DMA controllers enhance data transfer efficiency and system throughput by bypassing CPU during large transfers.

Q6. How should two or more simultaneous interrupt requests be handled? Explain with figure.

Introduction:
When multiple devices send interrupts simultaneously, the CPU must determine which to handle first. This is achieved through interrupt priority mechanisms.

Types of Interrupts:
- Maskable Interrupts
- Non-Maskable Interrupts

Methods for Handling Multiple Interrupts:
1. Software Polling: CPU checks devices sequentially; slow but simple.
2. Hardware Priority (Vectored Interrupts): Each device has fixed priority and sends interrupt vector directly to CPU.
3. Daisy Chaining: Devices connected serially; highest priority device nearest CPU captures acknowledgment first.
Diagram Description:
CPU ← Device 1 ← Device 2 ← Device 3 (priority order)

4. Priority Encoder: Circuit encodes highest-priority request when multiple signals are active.

Conclusion:
Simultaneous interrupt requests are resolved using software or hardware priority methods such as daisy chaining or vectored interrupts to ensure efficient service and system reliability.