Hardware Synthesis Lab
First semester/ 2021
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Skill Test

Part I

Answer the following questions. You may typeset your answers and draw pictures. No hand-writing is accepted. The solution must be submitted in and only in PDF.

1. (2 pt.) Briefly explain the difference between wire (net) and reg in VerilogHDL.
2. (2 pt.) Briefly explain the difference between blocking assignment and non-blocking assignment.
3. (2 pt.) Give at least two benefits of applying time-division multiplexing in your design.
4. (2 pt.) What is a parameter in VerilogHDL? Why is it useful for reusing a component? Please explain.
5. (4 pt.) What is a procedural assignment (e.g always) block? Why is it possible to have more than one *always* block in a VerilogHDL module. Please explain.
6. (4 pt.) What is a bounce? Please create a simple finite state machine that will debounce a switch in VerilogHDL.
7. (4 pt.) Please design an 8-bit 4:1 multiplexor by using a case statement in VerilogHDL.

Part II

(10 pt) Please design and implement the following circuit using VerilogHDL and demonstrate the system on our class FPGA board (BASYS 3). The circuit must show your birthday on a 4-digit 7-segment display. Suppose that your birthday is January 5, 2004. The fist cycle must show 01.05. (MM.DD.). After one second, the second cycle must show 2004. (YYYY.) Do not forget to show the dots at the end of each part.

Please submit a video of your implementation (less than 5 minutes). The video must show your modular design, the simulation, and the synthesis. In particular, show how do you create clock for TDM (about 1/15 second) and for the main state machine (1 second)