

\$40	(read_n / write)	ID 508 ID 504	MSX2+ FS-A1 Series MSX++ Computers and Compatibles	Z80B 5.37MHz OCM-PLD v2.4 or later
\$41	(read_n / write)	BIT 0	Smart Command ID (see the table on the right)	CPL or \$FF (null)
		BIT 1		
		BIT 2		
		BIT 3		
		BIT 4		
		BIT 5		
		BIT 6		
\$42	(read / write_n)	BIT 7		
		BIT 0	CPU Clock	Virtual DIP-SW1
		BIT 1	Video Output (MSB)	Virtual DIP-SW2
		BIT 2	Video Output (LSB)	Virtual DIP-SW3
		BIT 3	Cartridge Slot-1	Virtual DIP-SW4
		BIT 4	Cartridge Slot-2 (MSB)	Virtual DIP-SW5
		BIT 5	Cartridge Slot-2 (LSB)	Virtual DIP-SW6
\$43	(read / write_n)	BIT 6	Current Mapper Size	Virtual DIP-SW7
		BIT 7	Current MegaSD Mode	Virtual DIP-SW8
		BIT 0	Lock Mask of the Toggles	CPU Clock
		BIT 1		Video Output
		BIT 2		Audio Mixer & SCRLK
		BIT 3		Cartridge Slot-1
		BIT 4		Cartridge Slot-2
		BIT 5		System Reset
BIT 6	Internal Mapper			
\$44	(read / write_n)	BIT 7		Internal MegaSD
		BIT 0	Lights I/O + Dynamic ID (d-ID) (SM-X, SX-2 and SX-E only use Led 8 but this register works the same way)	Led 1 Status
		BIT 1		Led 2 Status
		BIT 2		Led 3 Status
		BIT 3		Led 4 Status
		BIT 4		Led 5 Status
		BIT 5		Led 6 Status
		BIT 6		Led 7 Status
\$45	(read / write_n)	BIT 7		Led 8 Status
		BIT 0 (LSB)	PSG Volume Level (0 - 7)	BIT 0 (LSB)
		BIT 1		BIT 1 (MSB)
		BIT 2		Status
		BIT 3		BIT 0 (LSB)
		BIT 4		BIT 1
		BIT 5		BIT 2 (MSB)
		BIT 6		Status
		\$46		(read / write_n)
BIT 0 (LSB)	OPLL Volume Level (0 - 7)		BIT 0 (LSB)	
BIT 1			BIT 1	
BIT 2			BIT 2 (MSB)	
BIT 3			Status	
BIT 4			BIT 0 (LSB)	
BIT 5			BIT 1	
BIT 6			BIT 2 (MSB)	
\$47			(read only)	
	BIT 0 (LSB)	SCC-I Volume Level (0 - 7)		BIT 0 (LSB)
	BIT 1			BIT 1
	BIT 2			BIT 2 (MSB)
	BIT 3			Status
	BIT 4			Status
	BIT 5			0=Normal, 1=Fast
	BIT 6			Mapper Size Req
	\$48			(read only)
BIT 0 (LSB)		CPU Custom Speed Level (1 - 7)	Status	
BIT 1			BIT 1	
BIT 2			BIT 2 (MSB)	
BIT 3			Status	
BIT 4			Turbo MegaSD (tMSD)	
BIT 5			Turbo Pana Redirection (LPR)	
BIT 6			VDP Speed Mode	
\$49			(read only)	
	BIT 0 (LSB)	Turbo Pana		0=2048 KB, 1=4096 KB
	BIT 1			Status
	BIT 2			0=JP, 1=Non-JP
	BIT 3			Current Keyboard Layout
	BIT 4			SCRLK Toggle
	BIT 5			Lights Mode
	BIT 6			Red Mode (Led 0)
	\$4A			(read only)
BIT 0 (LSB)		Pseudo Stereo	0=Cold Reset ack, 1=Warm Reset ack	
BIT 1			Status	
BIT 2			MegaSD Blink	
BIT 3			Status	
BIT 4			External Clock Mode	
BIT 5			0=Sync to CPU, 1=3.58MHz	
BIT 6			Machine Type ID	
\$4B			(read only)	
	BIT 0	NTSC/PAL Type		BIT 1
	BIT 1			BIT 2
	BIT 2			BIT 3 (MSB)
	BIT 3			0=Forced, 1=Auto
	BIT 4			0=60Hz (NTSC), 1=50Hz (PAL)
	BIT 5			Status
	BIT 6			Right Inverse Audio
	\$4C			(read only)
BIT 0		Centering YIK Modes/R25 Mask	BIT 1	
BIT 1			BIT 2 (MSB)	
BIT 2			Status	
BIT 3			0=To VGA, 1=To VGA+	
BIT 4			Assignment of Legacy Output	
BIT 5			Internal Slot-1 Linear	
BIT 6			Internal Slot-2 Linear	
\$4D			(read only)	
	BIT 0 (LSB)	VGA Scanlines Level		BIT 0 (LSB)
	BIT 1			BIT 1 (MSB)
	BIT 2			Status
	BIT 3			0=None, 1=Light, 2=Medium, 3=Heavy
	BIT 4			SDRAM Size
	BIT 5			(0=8 MB, 1=16 MB, 2=32 MB, 3=Over 32 MB)
	BIT 6			OCM-BIOS Reloading Req
	\$4E			(read only)
BIT 0		Extended MegaROM Reading	BIT 1	
BIT 1			BIT 2	
BIT 2			BIT 3 (MSB)	
BIT 3			Status	
BIT 4			Auxiliary SDRAM Size	
BIT 5			(0=64 MB, 1=128 MB, 2=192 MB, 3=256 MB, 4=384 MB, 5=512 MB, 6=768 MB, 7=1024 MB)	
BIT 6			Vertical Offset (Status+12)	
\$4F			(read only)	
	BIT 0	Sprite Limit		BIT 1
	BIT 1			BIT 2
	BIT 2			BIT 3 (MSB)
	BIT 3			BIT 0 (LSB)
	BIT 4			BIT 1
	BIT 5			BIT 2
	BIT 6			BIT 3 (MSB)
	\$40			(read / write_n)
BIT 0		64 KB VRAM Slot ID (Page 0)	BIT 1	
BIT 1			BIT 2	
BIT 2			BIT 3 (MSB)	
BIT 3			BIT 0 (LSB)	
BIT 4			BIT 1	
BIT 5			BIT 2	
BIT 6			BIT 3 (MSB)	
\$41			(read / write_n)	
	BIT 0	I/O Revision ID (0 - 31)		BIT 1
	BIT 1			BIT 2
	BIT 2			BIT 3
	BIT 3			BIT 4 (MSB)
	BIT 4			BIT 0 (LSB)
	BIT 5			BIT 1 (MSB)
	BIT 6			BIT 1 (MSB)
	\$42			(read / write_n)
BIT 0		OCM-PLD main version X.Y{z} (range 0.0.z - 25.5.z)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4	
BIT 6			BIT 5	
\$43			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$44			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$45			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$46			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$47			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$48			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$49			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$4A			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$4B			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$4C			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$4D			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$4E			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$4F			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$50			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$51			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$52			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$53			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$54			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$55			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$56			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$57			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$58			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$59			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$5A			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$5B			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$5C			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$5D			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$5E			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$5F			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$60			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$61			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$62			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$63			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)
	\$64			(read / write_n)
BIT 0		OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)	BIT 7 (MSB)	
BIT 1			BIT 0 (LSB)	
BIT 2			BIT 1	
BIT 3			BIT 2	
BIT 4			BIT 3	
BIT 5			BIT 4 (MSB)	
BIT 6			BIT 0 (LSB)	
\$65			(read / write_n)	
	BIT 0	OCM-PLD sub version (x.y).Z (range x.y.0 - x.y.3)		BIT 7 (MSB)
	BIT 1			BIT 0 (LSB)
	BIT 2			BIT 1
	BIT 3			BIT 2
	BIT 4			BIT 3
	BIT 5			BIT 4 (MSB)
	BIT 6			BIT 0 (LSB)