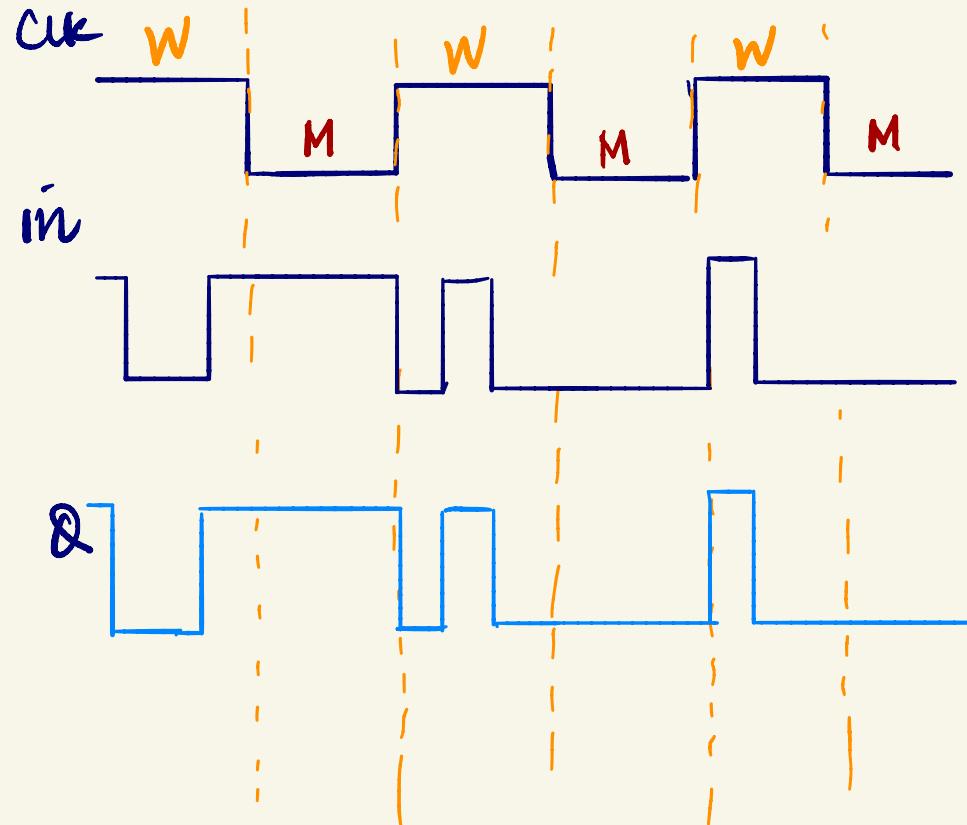
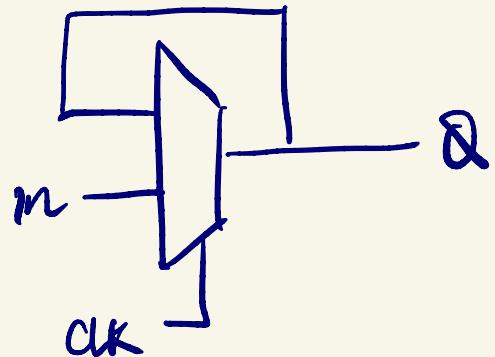


$Clk = 0$  memory mode

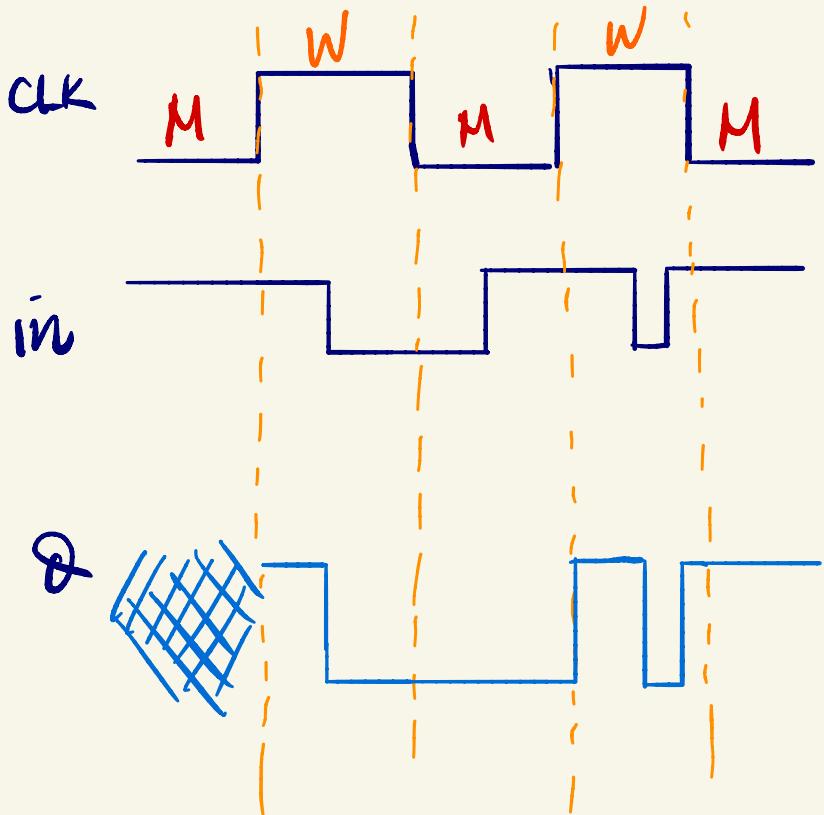
$Clk = 1$  write mode

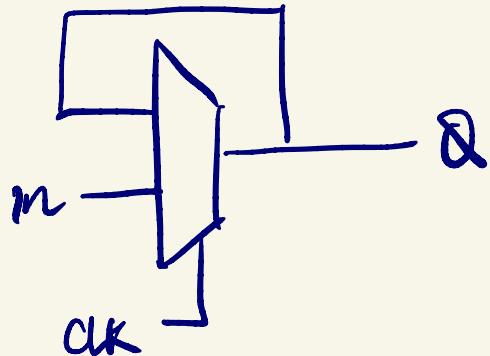




$Clk = 0$  memory mode

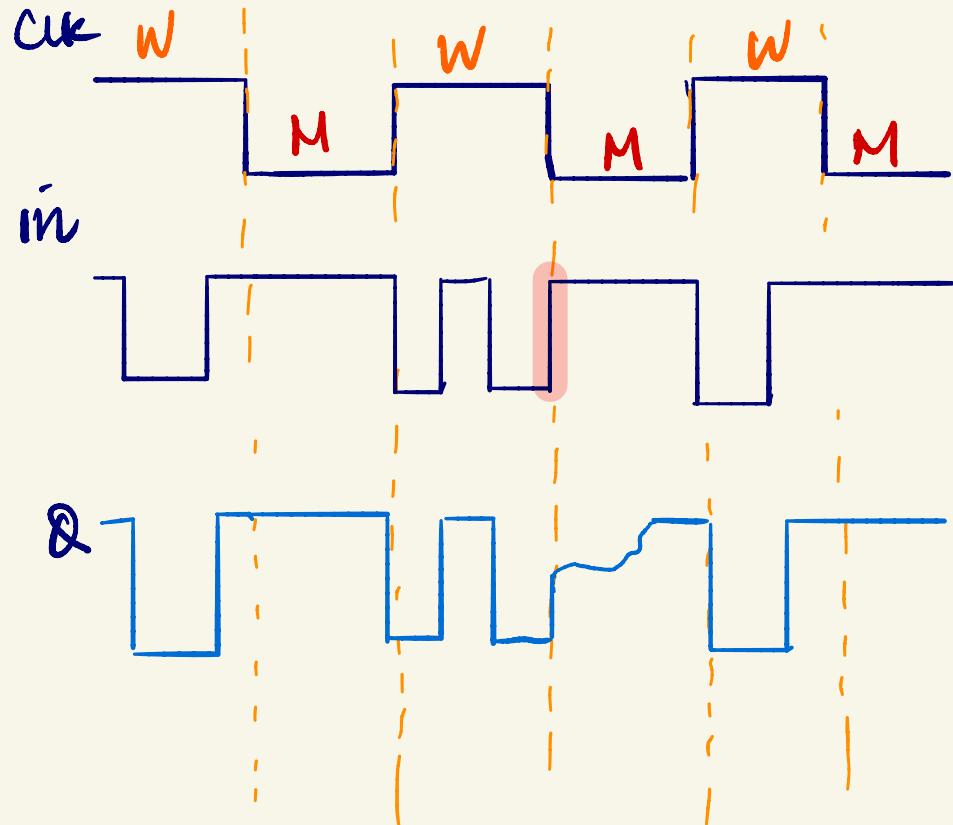
$Clk = 1$  write mode

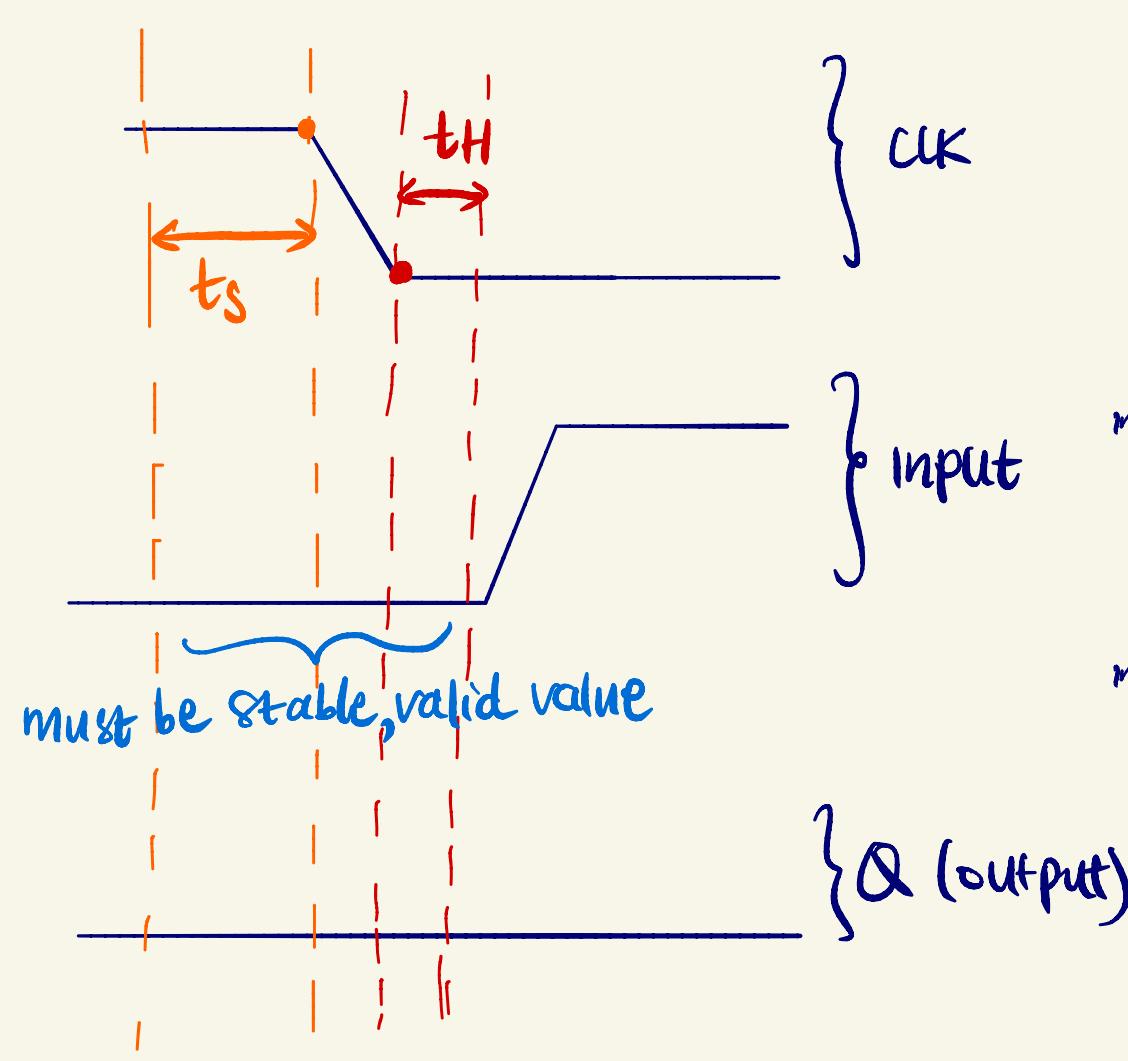




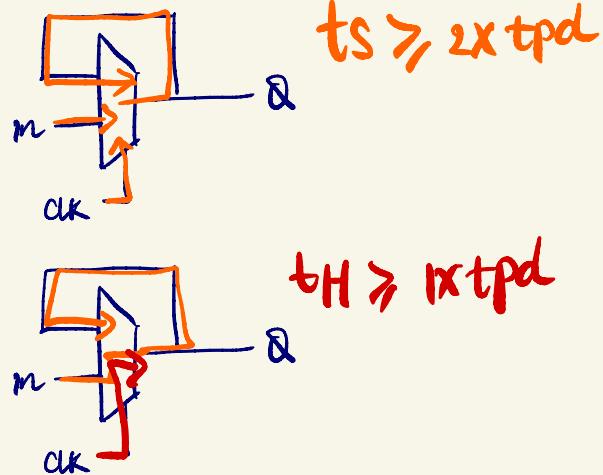
$\text{Clk} = 0$  memory mode

$\text{Clk} = 1$  write mode

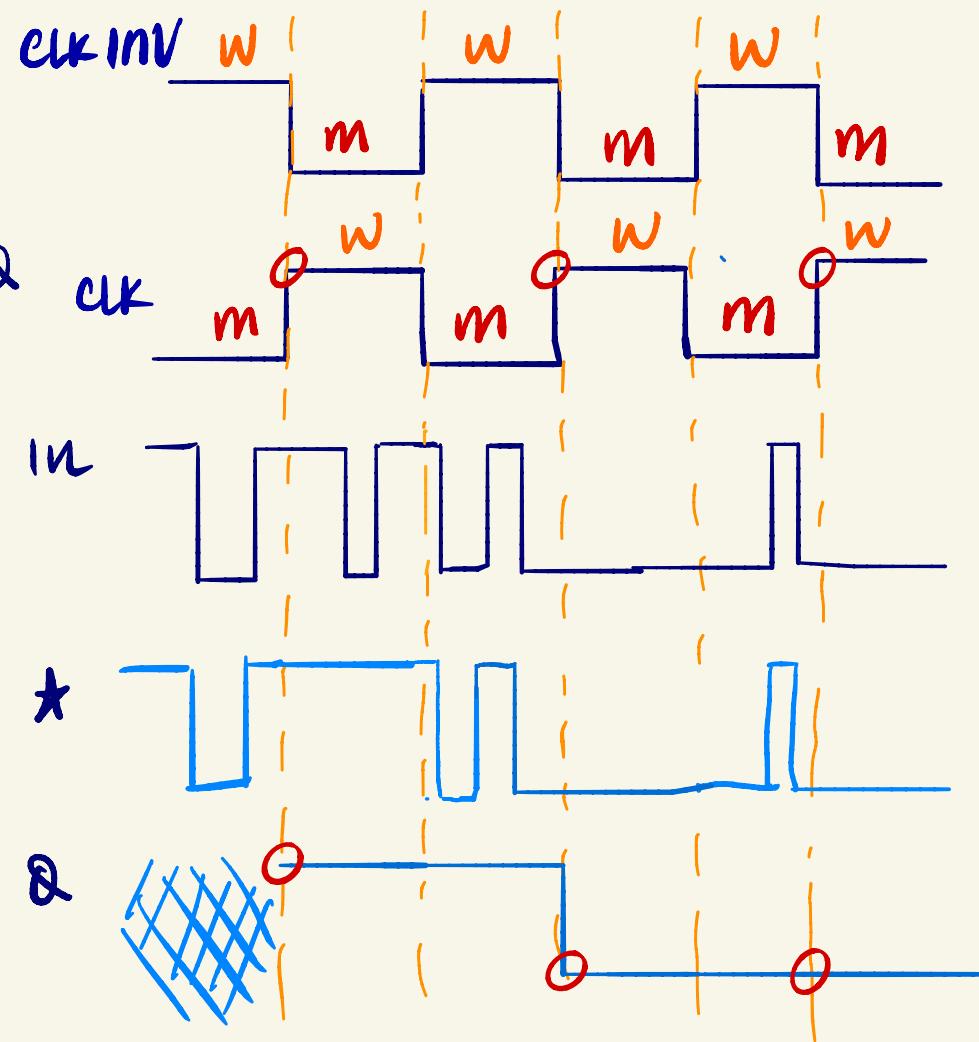
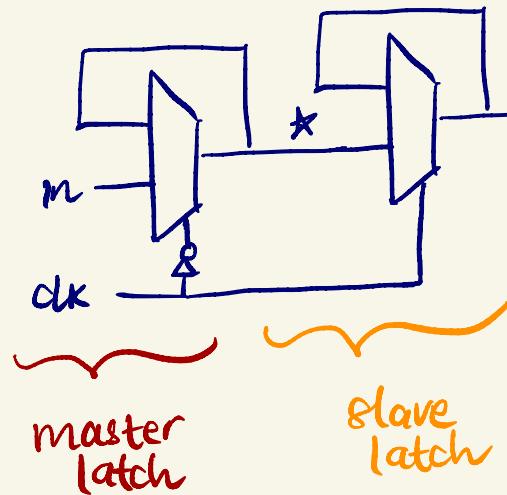


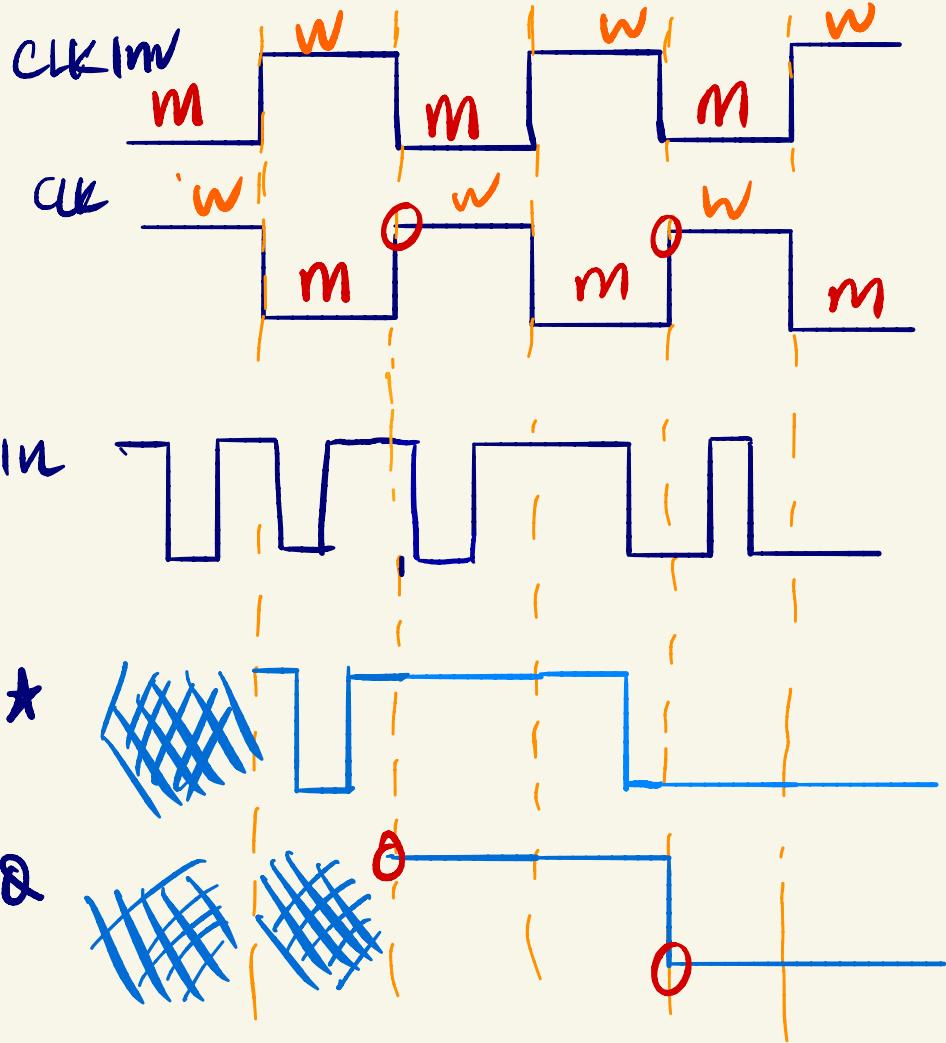
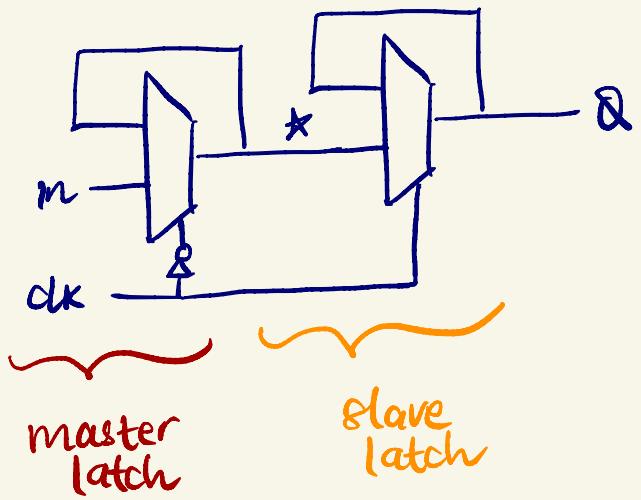


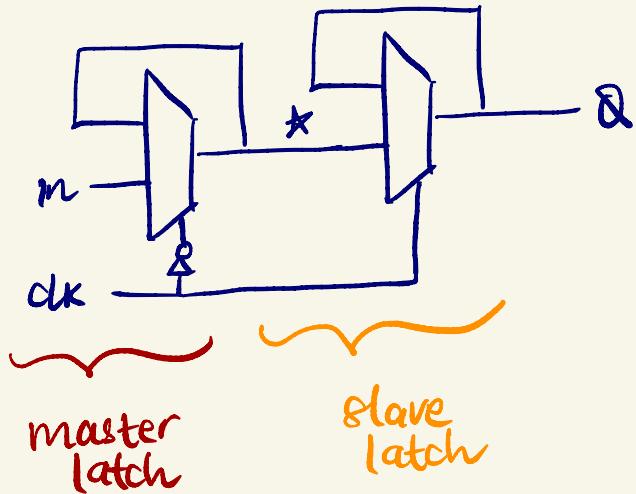
## Dynamic Discipline



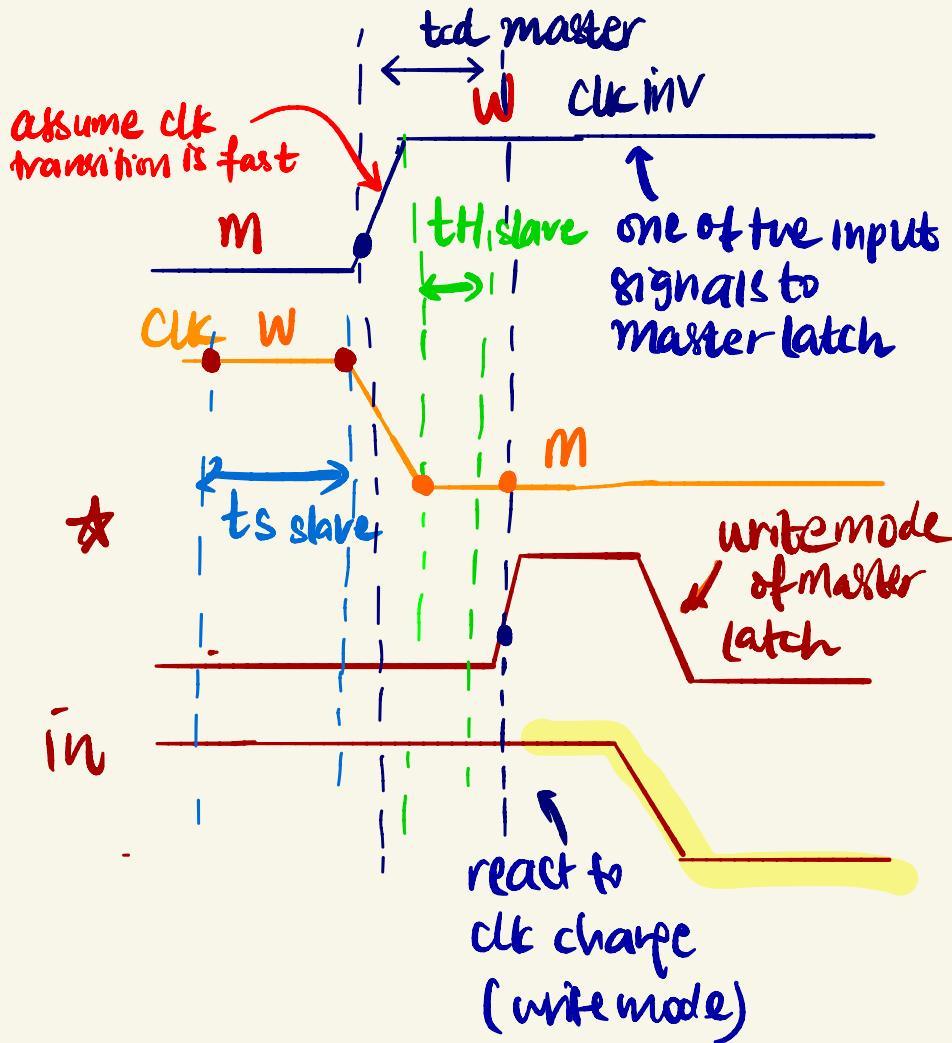
# Registers



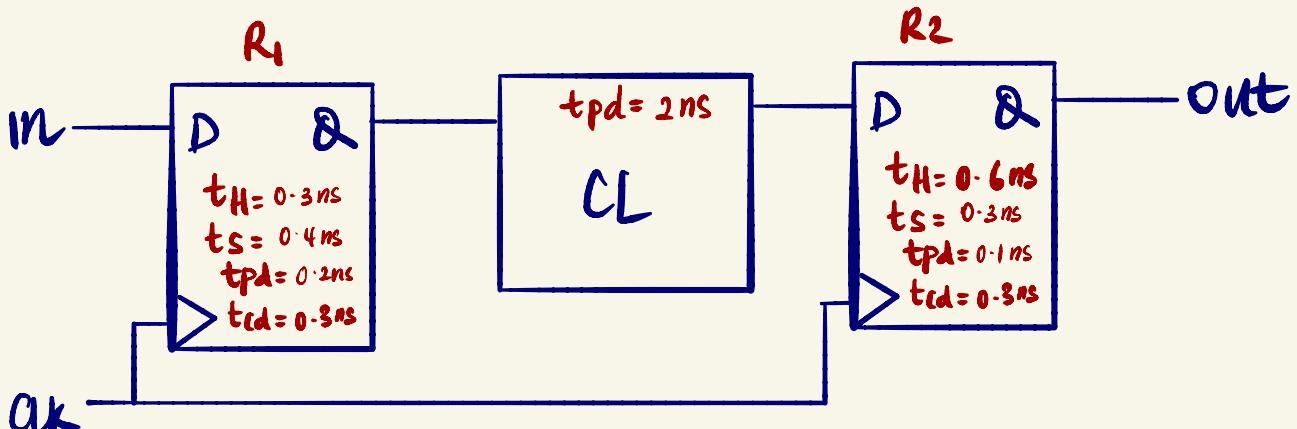




$t_{CD}$  of master latch >  
 $t_{Hold}$  slave latch  
 → for dynamic discipline  
 to apply



case 1



$$\text{overall } t_{PD} = t_{PD} R_2 = 0.1 \quad \left. \right\} \text{sequential logic}$$

$$\text{overall } t_{CD} = t_{CD} R_2 = 0.3$$

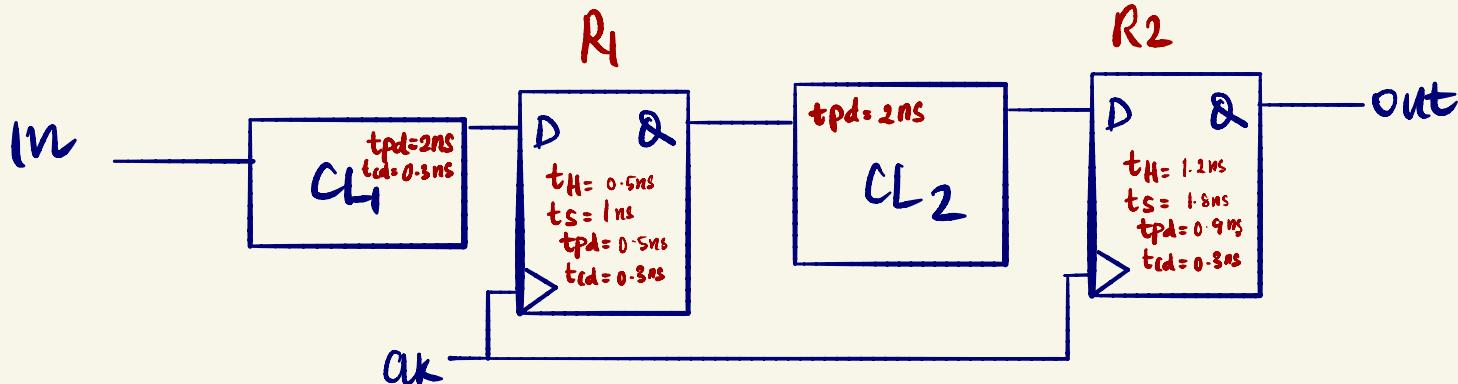
$$\min t_{CD} CL = t_H R_2 - t_{CD} R_1 = 0.6 - 0.3 = 0.3$$

$$\min \text{clk period} = t_{PD} R_1 + t_{PD} CL + t_S R_2 = 0.2 + 2 + 0.3 = 2.5$$

$$t_H \text{ input} = t_H R_1 = 0.3$$

$$t_S \text{ input} = t_S R_1 = 0.4$$

## Case 2



$$\text{overall } t_{pd} = t_{pd} R_2 = 0.9 \quad \left. \right\} \text{sequential logic}$$

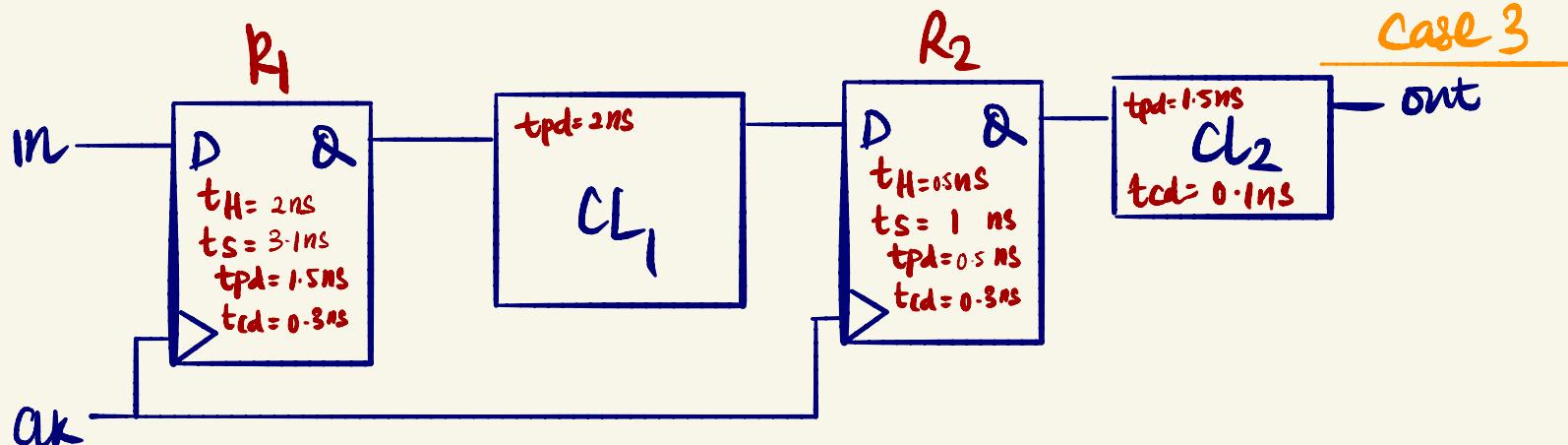
$$\text{overall } t_{cd} = t_{cd} R_2 = 0.3$$

$$\min t_{cd} CL_2 = t_H R_2 - t_{cd} R_1 = 1.2 - 0.3 = 0.9$$

$$\min \text{clk period} = t_{pd} R_1 + t_{pd} CL_2 + t_S R_2 = 0.5 + 2 + 1.8 = 4.3$$

$$t_H \text{ input} = t_H R_1 - t_{cd} CL_1 = 0.5 - 0.3 = 0.2$$

$$t_S \text{ input} = t_S R_1 + t_{pd} CL_1 = 2 + 1 = 3$$



$$\text{Overall } t_{pd} = t_{pd} R_2 + t_{pd} CL_2 = 0.5 + 1.5 = 2$$

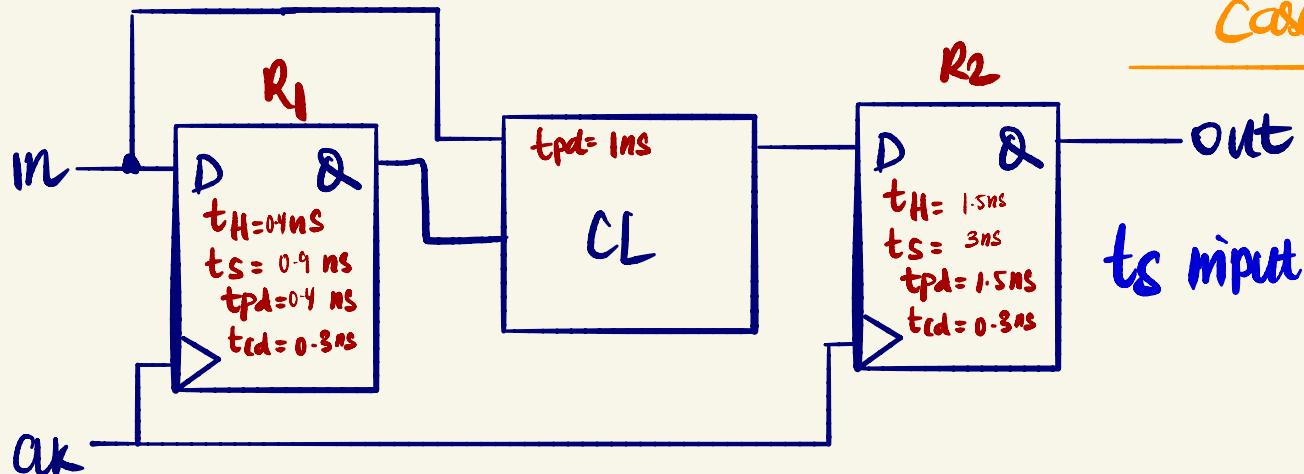
$$\text{Overall } t_{cd} = t_{cd} R_2 + t_{cd} CL_2 = 0.3 + 0.1 = 0.4$$

$$\min t_{cd} CL_1 = t_{H} R_2 - t_{cd} R_1 = 0.5 - 0.3 = 0.2$$

$$\min \text{clk period} = t_{pd} R_1 + t_{pd} CL_2 + t_S R_2 = 1.5 + 2 + 1 = 4.5$$

$$t_H \text{ input} = t_H R_1 = 2$$

$$t_S \text{ input} = t_S R_1 = 3.1$$



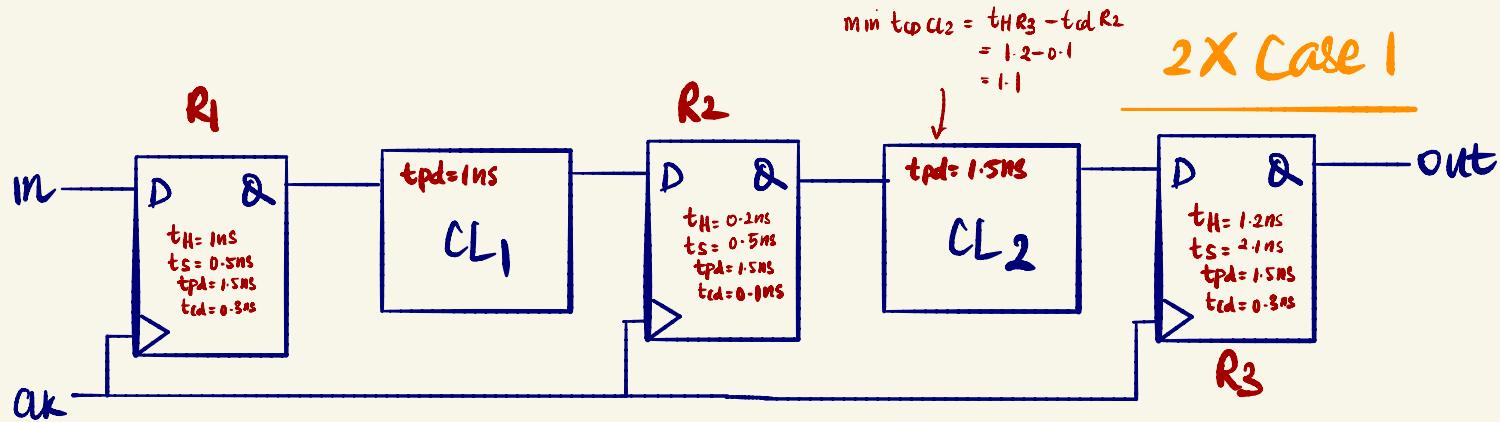
$$\text{Overall } t_{pd} = t_{pd\text{R2}} = 1.5 \quad \left. \begin{array}{l} \\ \end{array} \right\} \text{sequential logic}$$

$$\text{Overall } t_{cd} = t_{cd\text{R2}} = 0.3$$

$$\min t_{cd\text{CL}} = t_{H\text{R2}} - t_{cd\text{R1}} = 1.5 - 0.3 = 1.2$$

$$\min \text{clk period} = t_{pd\text{R1}} + t_{pd\text{CL}} + t_{SR2} = 0.4 + 1 + 3 = 4.4$$

$$t_{H\text{ input}} = \begin{cases} t_H R_1 = 0.4 \\ t_H R_2 - t_{cd\text{CL}} = 1.5 - 1.2 = 0.3 \end{cases}$$



Overall  $t_{pd} = t_{pd} R_3 = 1.5$  } sequential logic  
 Overall  $t_{cd} = t_{cd} R_3 = 0.3$       time cannot be  
-ve so clamp to 0

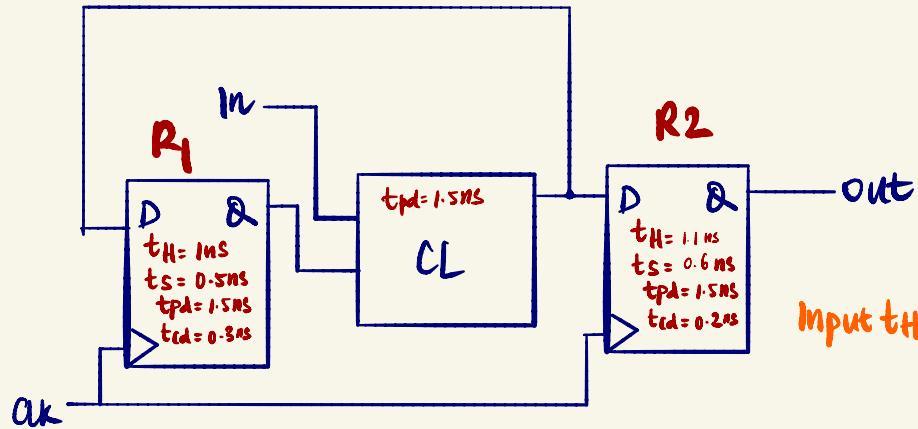
$$\min t_{CD} CL_1 = t_{HR_2} - t_{CD} R_1 = 0.2 - 0.3 = 0$$

$$\min CLK period = \max \left\{ \begin{array}{l} t_{pd} R_1 + t_{pd} CL_1 + t_S R_2 = 3 \\ t_{pd} R_2 + t_{pd} CL_2 + t_S R_3 = 5.1 \end{array} \right. = 5.1$$

$t_H$  input =  $t_{HR_1} = 1$

$t_S$  input =  $t_S R_1 = 0.5$

## Case 1 + case looped



$$\begin{aligned} \text{Input } t_S &= \max \left\{ t_{SR2} + t_{pdCL}, t_{SR1} + t_{pdCL} \right\} \\ &= \max \left\{ 0.6 + 1.5 = 2.1, 0.5 + 1.5 = 2.0 \right\} \\ \text{Input } t_H &= \max \left\{ t_{HR2} - t_{cdCL} = 1 - 0.8 = 0.2, t_{HR2} - t_{cdCL} = 1.1 - 0.8 = 0.3 \right\} \end{aligned}$$

0.3

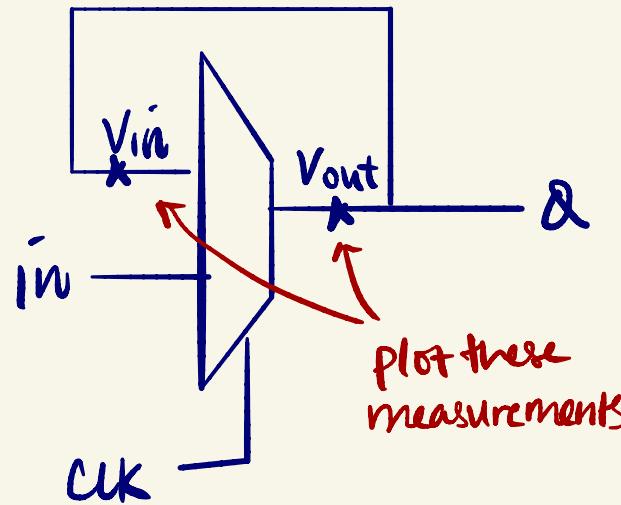
Overall  $t_{pd} = t_{pdR2} = 1.5$

Overall  $t_{cd} = t_{cdR2} = 0.2$

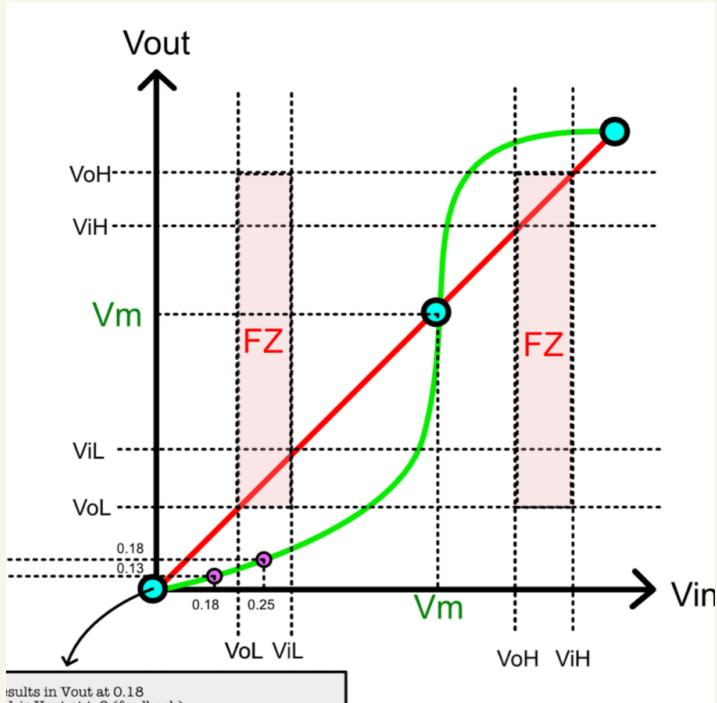
use it here

$$\min t_{cdCL} = \max \left\{ t_{HR2} - t_{cdR1} = 1.1 - 0.3 = 0.8, t_{HR1} - t_{cdR1} = 1 - 0.3 = 0.7 \right\} = 0.8$$

$$\begin{aligned} \min CLK &= \max \left\{ t_{pdR1} + t_{pdCL} + t_{SR2} = 1.5 + 1.5 + 0.6 = 3.6, t_{pdR1} + t_{pdCL} + t_{SR1} = 1.5 + 1.5 + 0.5 = 3.5 \right\} = 3.6 \end{aligned}$$



plot these  
measurements



given:

$$\text{at } t=t_0 \rightarrow V_{in} = 0.18V \quad \left. \begin{array}{l} \\ \end{array} \right\} \text{first loop}$$

$$V_{out} = 0.13$$

$$\text{at } t=t_1 \rightarrow V_{in} = V_{out}(t=0) + \text{noise} \quad \left. \begin{array}{l} \\ \end{array} \right\} \text{2nd loop}$$

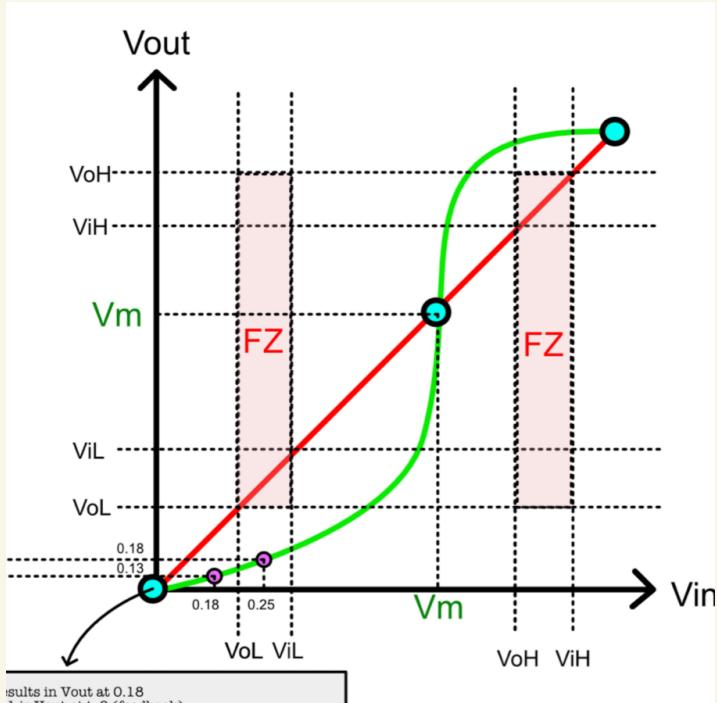
$$= 0.14$$

$$V_{out} = 0.05 - \text{noise} \quad \left. \begin{array}{l} \\ \end{array} \right\} \text{3rd loop}$$

$$\text{at } t=t_2 \rightarrow V_{in} = V_{out}(t=1) + \text{noise}$$

$$= 0.04$$

$V_{out} \approx 0$   
 $\curvearrowright$  stable



given:

$$\text{at } t=t_0 \rightarrow V_{in} = V_m$$

$$V_{out} = V_m$$

*{ first loop }*

$$\text{at } t=t_1 \rightarrow V_{in} = V_{out}(t=0) \stackrel{\text{+ noise}}{=} V_m + 0.01$$

*{ 2nd loop }*

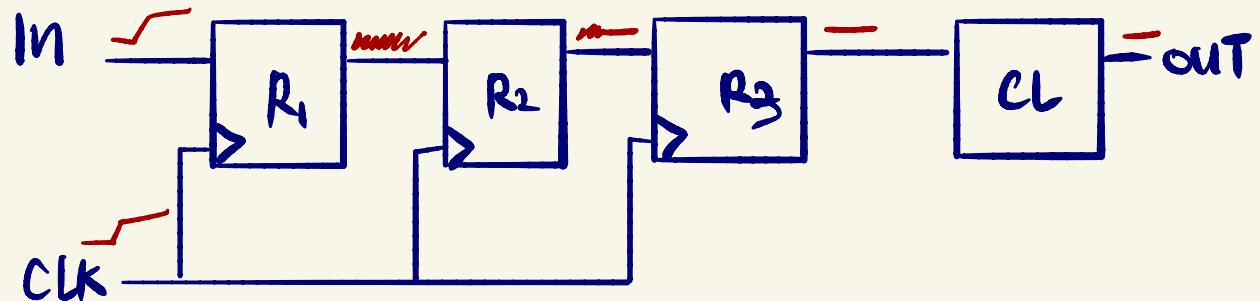
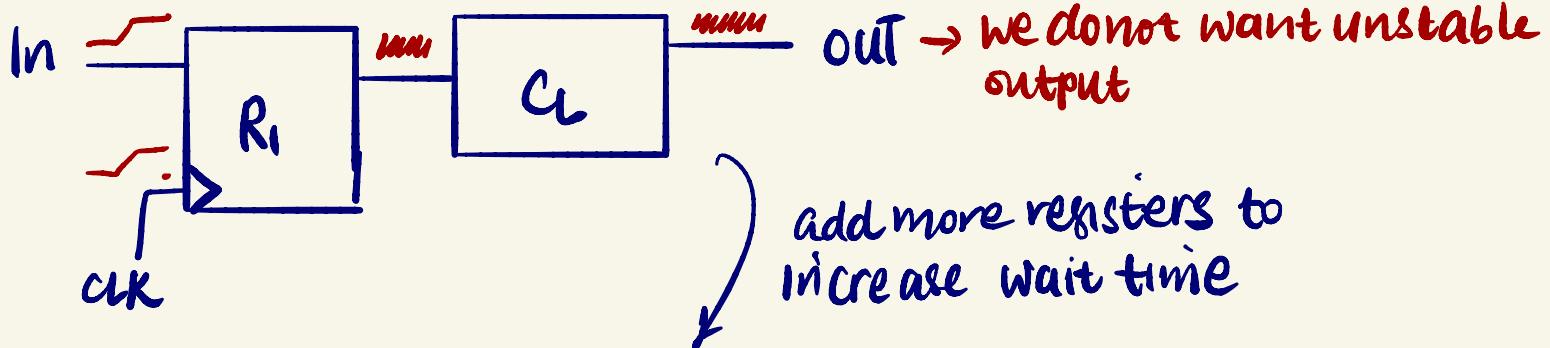
$$V_{out} = V_m - 0.01$$

$$\text{at } t=t_2 \rightarrow V_{in} = V_{out}(t=1) \stackrel{\text{+ noise}}{=} V_m - 0.01$$

*{ 3rd loop }*

$V_{out} = V_m + 0.02$   
*oscillating*

METASTABLE STATE

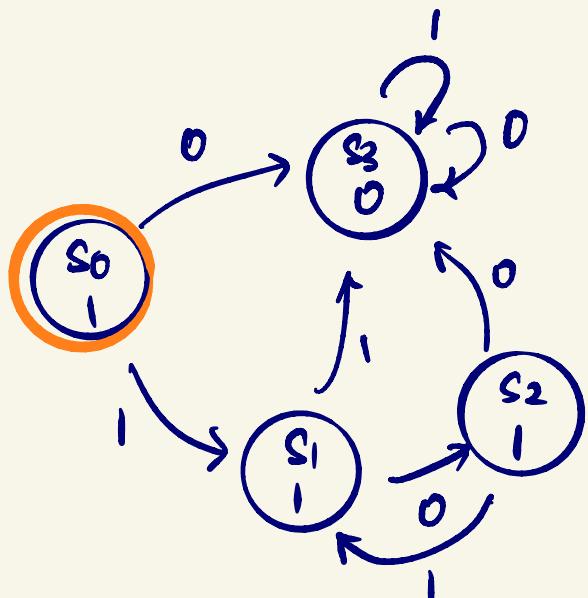


# Task: Binary parser

101010 ✓  
1110 X  
0001 X

input	state	next state	output
0	S0	S3	0
1	S0	S1	1
0	S1	S2	1
1	S1	S3	0
0	S2	S3	0
1	S2	S1	1
0	S3	S3	0
1	S3	S3	0

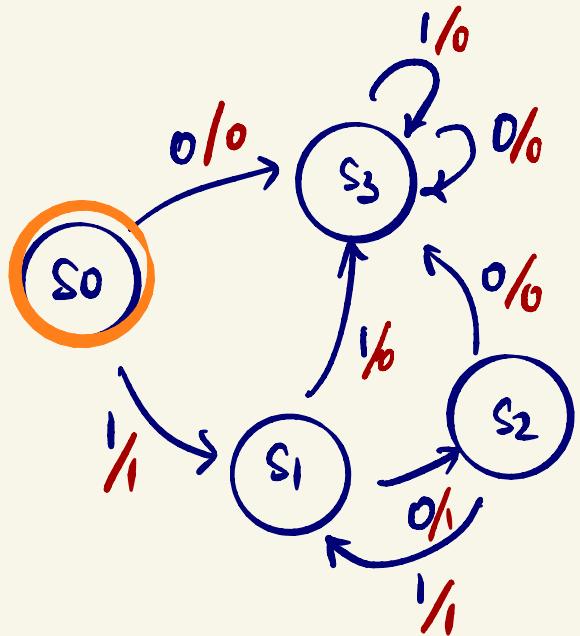
# Moore machine



input	state	next state	output
0	S0	S3	0
1	S0	S1	1
0	S1	S2	1
1	S1	S3	0
0	S2	S3	0
1	S2	S1	1
0	S3	S3	0
1	S3	S3	0

} one state-output pair  
if we have  $\boxed{S_2 \ 0}$ , then  
this is another state-output pair

# meally machine

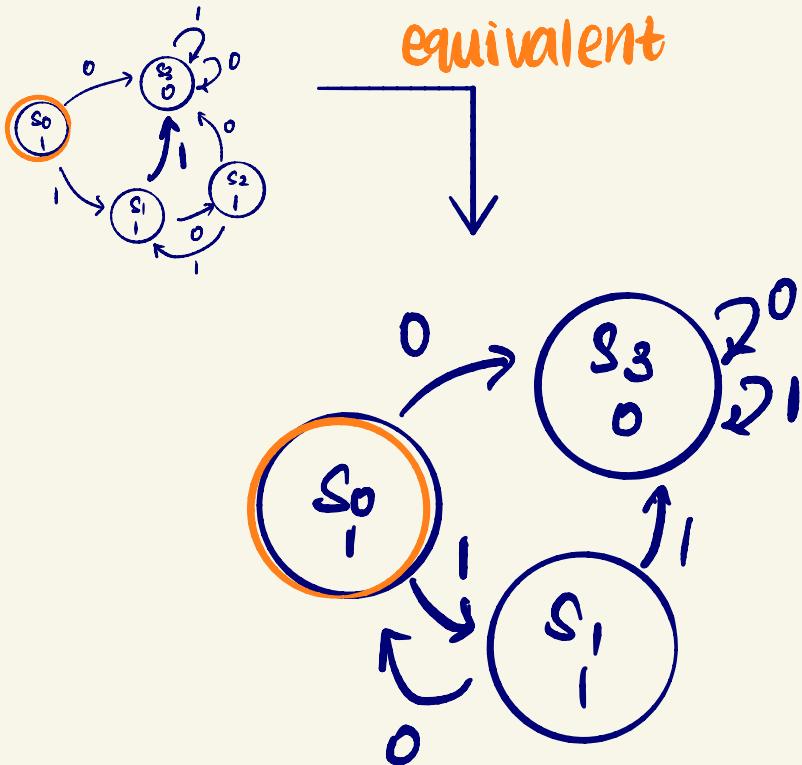


input	state	next state	output
0	S0	S3	0
1	S0	S1	1
0	S1	S2	1
1	S1	S3	0
0	S2	S3	0
1	S2	S1	1
0	S3	S3	0
1	S3	S3	0

} one per state.  
if we have entrance  
to  $S_2$  that produces '0',  
that's another "arrow" to  $S_2$ :

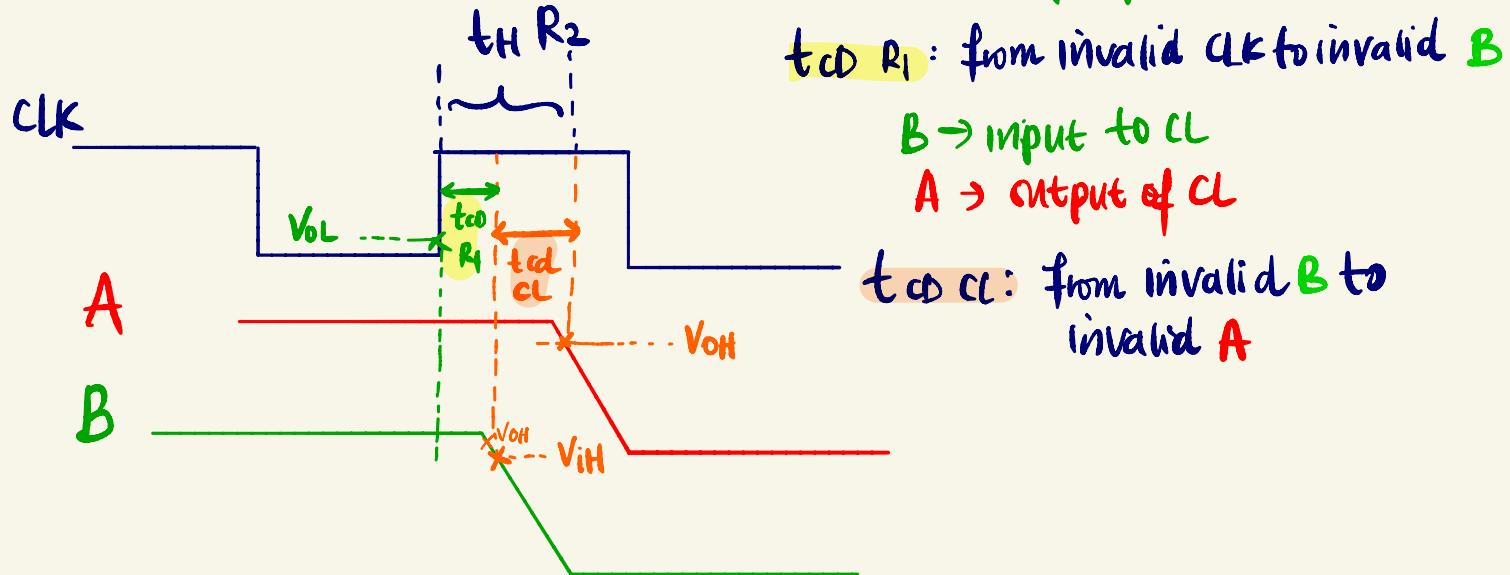
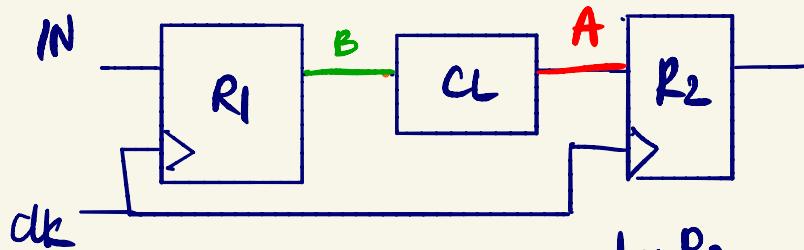
e.g.:  $I/O \rightarrow S_2$

# Equivalence

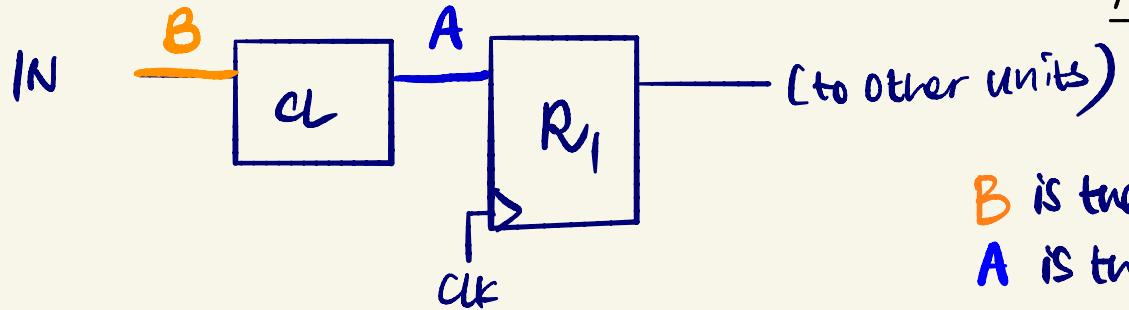


Input state		next state output	
0	S0	S3	0
1	S0	S1	1
0	S1	S2	1
1	S1	S3	0
0	S2	S3	0
1	S2	S1	1
0	S3	S3	0
1	S3	S3	0

## About min tcd CL



from graph:  $t_{HR2} = t_{cd} R_1 + t_{cd} CL \Rightarrow t_{cd} CL = t_{HR2} - t_{cd} R_1 \neq$



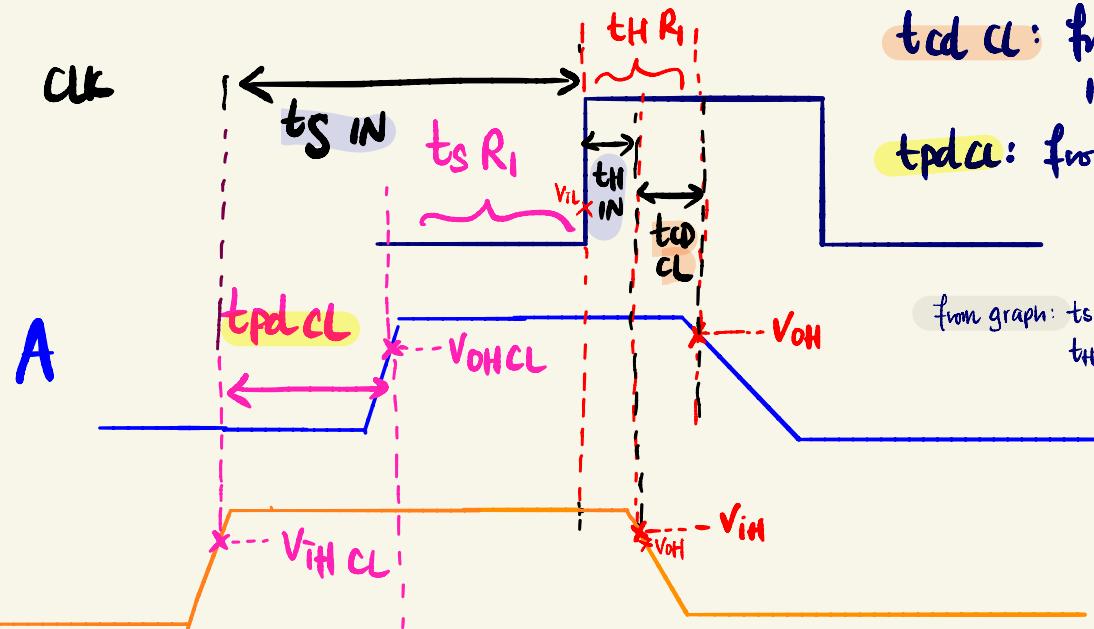
About  $t_{S\ IN}$  &  $t_{H\ IN}$

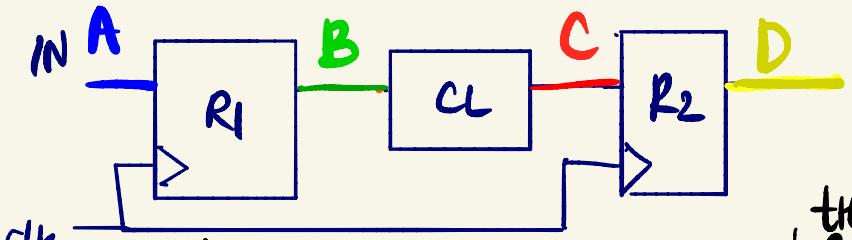
B is the input to CL

A is the output of CL

tcd CL: from invalid A to invalid B

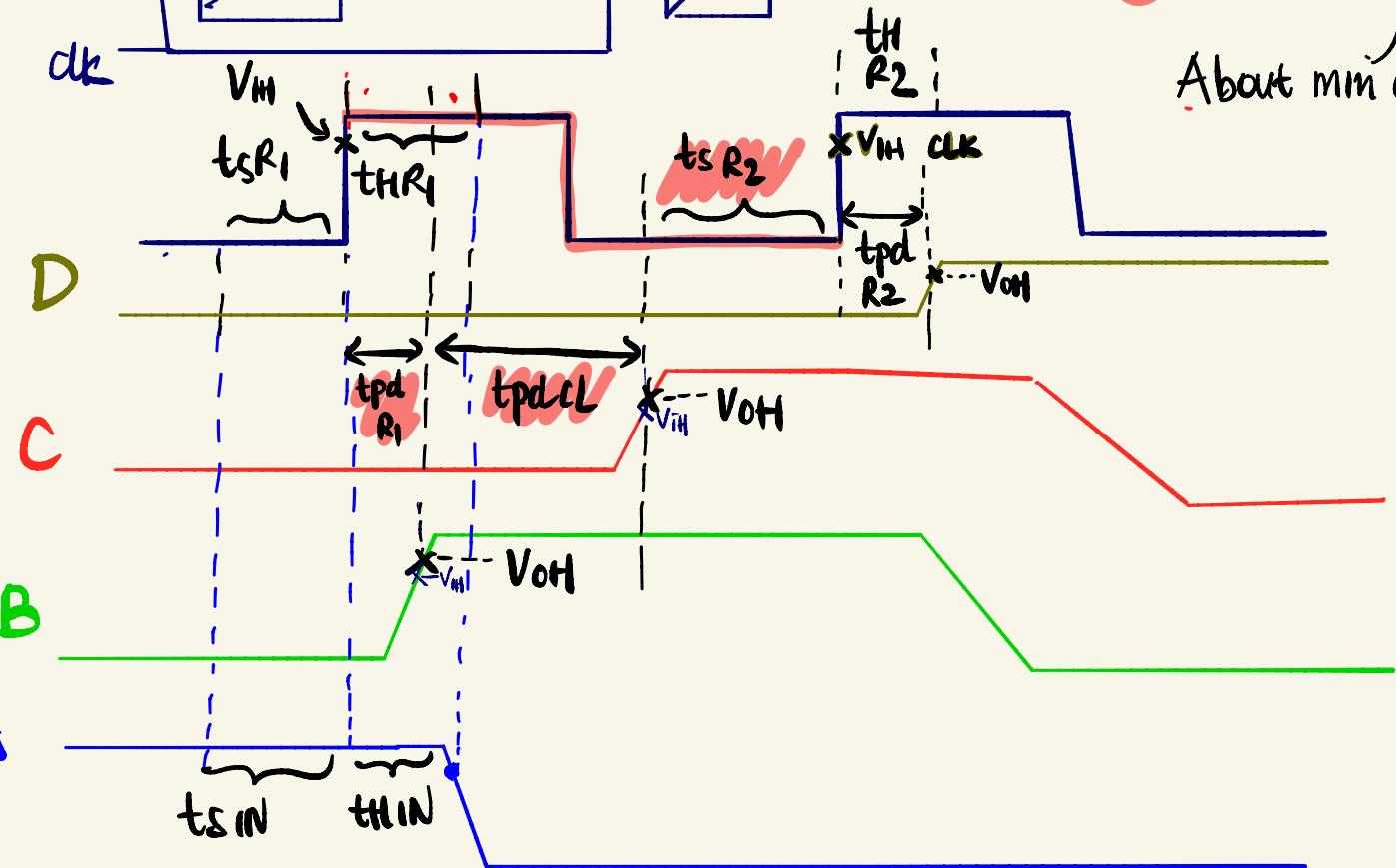
tpdCL: from valid A to valid B

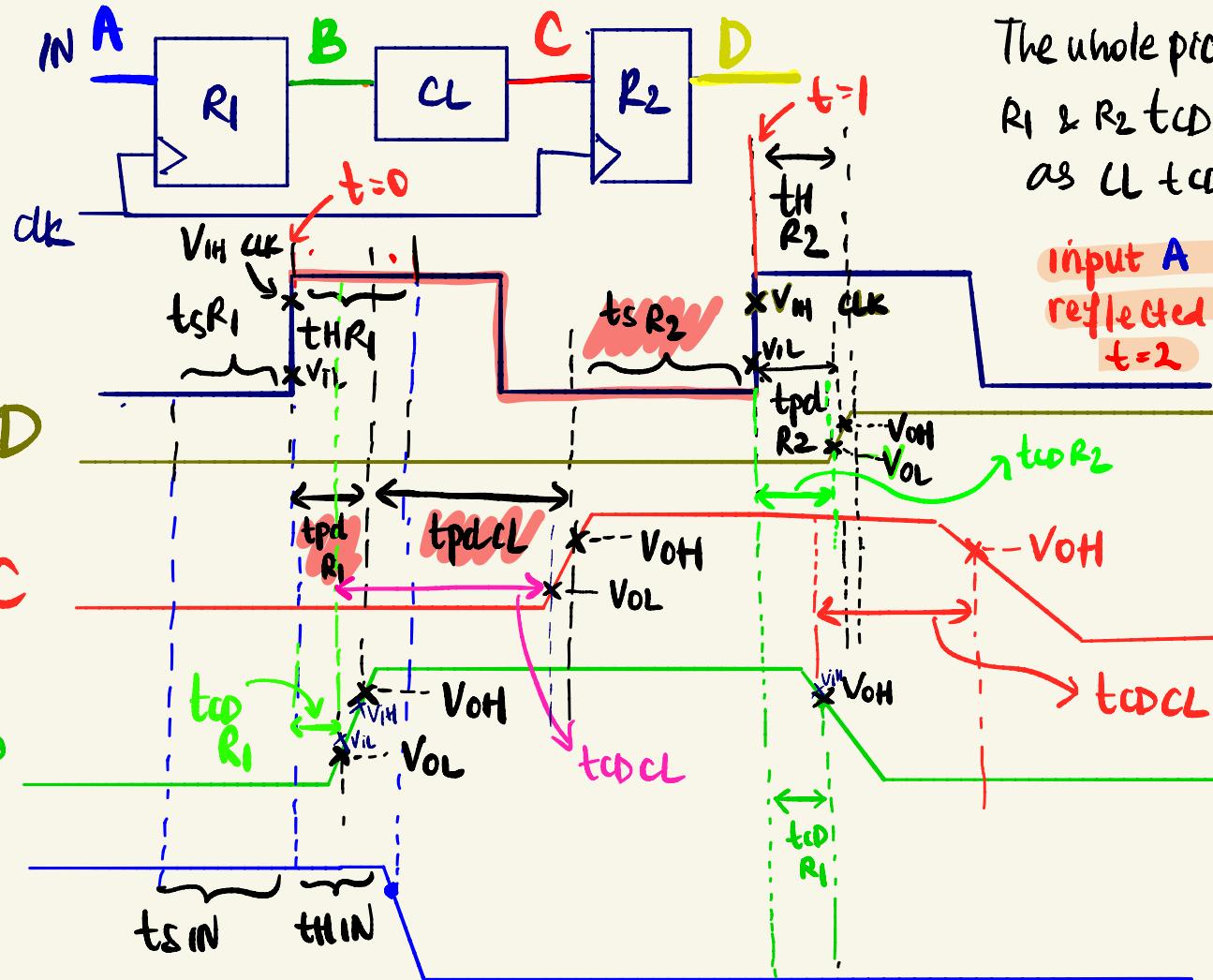




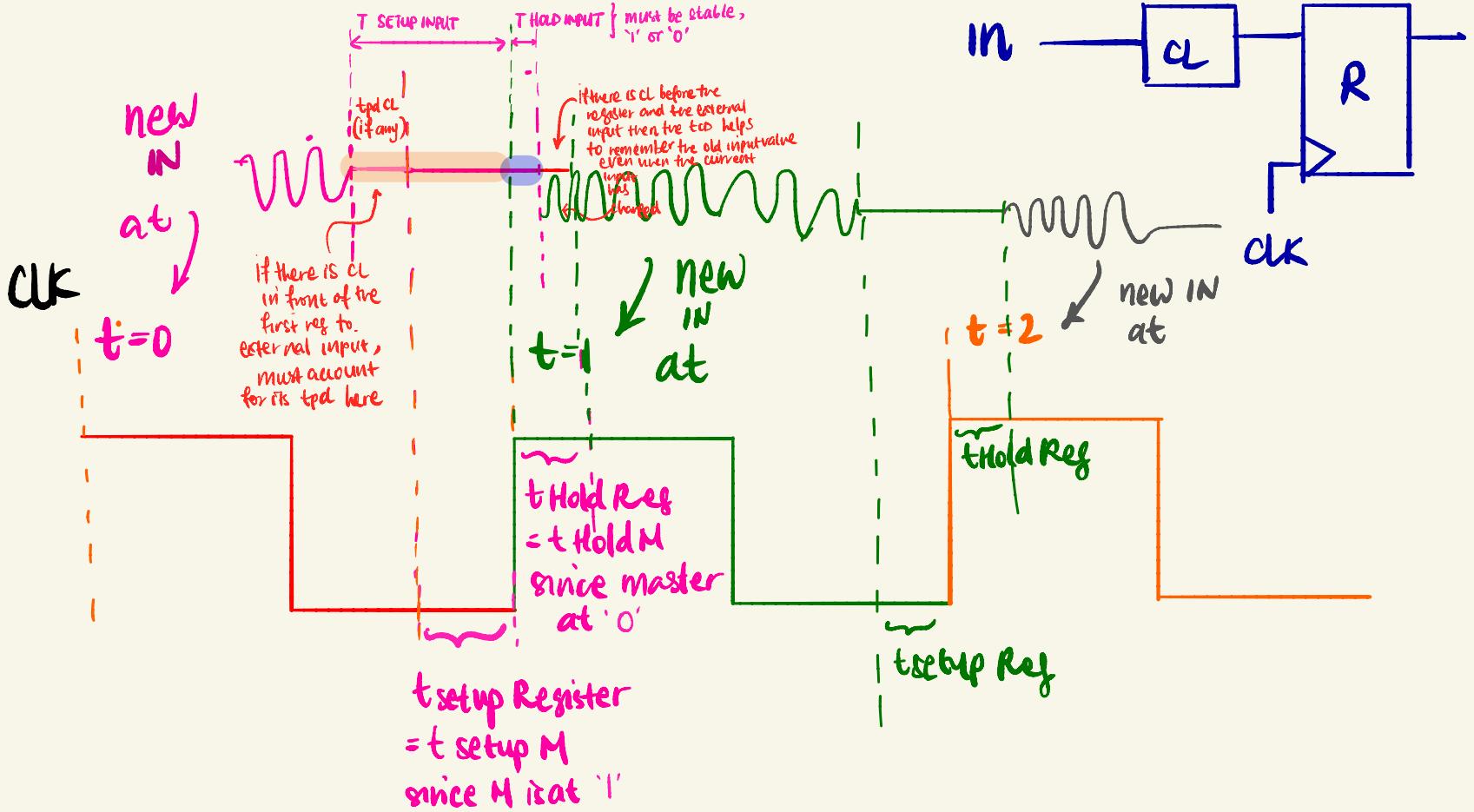
In ONE period we must fit:  
 $t_{pd} R_1 + t_{pd} CL + t_{SR_2}$

↑  
 About min clk period





The whole picture with  
 $R_1$  &  $R_2$   $t_{CD}$ , as well  
as  $CL$   $t_{CD}$



CLK

