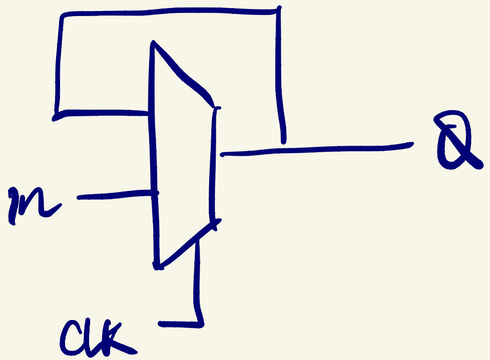
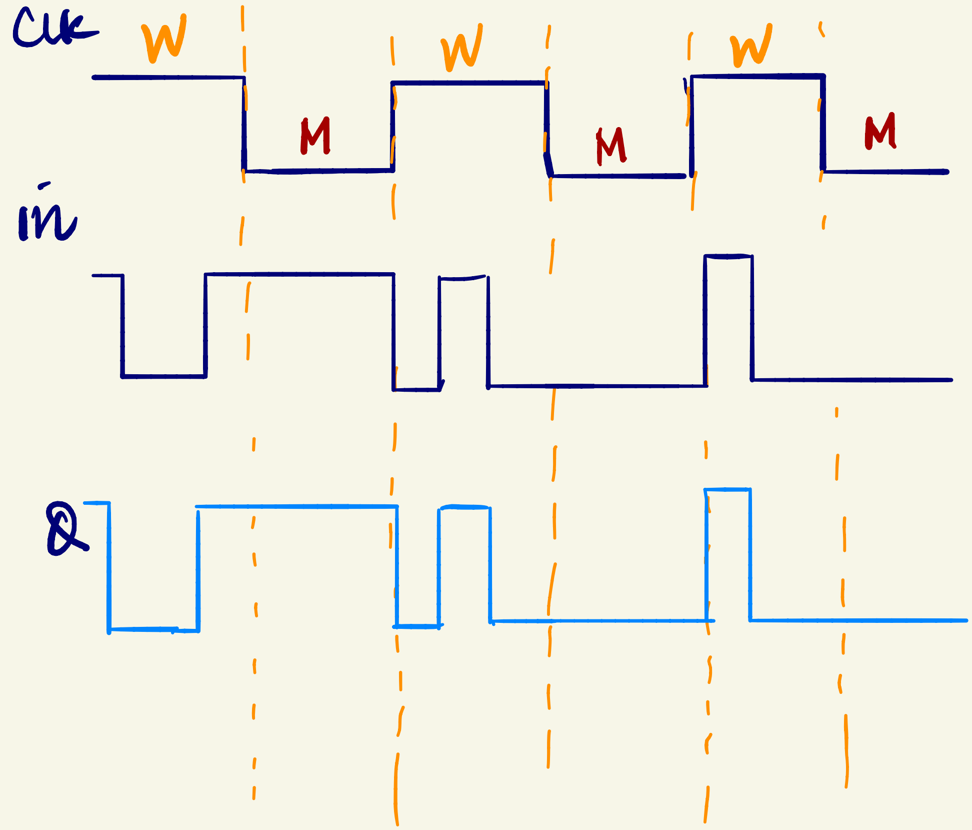
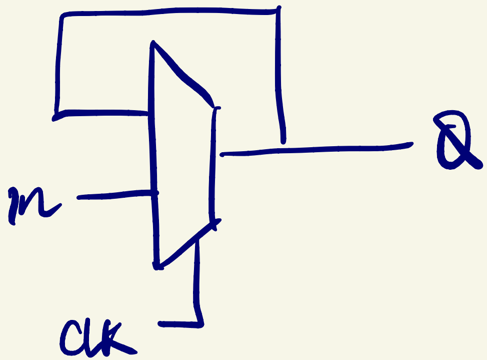
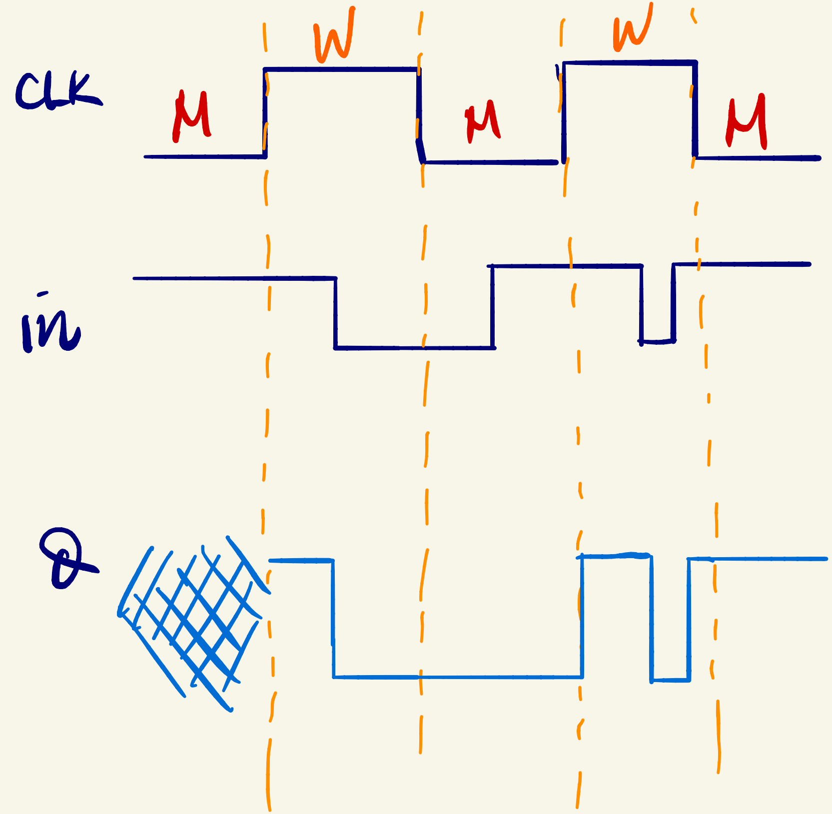




Clk = 0 memory mode

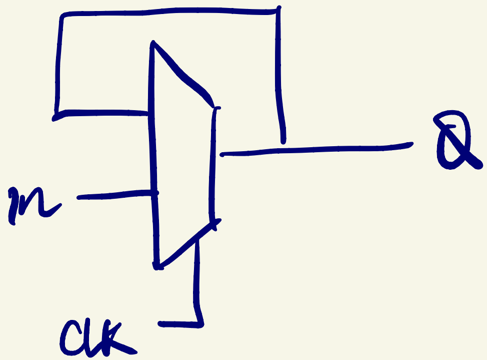
Clk = 1 write mode

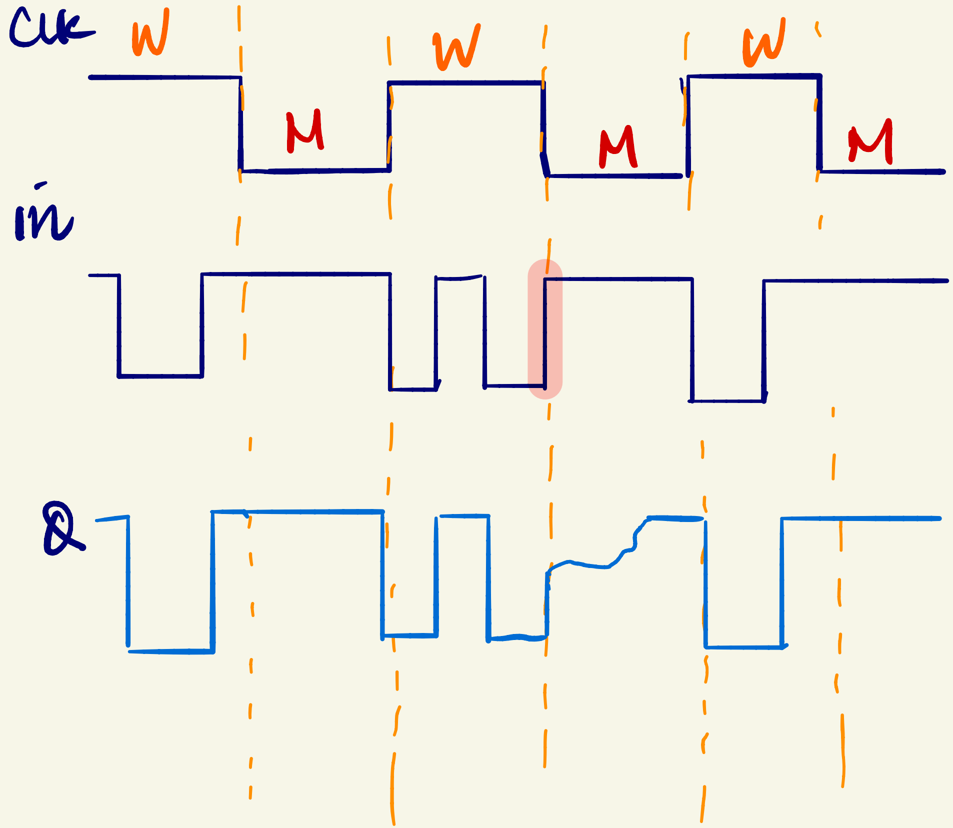




clk = 0 memory mode

clk = 1 write mode

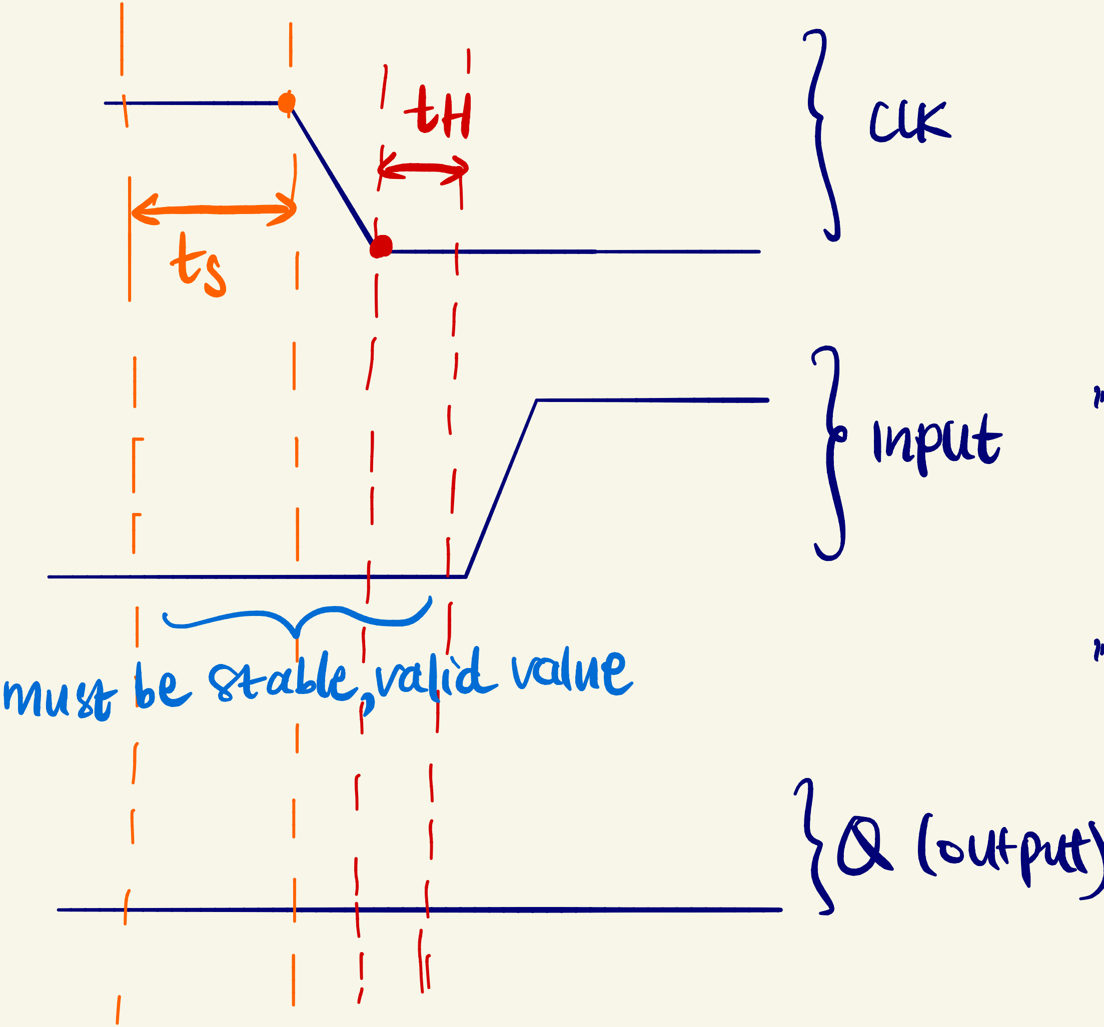




clk = 0 memory mode

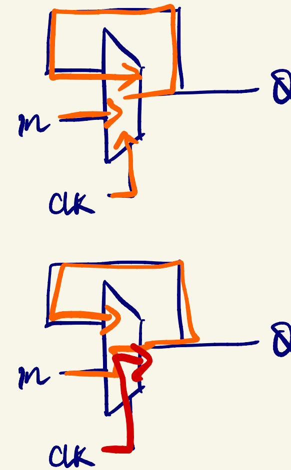
clk = 1 write mode

Dynamic Discipline

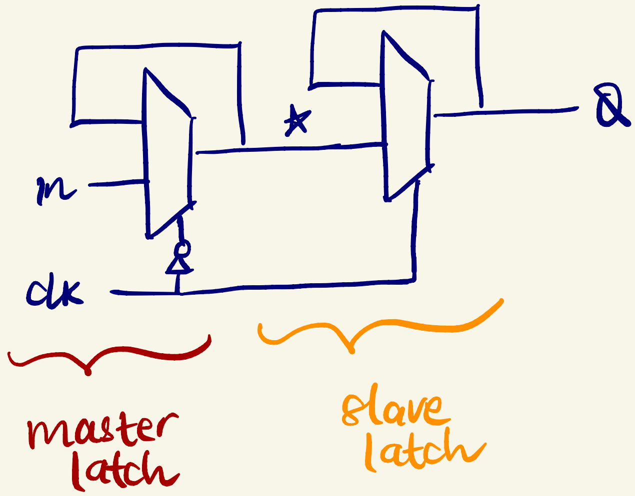


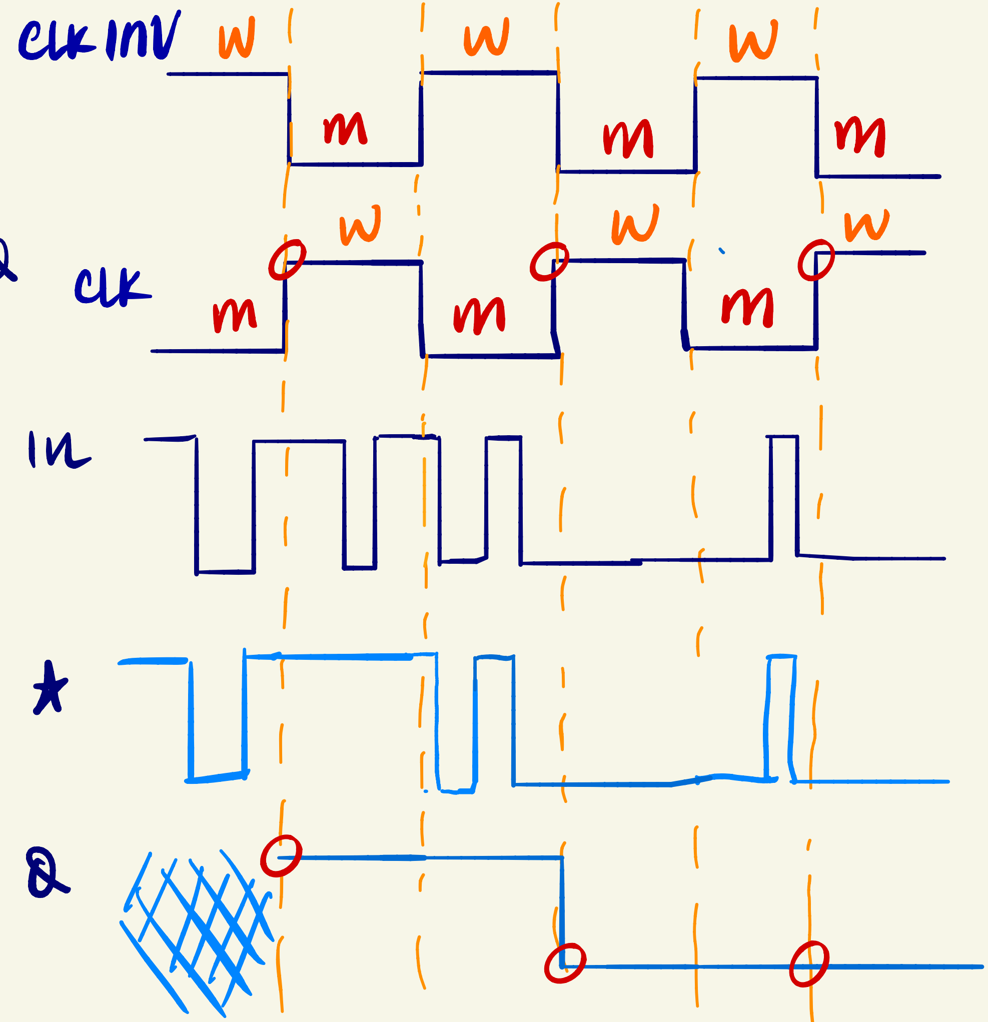
$t_S \geq 2 \times t_{pd}$

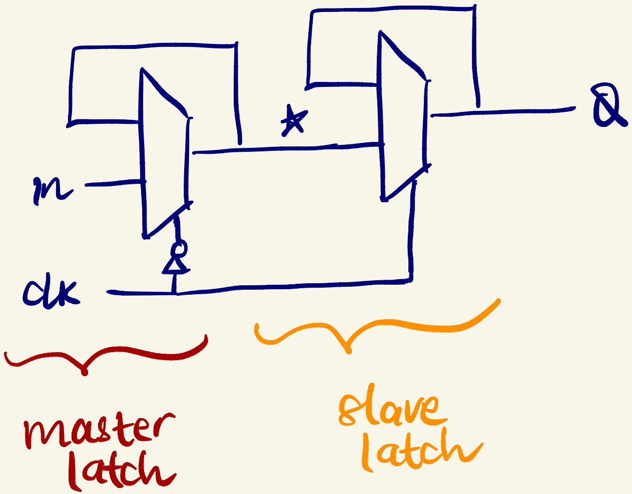
$t_H \geq 1 \times t_{pd}$

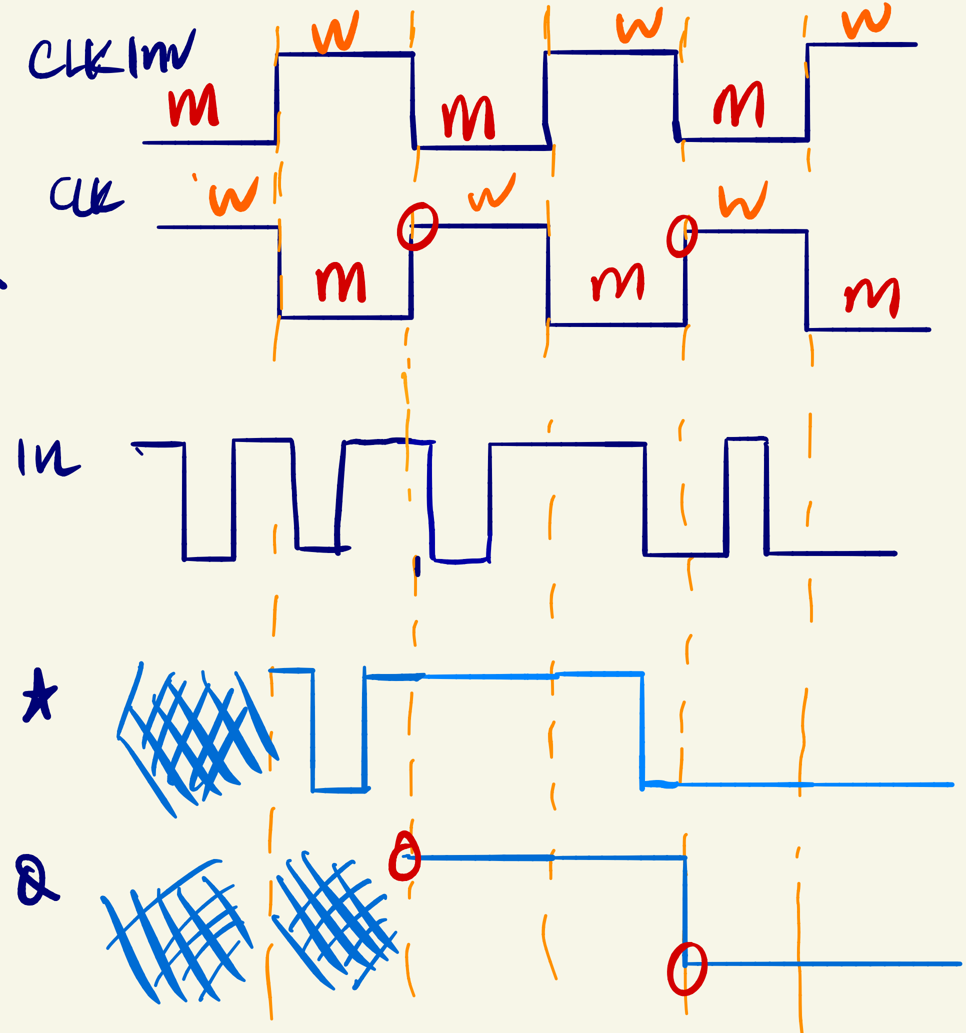


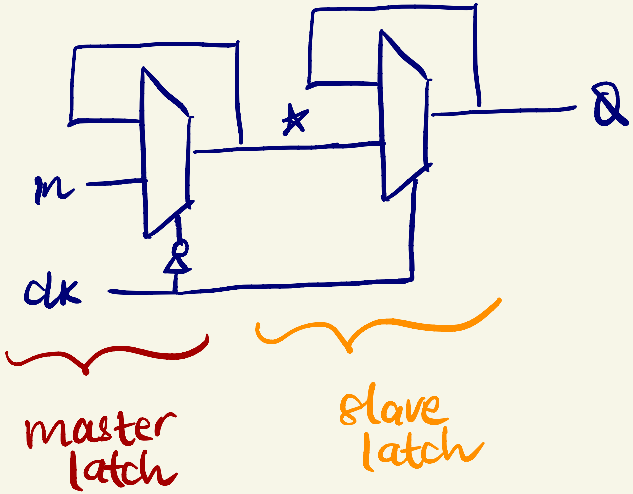
Registers

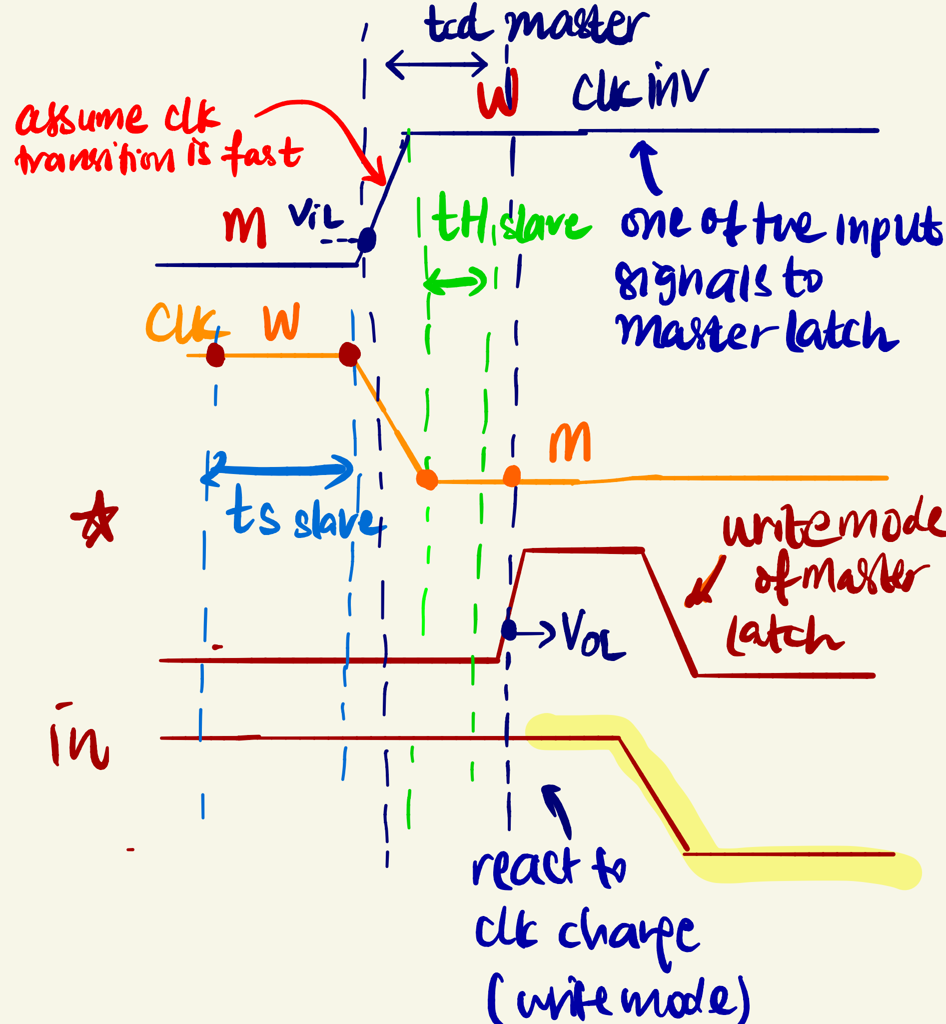





in
clk
★
Q
master latch
slave latch


clkInv
clk
in
★
Q
m
w



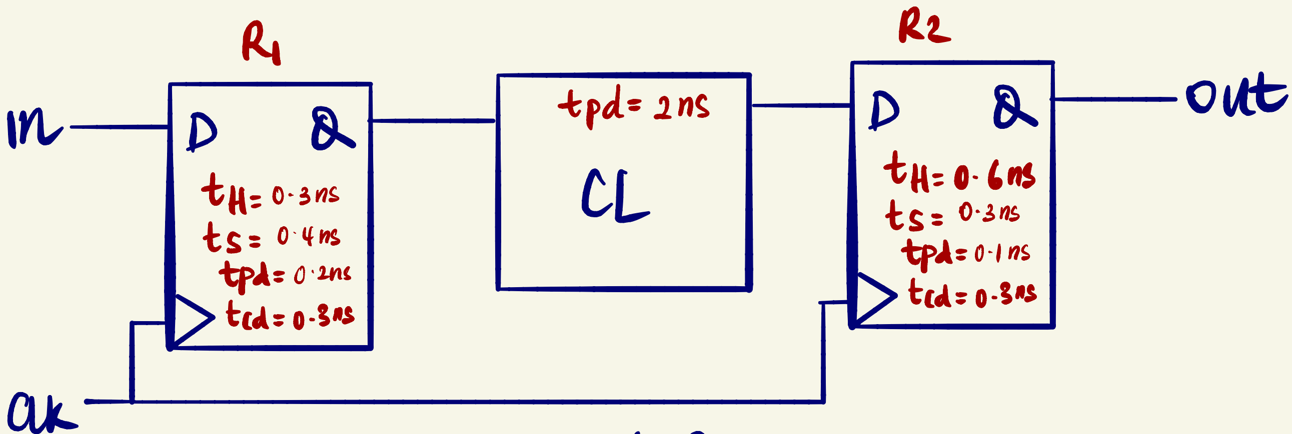


t_{CD} of master latch >

t_{Hold} slave latch

→ for dynamic discipline to apply

case 1



$\left.\begin{array}{l} \text{overall } t_{pd} = t_{pd}\,R_2 = 0.1 \\ \text{overall } t_{cd} = t_{cd}\,R_2 = 0.3 \end{array}\right\}$ sequential logic

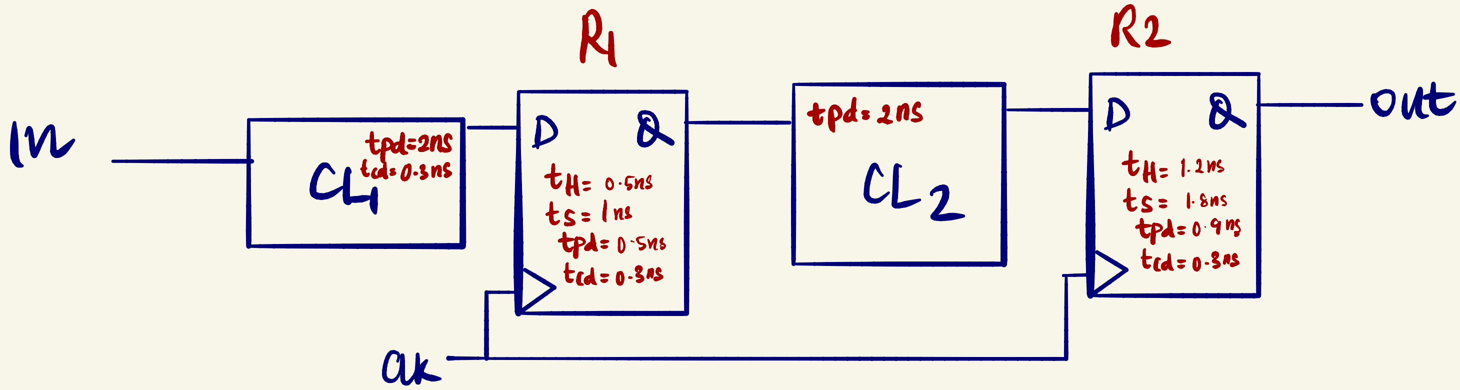
min t_{cd} CL $= t_H R_2 - t_{cd} R_1 = 0.6 - 0.3 = 0.3$

min clk period $= t_{pd} R_1 + t_{pd}$ CL $+ t_S R_2 = 0.2 + 2 + 0.3 = 2.5$

t_H input $= t_H\ R_1 = 0.3$

t_S input $= t_S\ R_1 = 0.4$

case 2



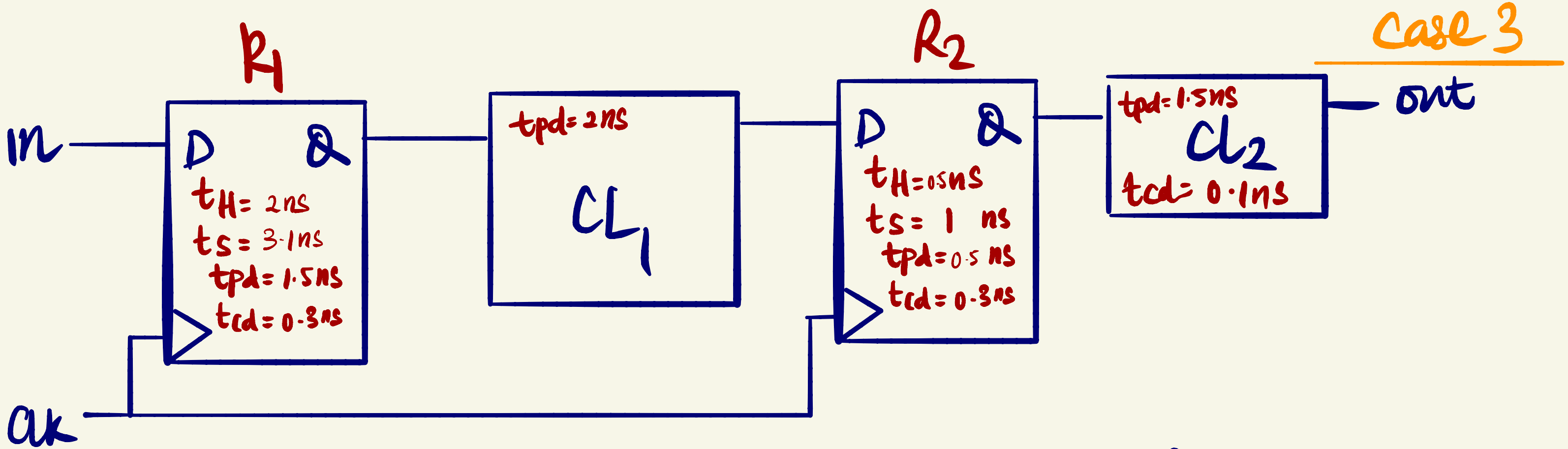
$$\left.\begin{array}{l} \text{overall } t_{pd} = t_{pd}\,R_2 = 0.9 \\ \text{overall } t_{cd} = t_{cd}\,R_2 = 0.3 \end{array}\right\} \text{sequential logic}$$

$$\text{min } t_{cd}\,CL_2 = t_H\,R_2 - t_{cd}\,R_1 = 1.2 - 0.3 = 0.9$$

$$\text{min clk period} = t_{pd}\,R_1 + t_{pd}\,CL_2 + t_s\,R_2 = 0.5 + 2 + 1.8 = 4.3$$

$$t_H \text{ input} = t_H\,R_1 - t_{cd}\,CL_1 = 0.5 - 0.3 = 0.2$$

$$t_s \text{ input} = t_s\,R_1 + t_{pd}\,CL_1 = 2 + 1 = 3$$



overall $t_{pd} = t_{pd}R_2 + t_{pd}CL_2 = 0.5 + 1.5 = 2$

overall $t_{cd} = t_{cd}R_2 + t_{cd}CL_2 = 0.3 + 0.1 = 0.4$

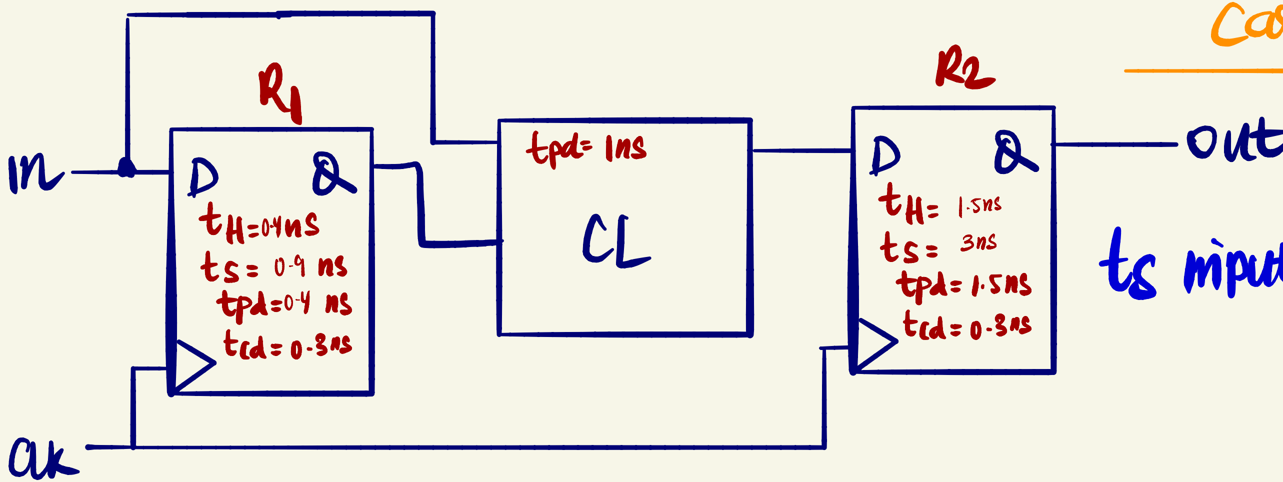
min $t_{cd}CL_1 = t_HR_2 - t_{cd}R_1 = 0.5 - 0.3 = 0.2$

min clk period $= t_{pd}R_1 + t_{pd}CL_2 + t_SR_2 = 1.5 + 2 + 1 = 4.5$

t_H input $= t_HR_1 = 2$

t_S input $= t_SR_1 = 3.1$

Case 1 + case 2



$$t_s \text{ input} = \begin{cases} t_s R_1 = 0.9 \\ t_s R_2 + t_{pd} CL = 3 + 1 = 4 \end{cases}$$

$$\left.\begin{aligned} \text{overall } t_{pd} &= t_{pd} R_2 = 1.5 \\ \text{overall } t_{cd} &= t_{cd} R_2 = 0.3 \end{aligned}\right\} \text{sequential logic}$$

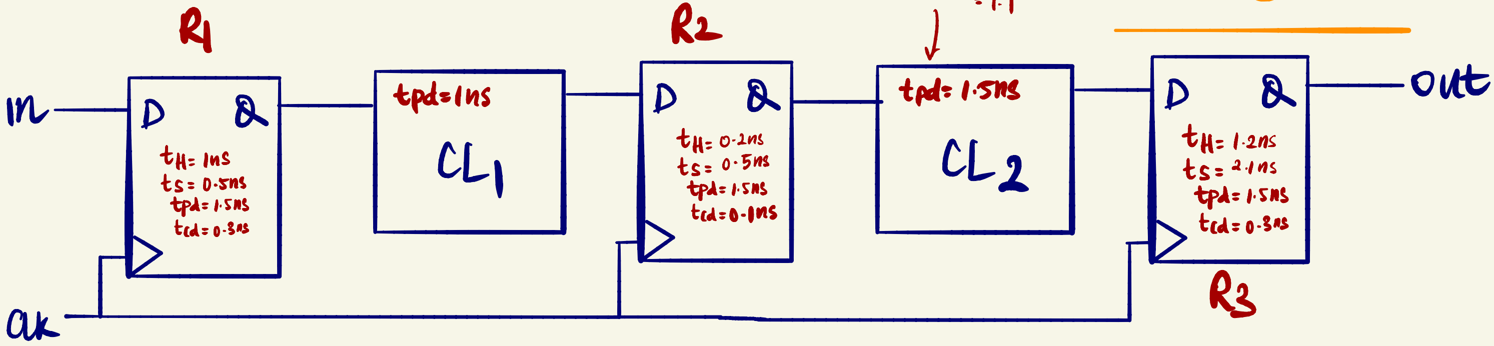
$$\text{min } t_{cd} CL = t_H R_2 - t_{cd} R_1 = 1.5 - 0.3 = 1.2$$

$$\text{min clk period} = t_{pd} R_1 + t_{pd} CL_2 + t_s R_2 = 0.4 + 1 + 3 = 4.4$$

$$t_H \text{ input} = \begin{cases} t_H R_1 = 0.4 \\ t_H R_2 - t_{cd} CL = 1.5 - 1.2 = 0.3 \end{cases}$$

2X Case 1

min $t_{cd}\ CL_2 = t_H R_3 - t_{cd} R_2$
$= 1.2 - 0.1$
$= 1.1$



$$\left.\begin{aligned}\text{overall } t_{pd} &= t_{pd} R_3 = 1.5 \\ \text{overall } t_{cd} &= t_{cd} R_3 = 0.3\end{aligned}\right\}\text{ sequential logic}$$

time cannot be -ve so clamp to 0

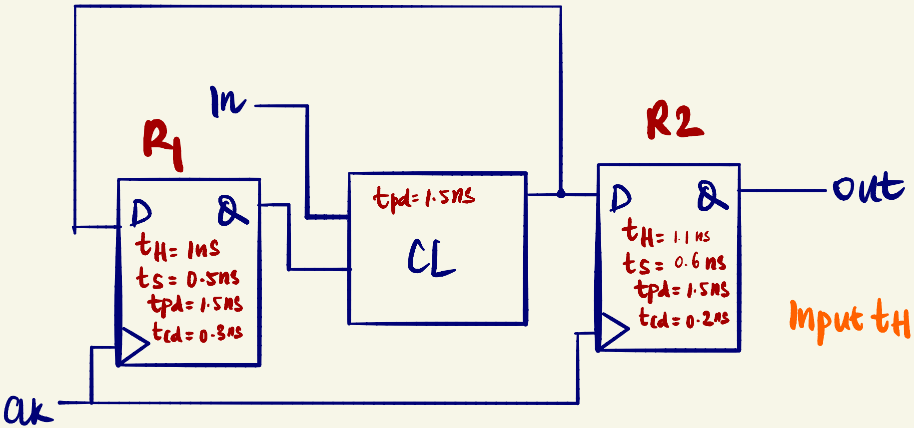
$$\text{min } t_{cd}\ CL_1 = t_H R_2 - t_{cd} R_1 = 0.2 - 0.3 = 0$$

$$\text{min clk period} = \text{max}\begin{cases} t_{pd} R_1 + t_{pd}\ CL_1 + t_s R_2 = 3 \\ t_{pd} R_2 + t_{pd}\ CL_2 + t_s R_3 = 5.1 \end{cases} = 5.1$$

t_H input $= t_H R_1 = 1$

t_s input $= t_s R_1 = 0.5$

Case 1+ case looped



$$\text{Input } t_s = \max \begin{cases} t_s R_2 + t_{pd} CL \\ t_s R_1 + t_{pd} CL \end{cases} = \max \begin{cases} 0.6 + 1.5 = 2.1 \\ 0.5 + 1.5 = 2 \end{cases} \Downarrow 2.1$$

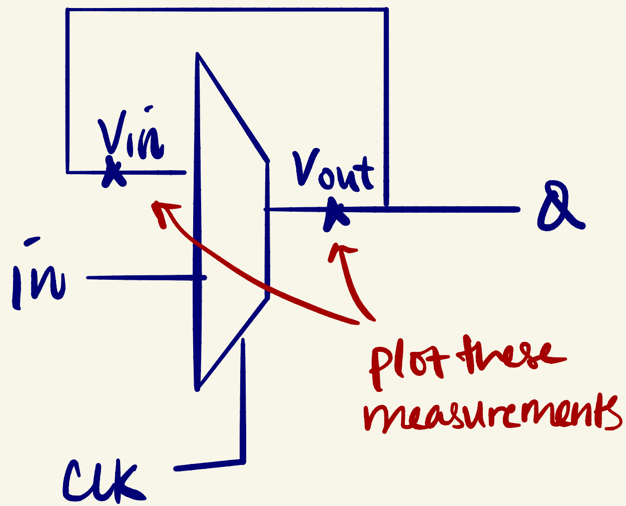
$$\text{Input } t_H = \max \begin{cases} t_H R_1 - t_{cd} CL = 1 - 0.8 = 0.2 \\ t_H R_2 - t_{cd} CL = 1.1 - 0.8 = 0.3 \end{cases} \Downarrow 0.3$$

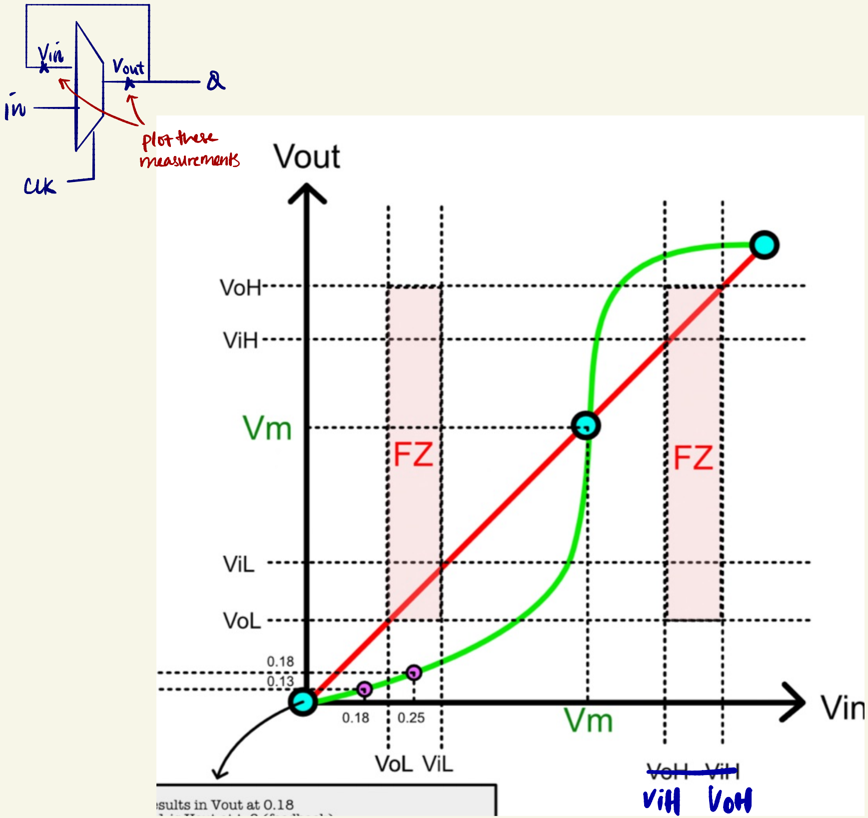
$$\left.\begin{aligned} \text{overall } t_{pd} &= t_{pd} R_2 = 1.5 \\ \text{overall } t_{cd} &= t_{cd} R_2 = 0.2 \end{aligned}\right\} \text{sequential logic}$$

use it here

$$\min t_{cd} CL = \max \begin{cases} t_H R_2 - t_{cd} R_1 = 1.1 - 0.3 = 0.8 \\ t_H R_1 - t_{cd} R_1 = 1 - 0.3 = 0.7 \end{cases} = 0.8$$

$$\min clk = \max \begin{cases} t_{pd} R_1 + t_{pd} CL + t_s R_2 = 1.5 + 1.5 + 0.6 = 3.6 \\ t_{pd} R_1 + t_{pd} CL + t_s R_1 = 1.5 + 1.5 + 0.5 = 3.5 \end{cases} = 3.6$$


Vin
Vout
Q
in
CLK
plot these measurements



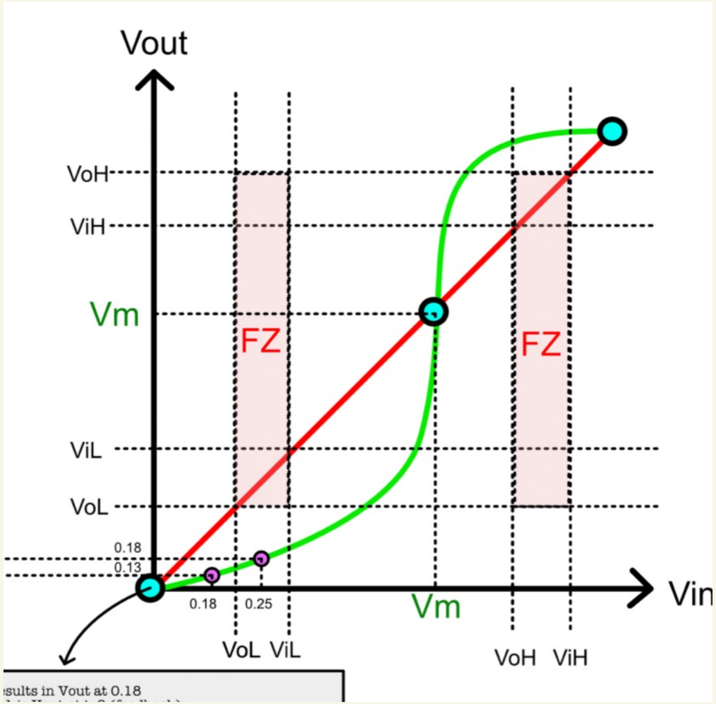
given:

$$\left.\begin{aligned} \text{at } t = t_0 \rightarrow V_{in} &= 0.18V \\ V_{out} &= 0.13 \end{aligned}\right\} \text{first loop}$$

$$\left.\begin{aligned} \text{at } t = t_1 \rightarrow V_{in} &= V_{out}(t=0) + \text{noise} \\ &= 0.14 \\ V_{out} &= 0.05 \end{aligned}\right\} \text{2nd loop}$$

$$\left.\begin{aligned} \text{at } t = t_2 \rightarrow V_{in} &= V_{out}(t=1) + \text{noise} \\ &= 0.04 \\ V_{out} &\approx 0 \end{aligned}\right\} \text{3rd loop}$$

$$\underbrace{\phantom{V_{out} \approx 0}}_{\text{stable}}$$



METASTABLE STATE

given:

at $t = t_0 \rightarrow V_{in} = V_m$

$V_{out} = V_m$

first loop

at $t = t_1 \rightarrow V_{in} = V_{out}(t=0)$ + noise

$= V_m + 0.01$

$V_{out} = V_m + 0.02$

2nd loop

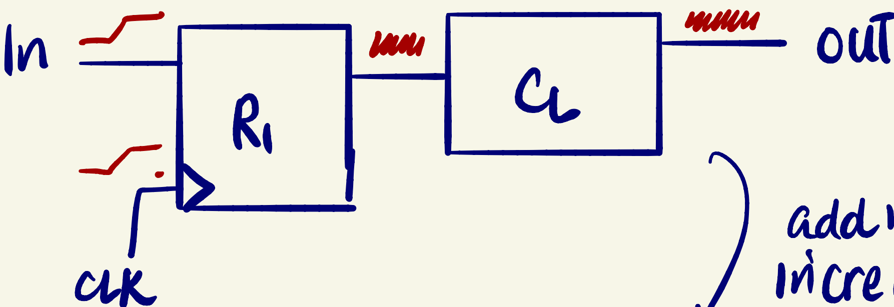
at $t = t_2 \rightarrow V_{in} = V_{out}(t=1)$ + noise

$= V_m - 0.01$

$V_{out} = V_m + 0.02$

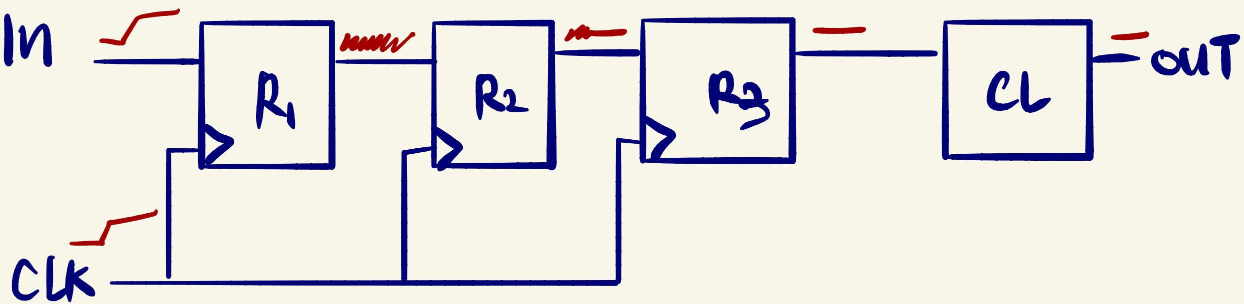
3rd loop

oscillating



we donot want unstable output

add more registers to increase wait time

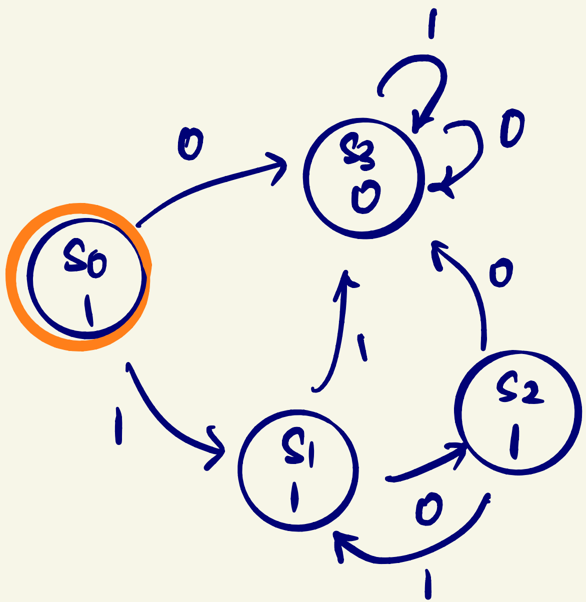


Task: Binary parser

101010 ✓
1110 ✗
0001 ✗

input	state	next state	output
0	S_0	S_3	0
1	S_0	S_1	1
0	S_1	S_2	1
1	S_1	S_3	0
0	S_2	S_3	0
1	S_2	S_1	1
0	S_3	S_3	0
1	S_3	S_3	0

Moore machine



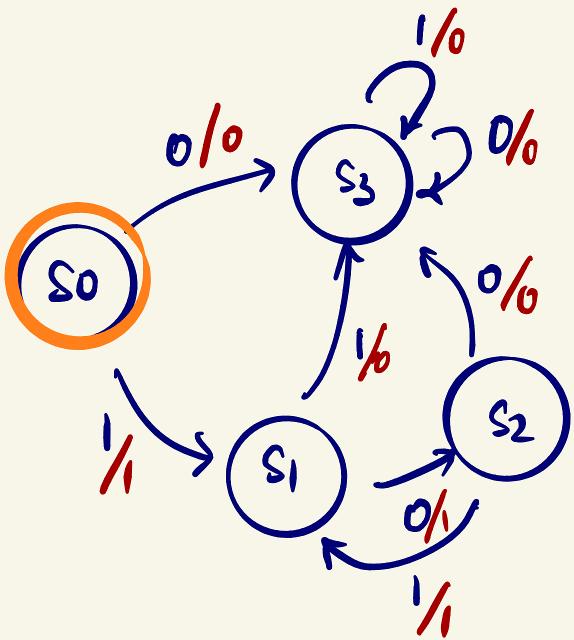
input	state	next state	output
0	S_0	S_3	0
1	S_0	S_1	1
0	S_1	S_2	1
1	S_1	S_3	0
0	S_2	S_3	0
1	S_2	S_1	1
0	S_3	S_3	0
1	S_3	S_3	0

} one state-output pair

if we have , then

this is another state-output pair

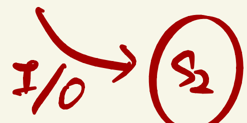
mealy machine



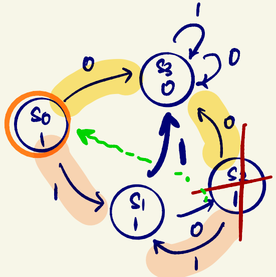
input	state	next state	output
0	S_0	S_3	0
1	S_0	S_1	1
0	S_1	S_2	1
1	S_1	S_3	0
0	S_2	S_3	0
1	S_2	S_1	1
0	S_3	S_3	0
1	S_3	S_3	0

} one per state.
if we have entrance to S_2 that produces '0', that's another "arrow" to S_2:

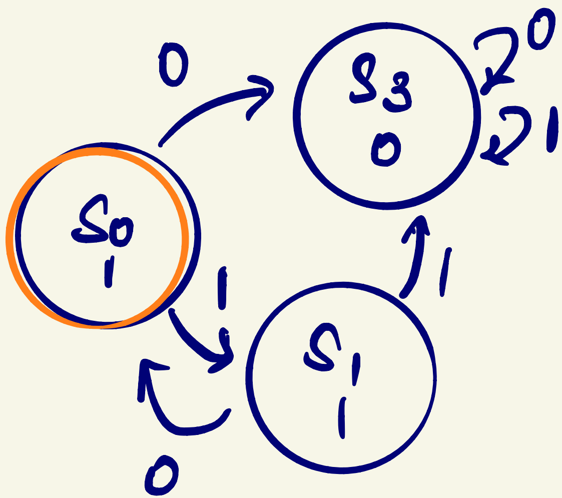
eg:



Equivalence

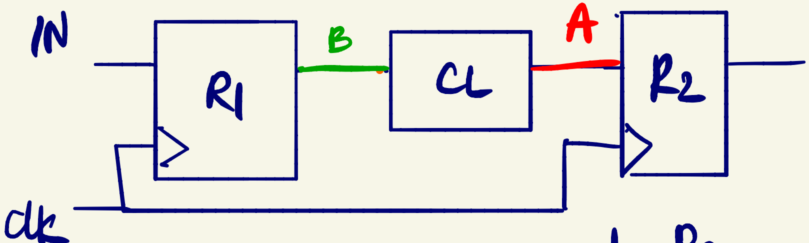


equivalent



input	state	next state	output
0	S_0	S_3	0
1	S_0	S_1	1
0	S_1	S_2	1
1	S_1	S_3	0
0	S_2	S_3	0
1	S_2	S_1	1
0	S_3	S_3	0
1	S_3	S_3	0

About min t_{cD} CL



CLK → input to R_1

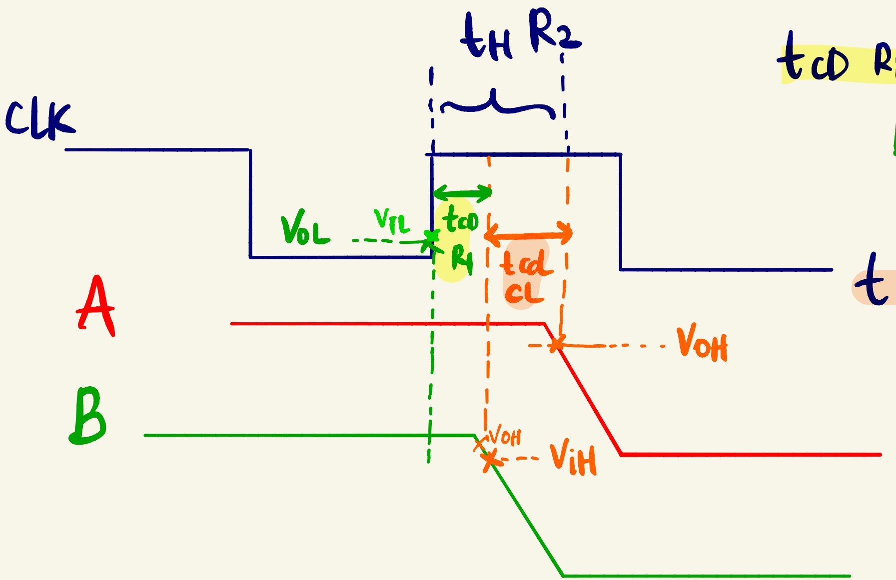
B → output of R_1

t_{cD} R_1 : from invalid clk to invalid B

B → input to CL

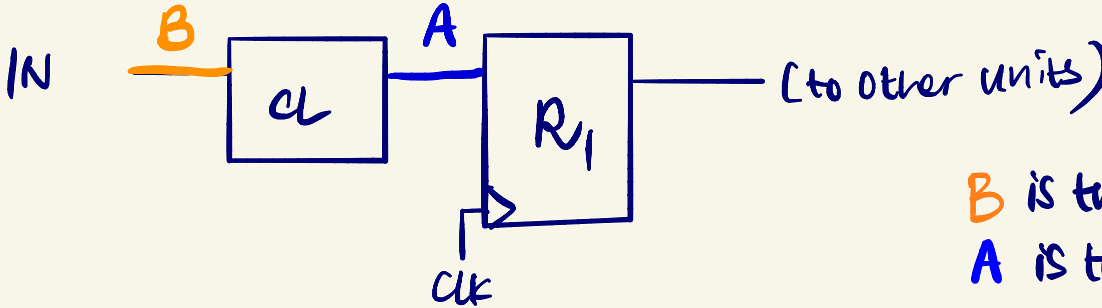
A → output of CL

t_{cD} CL : from invalid B to invalid A



from graph: $t_{HR_2} \le t_{cD\,R_1} + t_{cD\,CL} \Rightarrow t_{cD\,CL} = t_{HR_2} - t_{cd\,R_1}$ #

About $t_{S\,IN}$ & $t_{H\,IN}$

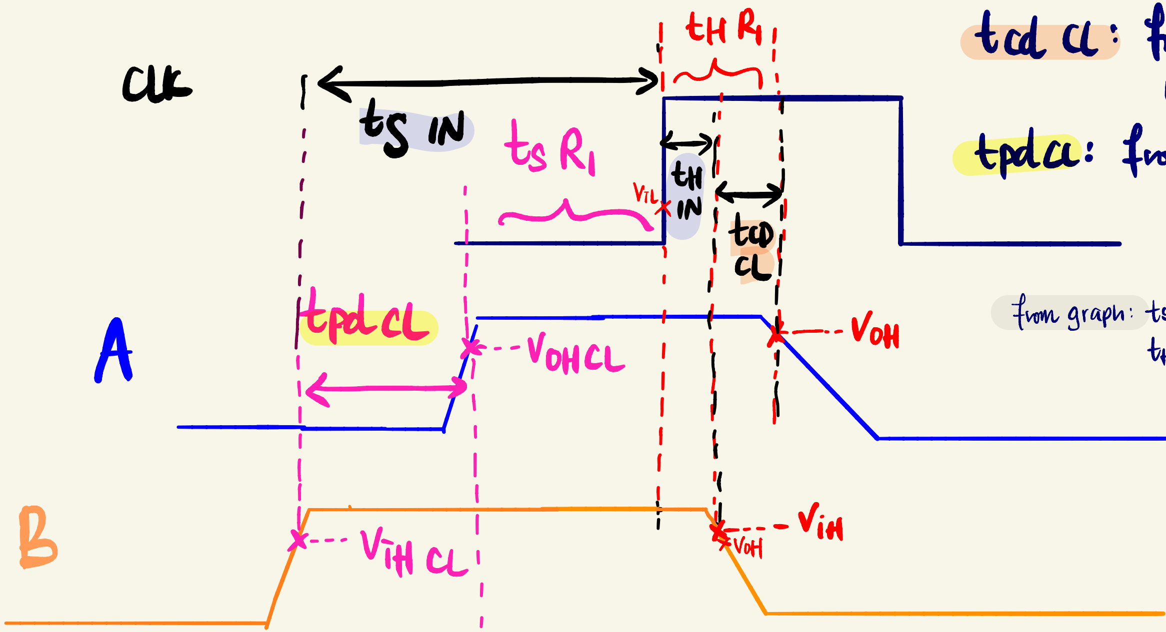


B is the input to CL

A is the output of CL

t_{cd} CL: from invalid A to invalid B

t_{pd} CL: from valid A to valid B



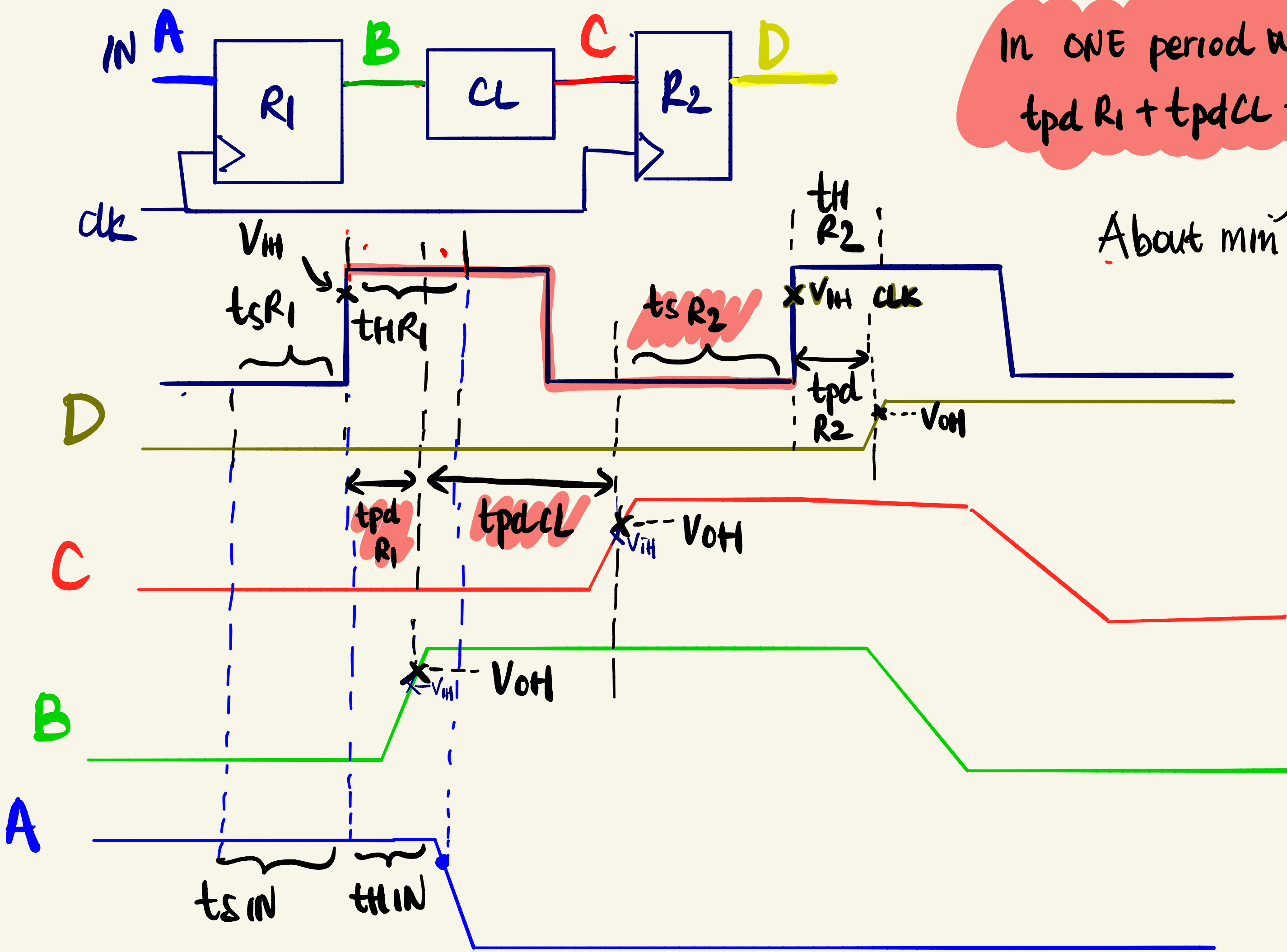
from graph: $t_{S\,IN} = t_{pd\,CL} + t_{S\,R_1}$

$t_{H\,IN} = t_{H\,R_1} - t_{CD\,CL}$

In ONE period we must fit:

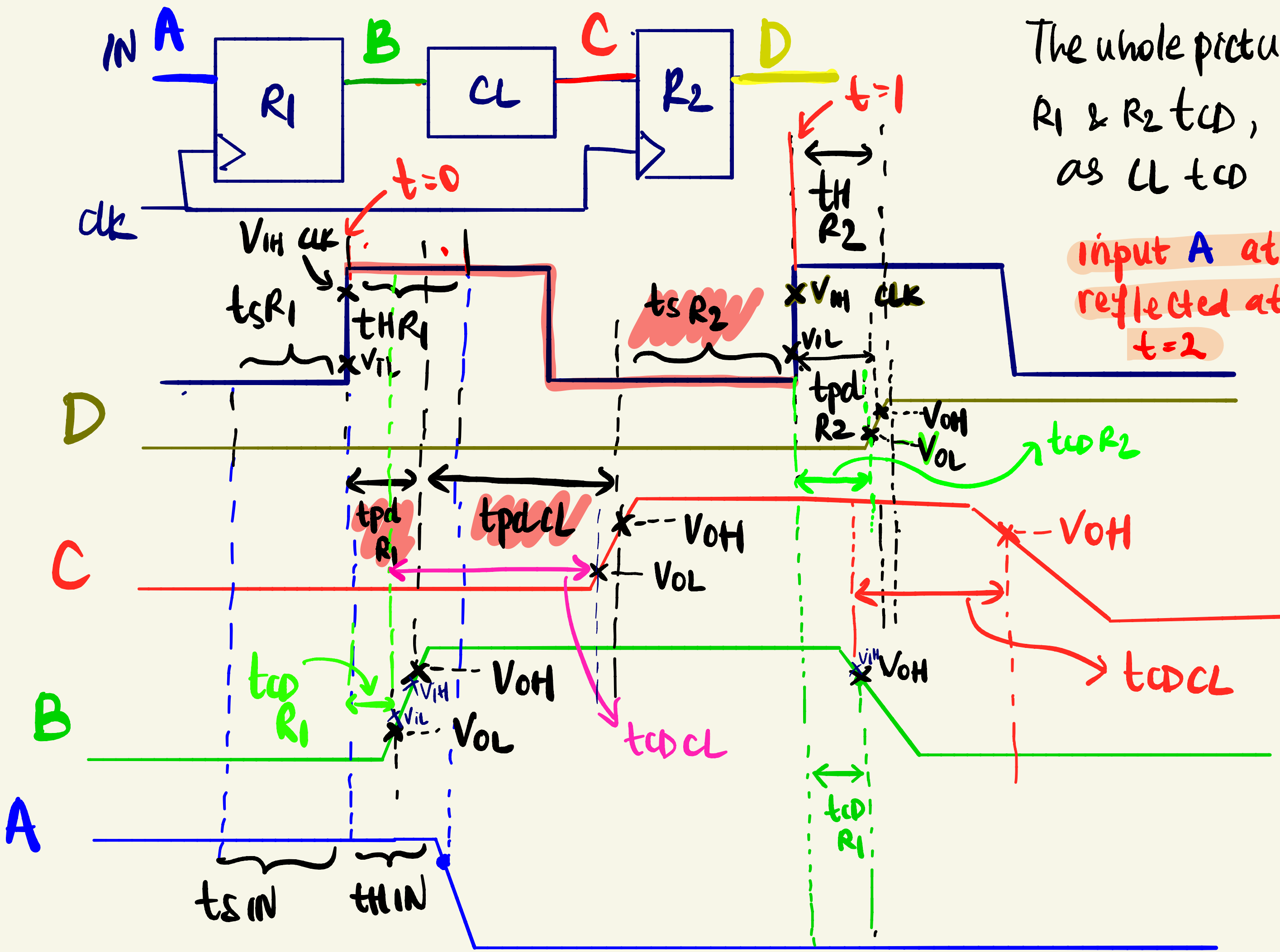
$t_{pd}R_1 + t_{pd}CL + t_sR_2$

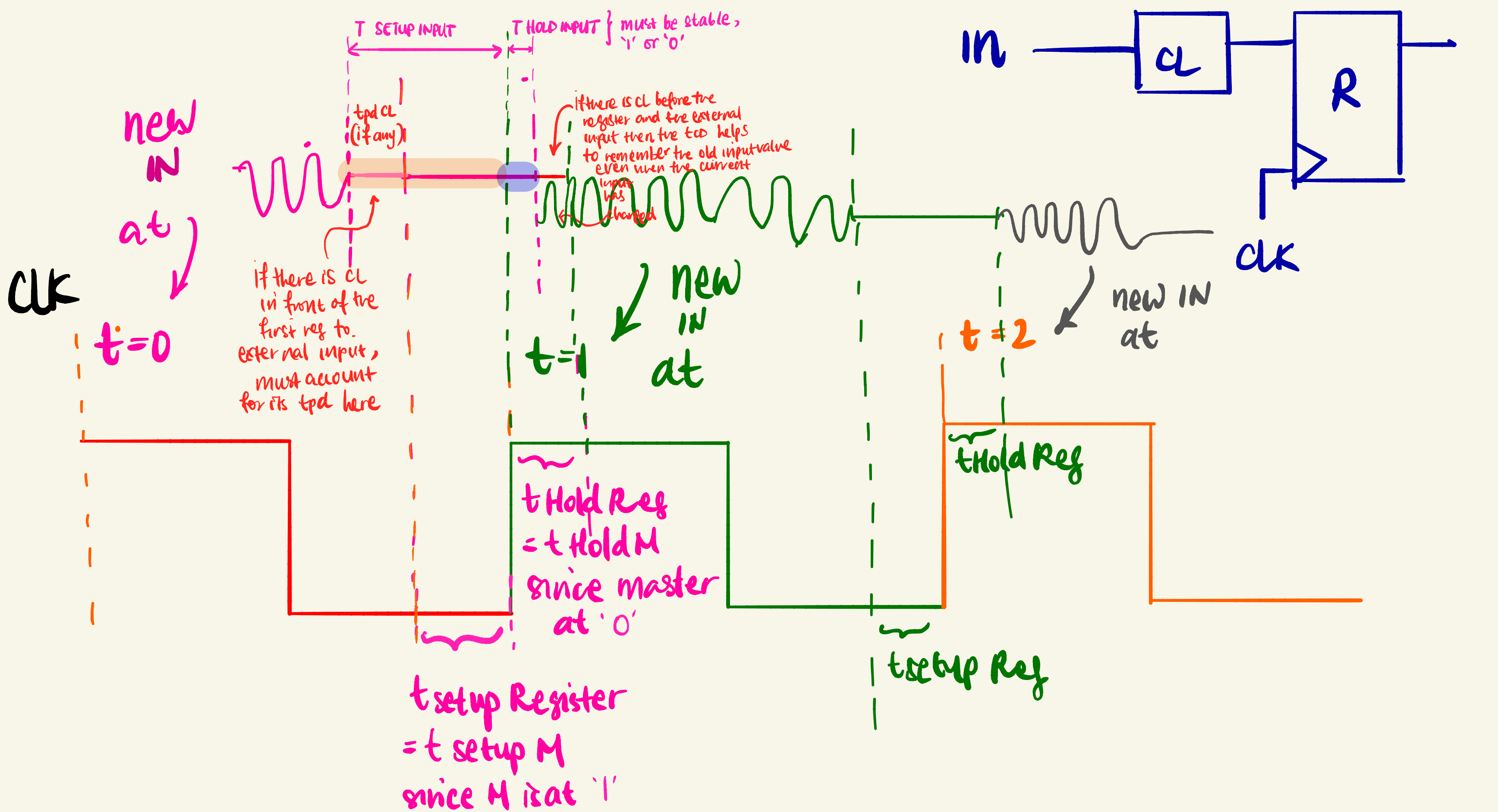
About min clk period

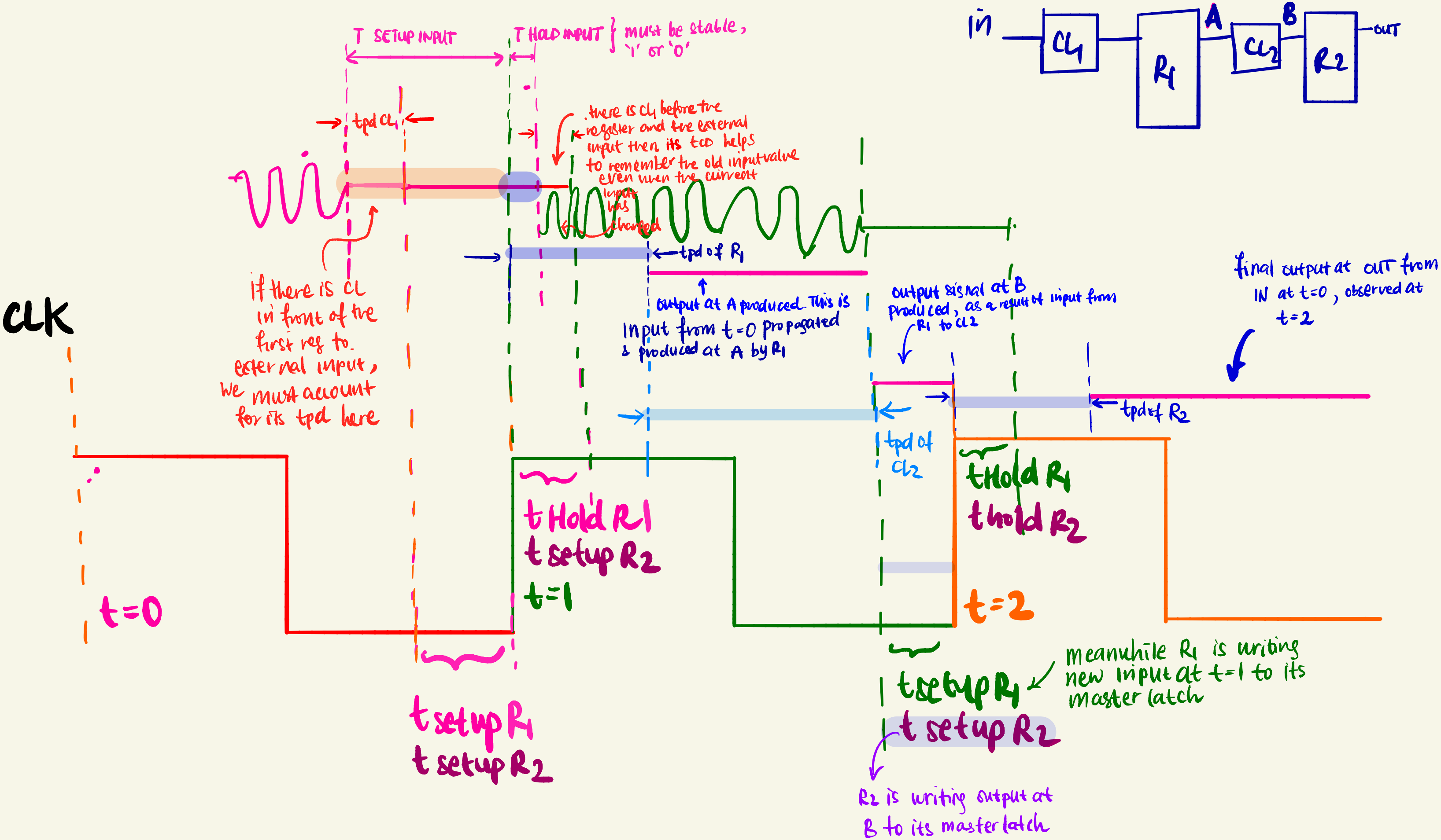


The whole picture with R_1 & R_2 t_{CD}, as well as CL t_{CD}

input A at t=1 is reflected at D at t=2




T SETUP INPUT
T HOLD INPUT
must be stable, '1' or '0'
tpd CL (if any)
new IN at
CLK
t=0
If there is CL in front of the first reg to external input, must account for its tpd here
If there is CL before the register and the external input then the tcd helps to remember the old input value even when the current input has changed
t=1
new IN at
t Hold Reg = t Hold M since master at '0'
t setup Register = t setup M since M is at '1'
t setup Reg
t=2
t Hold Reg
new IN at
IN
CL
R
CLK



in
CL1
R1
A
CL2
B
R2
OUT
T SETUP INPUT
T HOLD INPUT } must be stable, '1' or '0'
tpd CL1
there is CL1 before the register and the external input then its tcd helps to remember the old input value even when the current input was changed
If there is CL in front of the first reg to external input, we must account for its tpd here
CLK
t=0
tpd of R1
output at A produced. This is
input from t=0 propagated & produced at A by R1
tHold R1
t setup R2
t=1
t setup R1
t setup R2
output signal at B produced, as a result of input from R1 to CL2
tpd of CL2
tHold R1
thold R2
t=2
tpd of R2
final output at OUT from IN at t=0, observed at t=2
t setup R1
t setup R2
meanwhile R1 is writing new input at t=1 to its master latch
R2 is writing output at B to its master latch