REQUIREMENTS NOT MET

<insert any requirements not met, i.e., problems not solved, if applicable (if not applicable, write “N/A”)>

PROBLEMS ENCOUNTERED

<insert a brief summary of *all* problems encountered>

THE ABOVE SHOULD BE LIMITED TO THE FIRST PAGE, AND NOTHING ELSE SHOULD BE INCLUDED, WHICH ALSO IMPLIES THAT THIS SENTENCE OF TEXT SHOULD BE REMOVED.

HOMEWORK EXERCISES

1. Complete Exercises in DAD WaveForms Tutorial
   a. Exercise 1: Simple Circuit using Switches and LEDs

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Table 1: Exercise 1 - NOR Gate Truth Table, C = /(A + B)

A(H)	B(H)	C(H)
L	L	H
L	H	L
H	L	L
H	H	L

Table 2: Exercise 1 - NOR Gate Voltage Table, C = /(A + B)

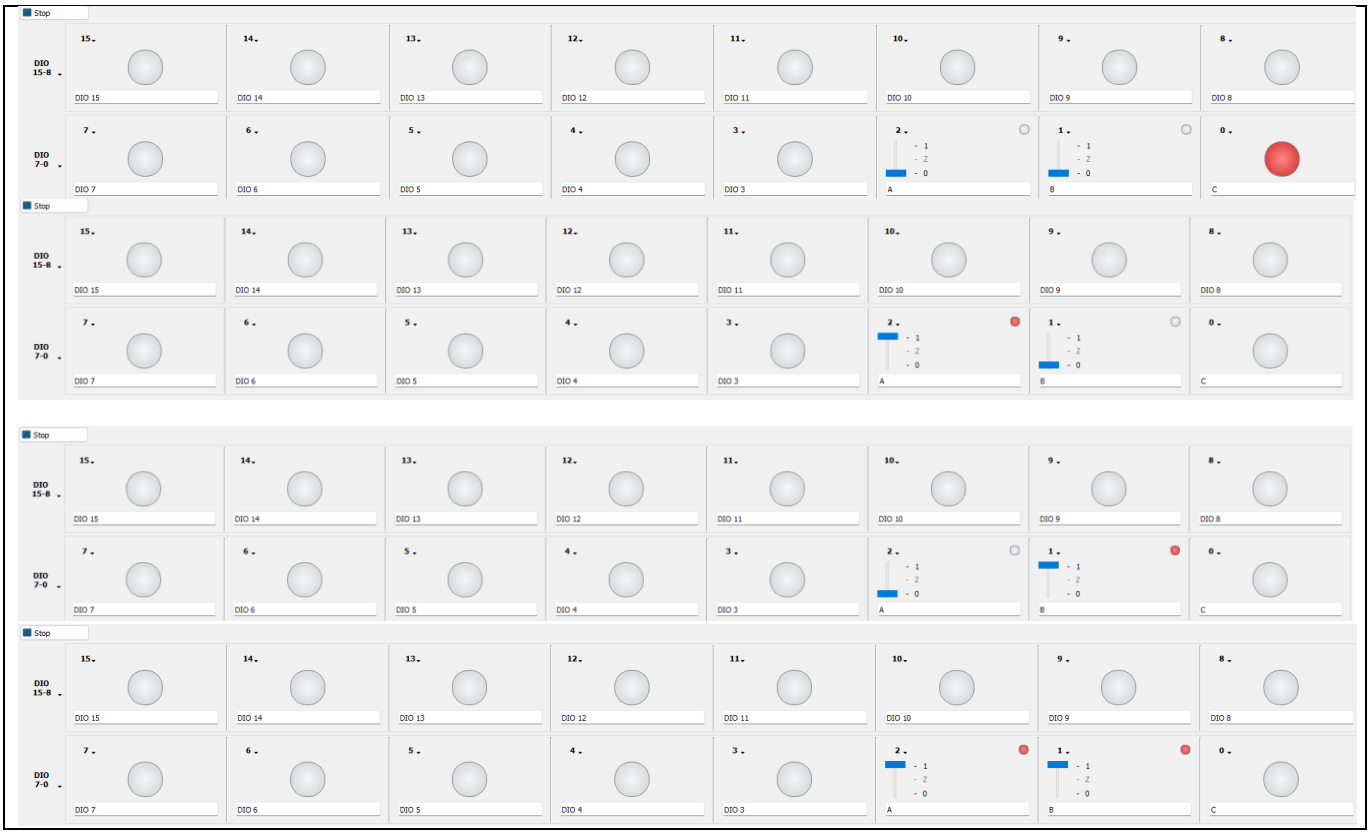

Table 3: Exercise 1 - Static I/O Results from NOR Gate

   b. Exercise 2: Pattern Generator

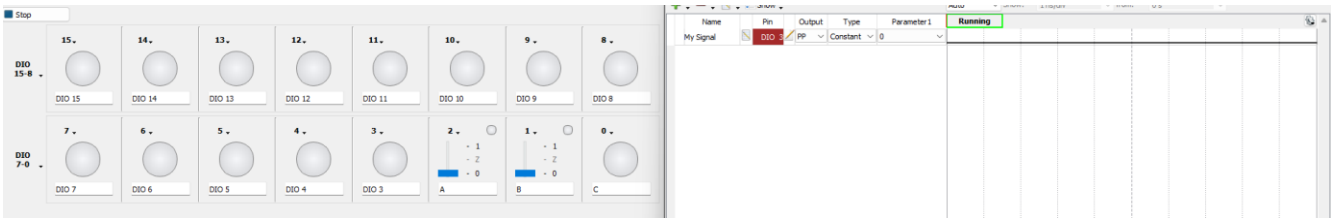

Table 4: Exercise 2 - Results from Pattern Generator Input 0

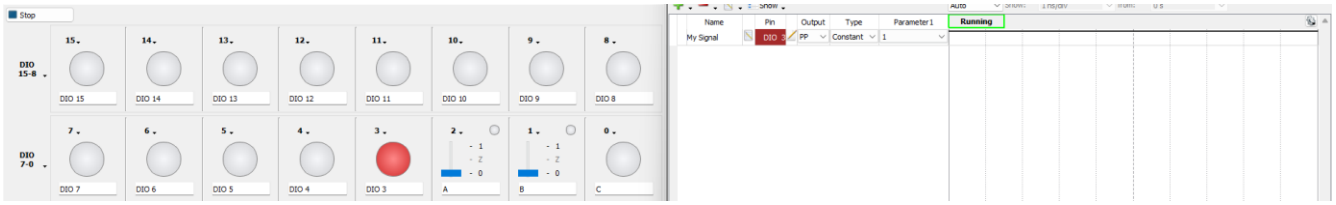

Table 5: Exercise 2 - Results from Pattern Generator Input 1

c. Exercise 3: Buses

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Table 6: Exercise 3 - NOR Gate Truth Table, C = /(A + B)

A(H)	B(H)	C(H)
L	L	H
L	H	L
H	L	L
H	H	L

Table 7: Exercise 3 - NOR Gate Voltage Table, C = /(A + B)

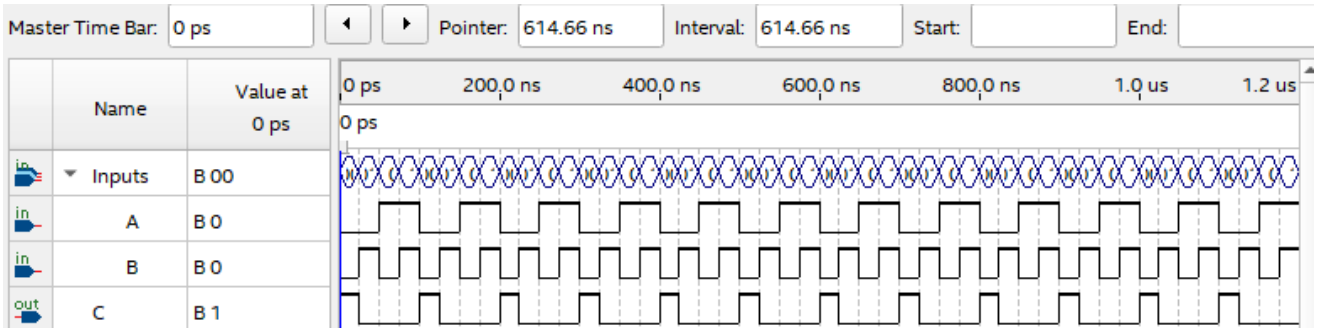

Table 8: Exercise 3 - Quartus Functional Simulation of NOR Gate

d. Logic Analyzer

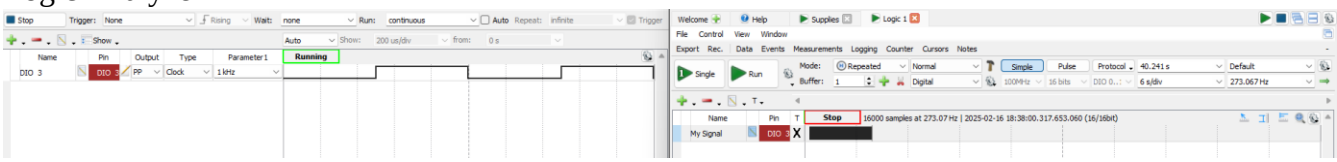

Table 9: Logic Analyzer for Output 3

e. Setting Up a Bus

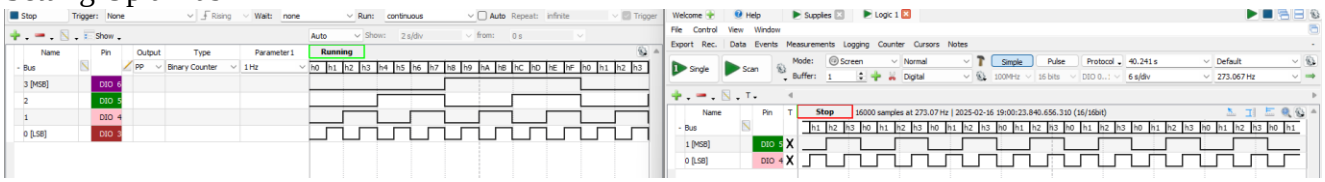

Table 10: Exercise 4 - Pattern Generator in Binary Count and Logic Analyzer with no Clock or Enable

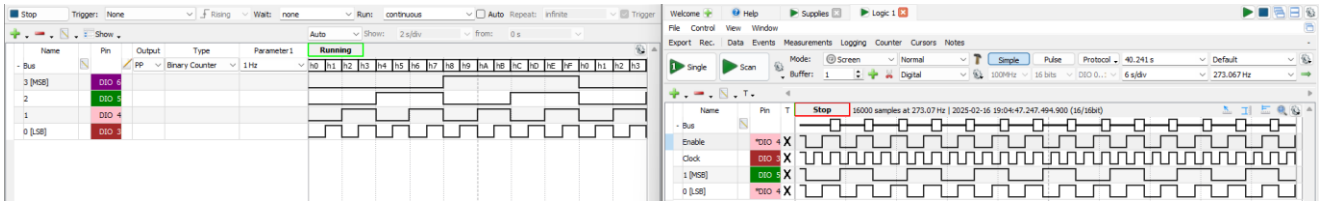

Table 11: Exercise 4 - Pattern Generator in Binary Count and Logic Analyzer with Clock DIO4 High and Enable DIO3 Rising

f. Pattern Generator Bus and Logic Analysis Bus

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Table 12: NOR Gate Truth Table, C = /(A + B)

A(H)	B(H)	C(H)
L	L	H
L	H	L
H	L	L
H	H	L

Table 13: NOR Gate Voltage Table, C = /(A + B)

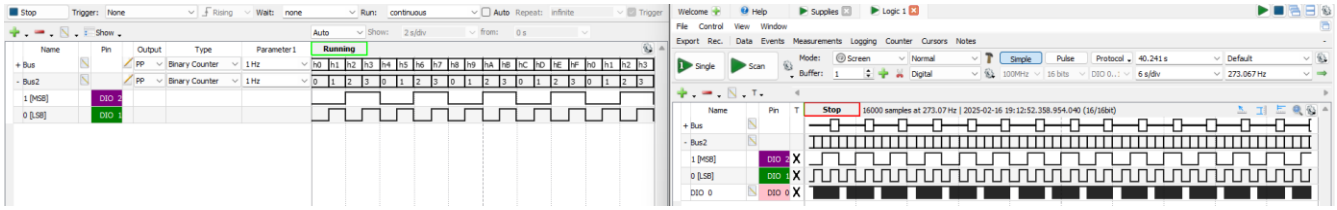

Table 14: Logic Analysis of NOR Gate

g. Kk;l

2. Quartus

a.

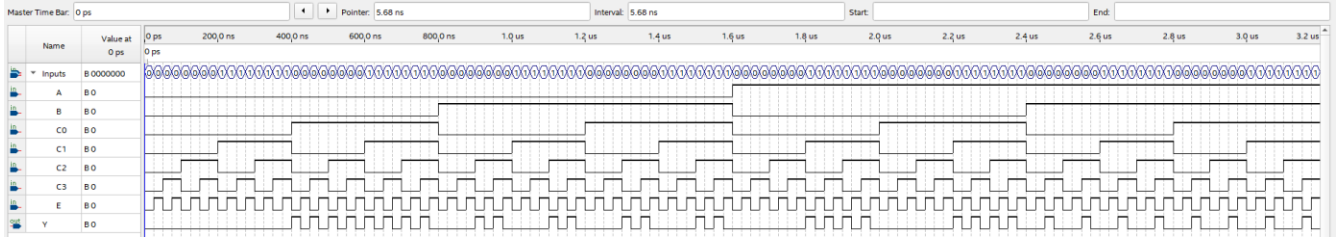

Table 15: Quartus Functional Smulation of MUX

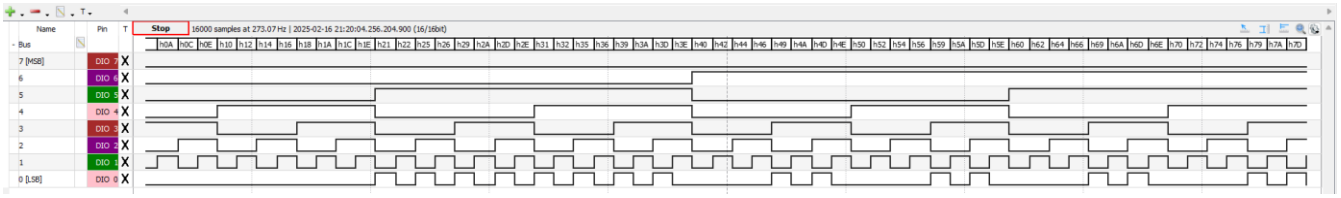

Table 16: WaveForm Logic Analysis of MUX

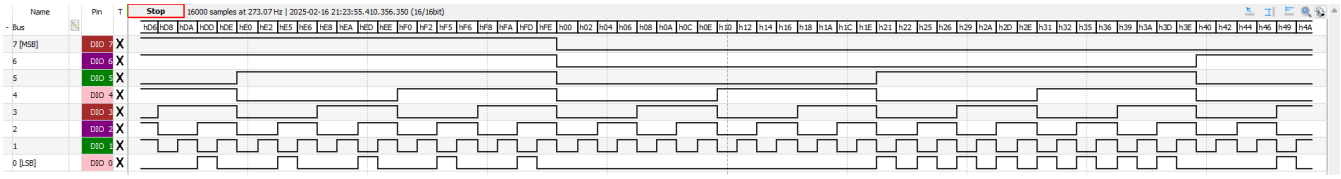

Table 17: Waveform Logic Analysis of MUX

b.

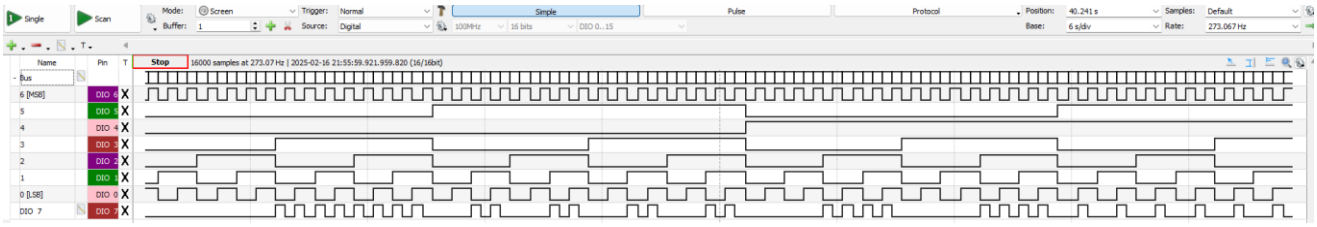

Table 18: MUX Logic Analysis of MUX with specified inputs

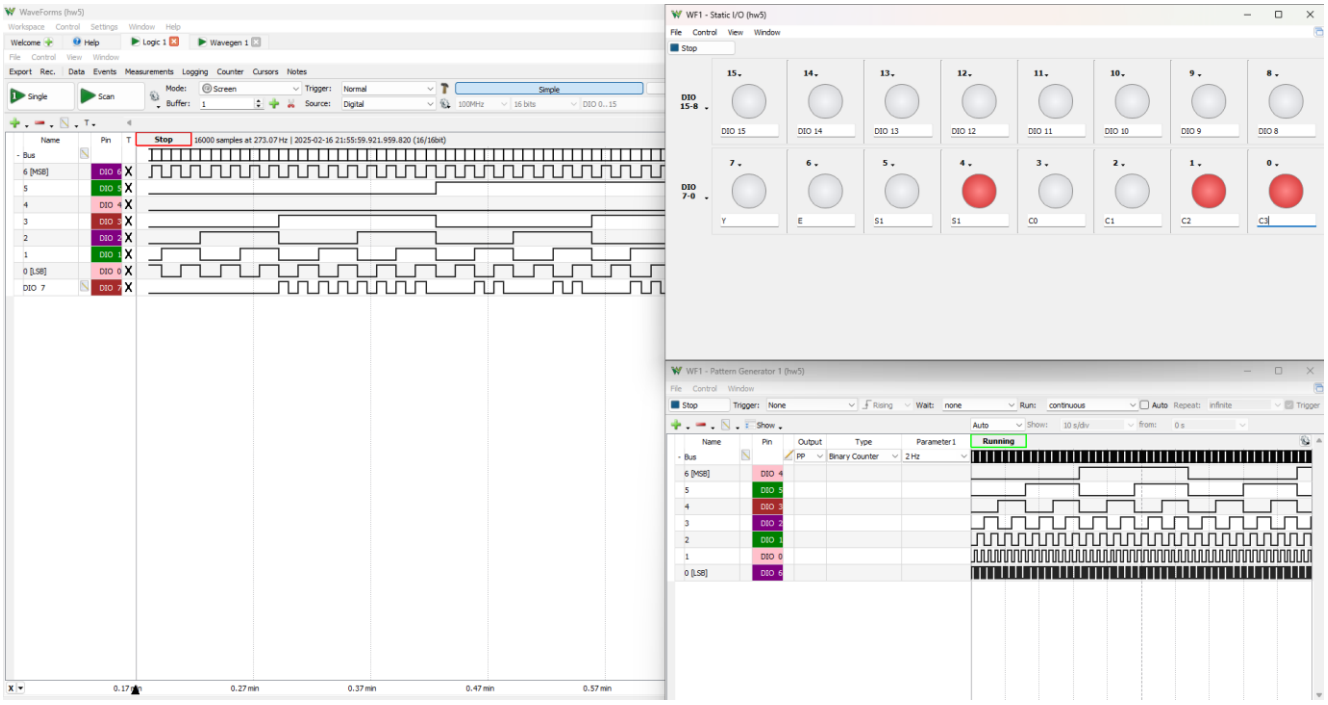

Table 19: MUX Logic Analysis of MUX with More of the Setup