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Lab Quiz 4

Problem: Part 1

Design a 4-bit shift register that has the following functionality:

00: Hold values

01: Read values from input bus

10: Arithmetic shift right 1 bit

11: Rotate all values right 1 bit (shift right 1 bit, but the least significant bit becomes the new most significant bit).

Design this register in Quartus and be prepared to show a simulation. You do not need to build it on your breadboard.

Problem: Part 2

In this part, you will implement a new table/program using the same RALU that you built in Lab 4 (no new hardware additions!) Like the pre-lab, you will use your DAD to implement in the pattern generator. If you did not complete your lab, you can write the program for partial credit. Necessary tables to form control words can be found at the end of this document. Here is the “pseudocode” you will implement. Keep in mind things shown on one line may need multiple cycles in your design.

A = 6

B = $B

A = A + B

A = A * 4

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Submit to Lab - Quiz 4 - Generic

- Quartus archive.
- Screenshot of bdf.
- Screenshot of simulation.

Submit to Lab - Quiz 4 - Phone

- Picture of any scratch paper used.

MSA/MSB1	MSA/MSB0	Bus Selected as Input to REGA/REGB
0	0	INPUT Bus
0	1	REGA Bus
1	0	REGB Bus
1	1	OUTPUT Bus

Table 2: Input source MUXs for Registers A and B.

MSC2:0	Action
000	REGA Bus to OUTPUT Bus
001	REGB Bus to OUTPUT Bus
010	complement of REGA Bus to OUTPUT Bus
011	bit wise AND REGA/REGB Bus to OUTPUT Bus
100	bit wise OR REGA/REGB Bus to OUTPUT Bus
101	sum of REGA Bus & REGB Bus to OUTPUT Bus
110	shift REGA Bus left one bit to OUTPUT Bus
111	shift REGA Bus right one bit to OUTPUT Bus without sign extension

Table 3: ALU function selection MUX (for MUX C).

A dual 4-Input mux is a 74153 in Quartus