EEL 3701C: Digital Logic & Computer Systems
Revision **0**
Lab **2** Report: **MSI Circuits**

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REQUIREMENTS NOT MET

N/A

VIDEO FILE LINK

https://drive.google.com/file/d/15XCk-p2LTxNXuliOADmf0P1iI8_1zABs/view?usp=sharing

PROBLEMS ENCOUNTERED

There were no problems encountered.

FUTURE WORK/APPLICATIONS

This lab primarily focused on the functions and uses of the MUX and Decoder (Hex to Seven-Segment Display), these components have several applications in constructing more complex circuits such as in future labs, with the counter and flip flops.

PRE-LAB QUESTIONS OR EXERCISES

PART 1: INTRODUCTION TO MULTIPLEXERS

Table 1: Truth Table for Part 1

S0	D1	D0	Y
0	*	0	0
0	*	1	1
1	0	*	0
1	1	*	1

SOP: Y = /S0*D0 + S0*D1

POS: Y = (S0 + D0)*(/S0 + D1)

Table 2: Voltage Table for Part 1

S0 (H)	D1 (H)	D0 (L)	Y (L)
L	*	H	H
L	*	L	L
H	L	*	H
H	H	*	L

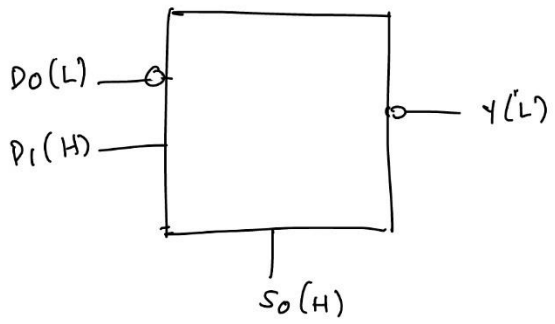


Figure 1: 2-input MUX Block Diagram

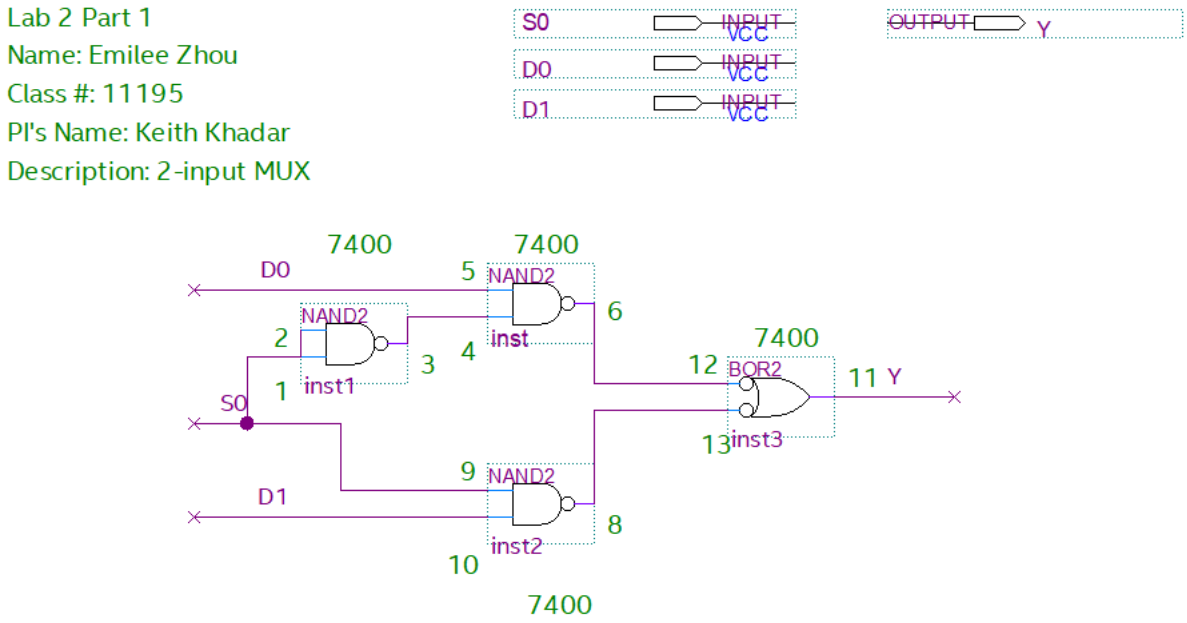


Figure 2: 2-input MUX BDF for Part 1

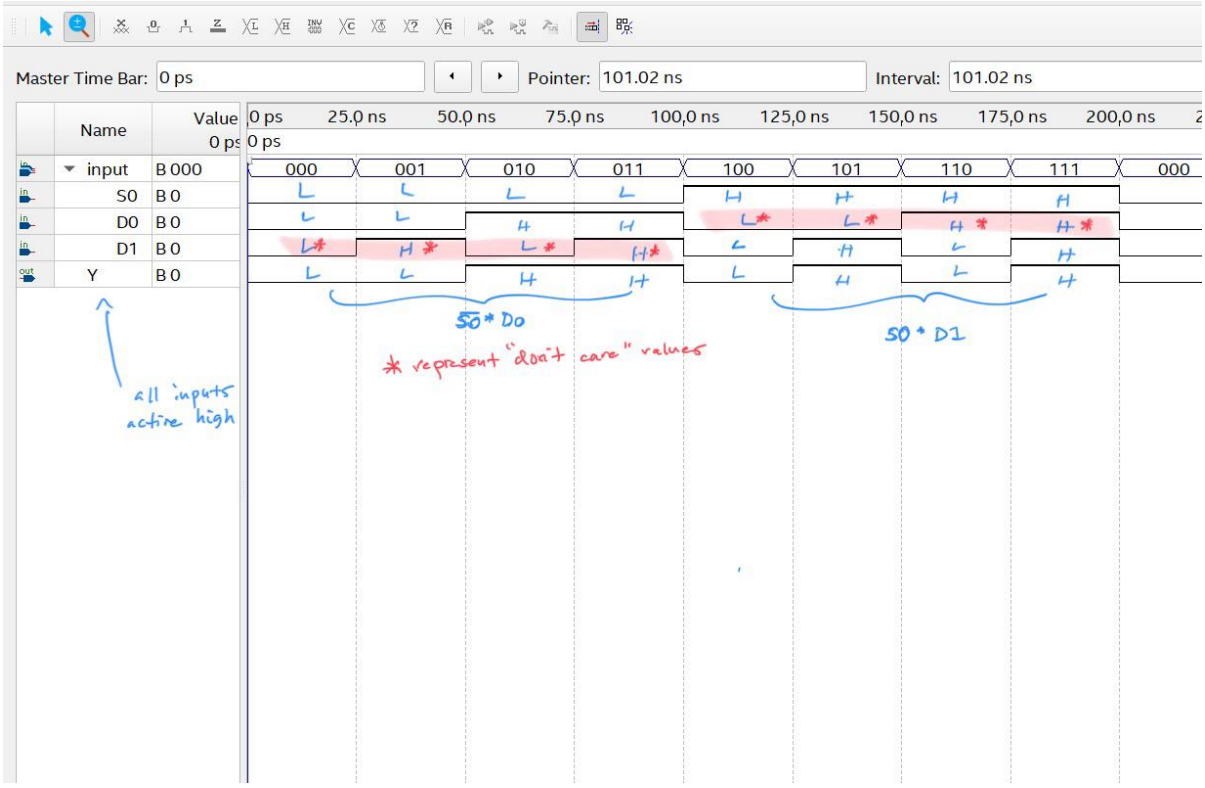


Figure 3: Function Simulation for Part 1

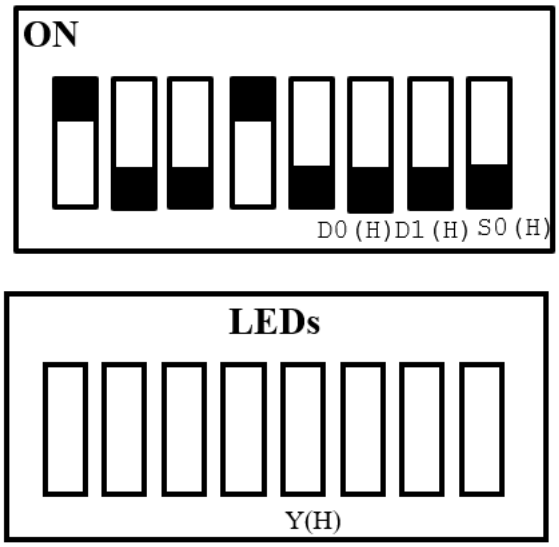


Figure 4: Switch and LED Legends for Part 1

PART 2: FOUR-INPUT MULTIPLEXER DESIGN

Table 3: Truth Table for Part 2

S1	S0	D3	D2	D1	D0	Y
0	0	*	*	*	0	0
0	0	*	*	*	1	1
0	1	*	*	0	*	0
0	1	*	*	1	*	1
1	0	*	0	*	*	0
1	0	*	1	*	*	1
1	1	0	*	*	*	0
1	1	1	*	*	*	1

POS: Y = (/S1 + /S0 + D0)*(/S1 + S0 + D1)*(S1 + /S0 + D2)*(S1 + S0 + D3)

SOP: Y = /S1*/S0*D0 + /S1*S0*D1 + S1*/S0*D2 + S1*S0*D3

Table 4: Voltage Table for Part 2

S1(H)	S0(H)	D3(H)	D2(L)	D1(H)	D0(L)	Y(H)
L	L	*	*	*	H	L
L	L	*	*	*	L	H
L	H	*	*	L	*	L
L	H	*	*	H	*	H
H	L	*	H	*	*	L
H	L	*	L	*	*	H
H	H	L	*	*	*	L
H	H	H	*	*	*	H

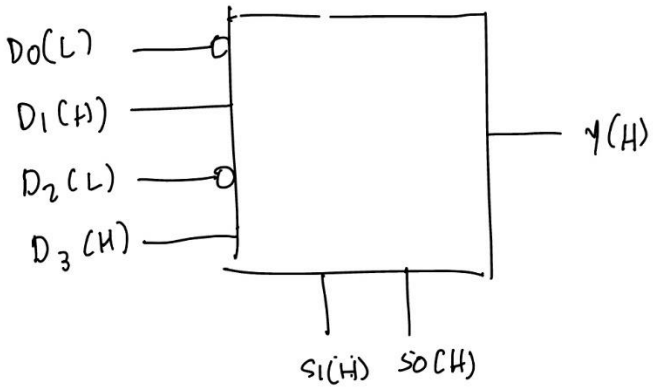


Figure 5: 4-input MUX Block Diagram for Part 2

$$Y = \overline{S1}\,\overline{S0}\,D0 + \overline{S1}\,S0\,D1 + S1\,\overline{S0}\,D2 + S1\,S0\,D3$$

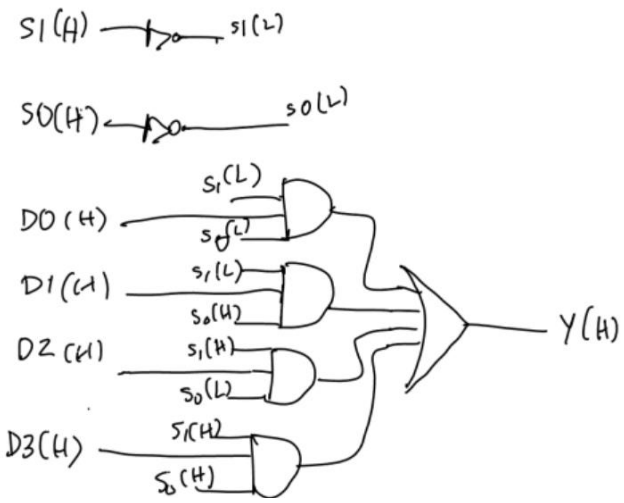


Figure 6: 4-input MUX Diagram for Part 2

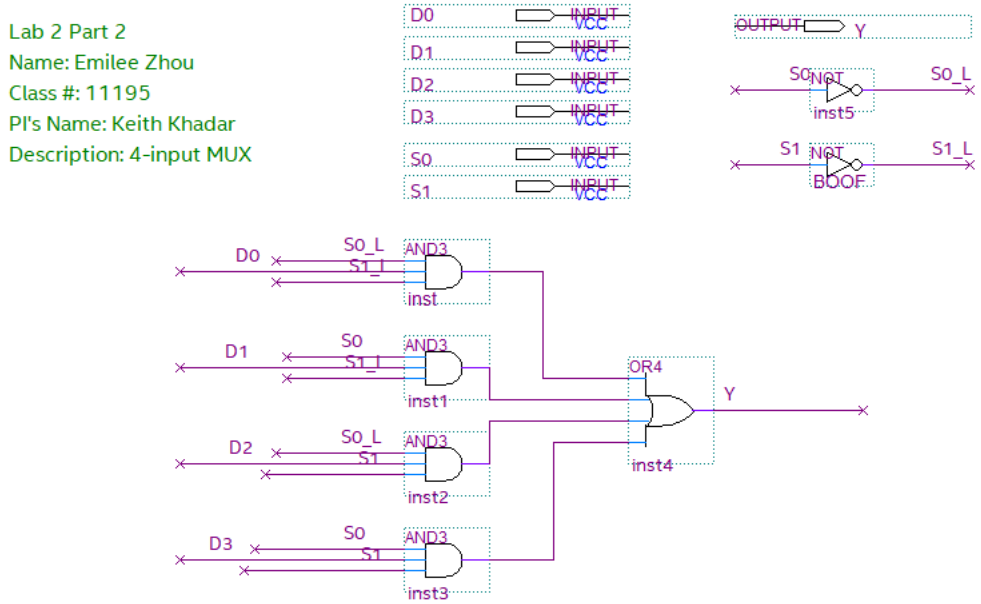


Figure 7: 4-input MUX BDF for Part 2

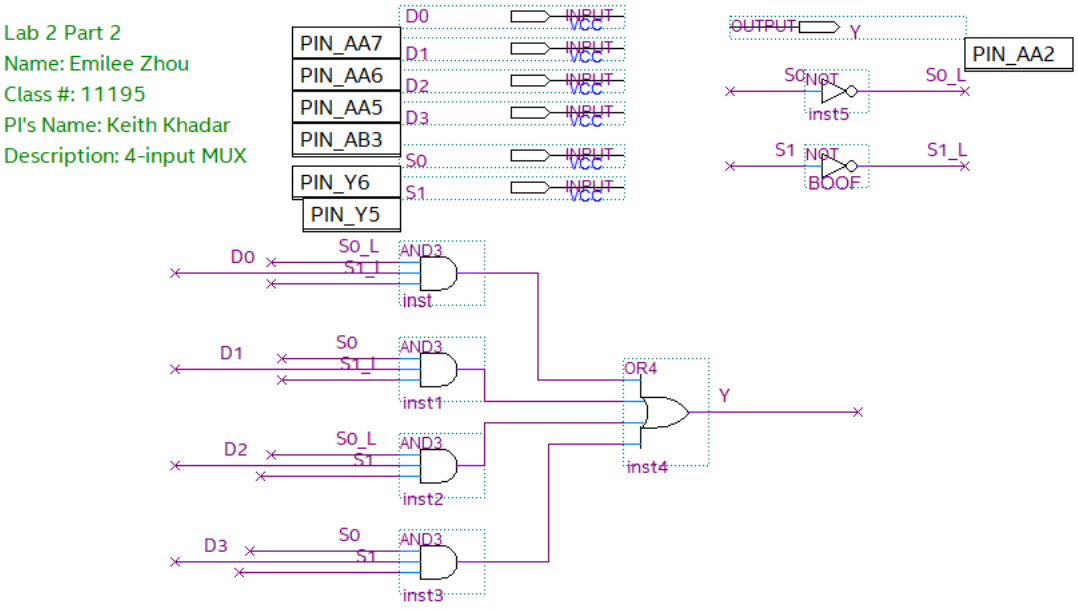


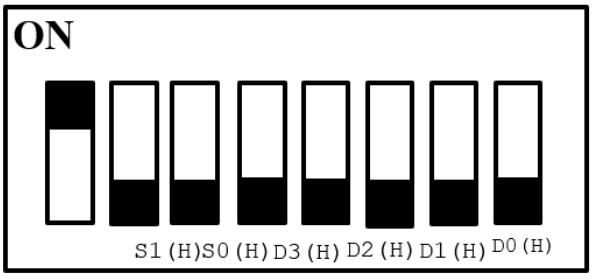
Figure 8: BDF with programmed pins for Part 2

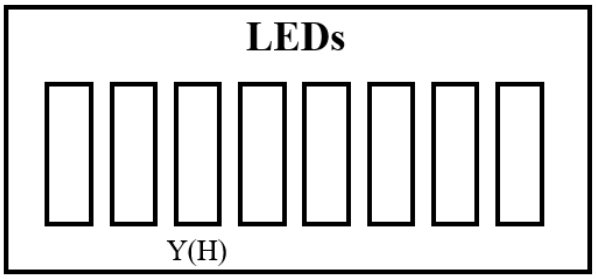
Named: * Edit:

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Diff
D0	Input	PIN_AA7	3	B3_N0	PIN_AA7	2.5 V		12mA (default)		
D1	Input	PIN_AA6	3	B3_N0	PIN_AA6	2.5 V		12mA (default)		
D2	Input	PIN_AA5	3	B3_N0	PIN_AA5	2.5 V		12mA (default)		
D3	Input	PIN_AB3	3	B3_N0	PIN_AB3	2.5 V		12mA (default)		
S0	Input	PIN_Y6	3	B3_N0	PIN_Y6	2.5 V		12mA (default)		
S1	Input	PIN_Y5	3	B3_N0	PIN_Y5	2.5 V		12mA (default)		
Y	Output	PIN_AA2	3	B3_N0	PIN_AA2	2.5 V		12mA (default)	2 (default)	
<<new node>>										

Figure 9: Pin Assignments for Part 2

Table 5: 4-input MUX LED and Switch Legends for Part 2





PART 3: DECODER DESIGN

Table 6: Truth Table for Part 3

T	X3	X2	X1	X0	A	B	C	D	E	F	G
0	0	0	0	0	1	1	1	1	1	1	0
0	0	0	0	1	0	1	1	0	0	0	0
0	0	0	1	0	1	1	0	1	1	0	1
0	0	0	1	1	1	1	1	1	0	0	1
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	0	1	1	0	1	1	0	1	1
0	0	1	1	0	1	0	1	1	1	1	1
0	0	1	1	1	1	1	1	1	0	0	0
0	1	0	0	0	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1
0	1	0	1	0	1	1	1	0	1	1	1
0	1	0	1	1	0	0	1	1	1	1	1
0	1	1	0	0	1	0	0	1	1	1	0
0	1	1	0	1	0	1	1	1	1	0	1
0	1	1	1	0	1	0	0	1	1	1	1
0	1	1	1	1	1	0	0	0	1	1	1
1	*	*	*	*	1	1	1	1	1	1	1

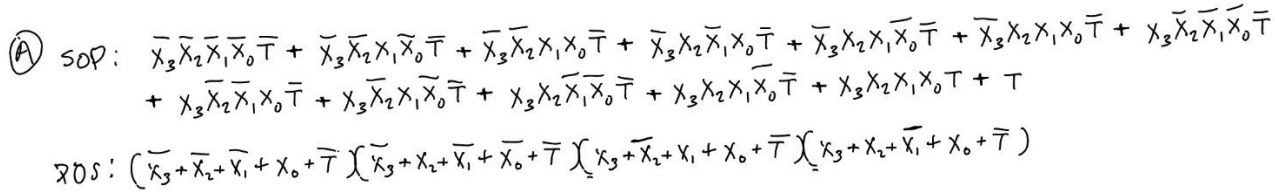


Figure 10: SOP and POS equations for Output A for Part 3

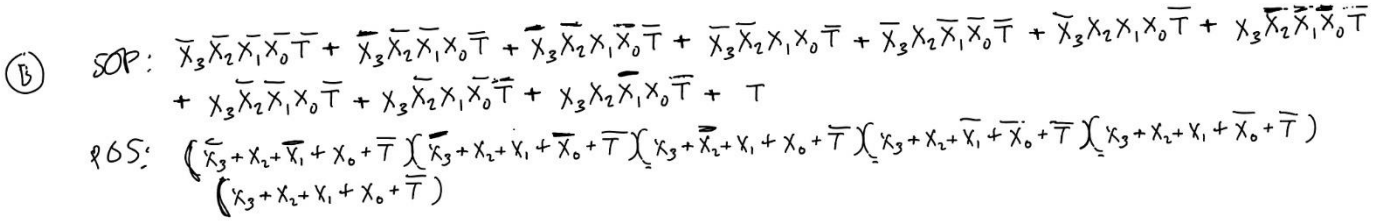


Figure 11: SOP and POS equations for Output B for Part 3

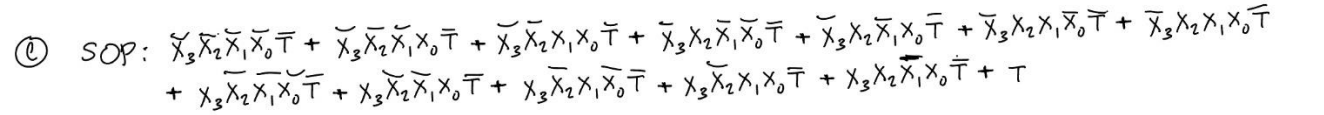


Figure 12: SOP equations for Output A for Part 3

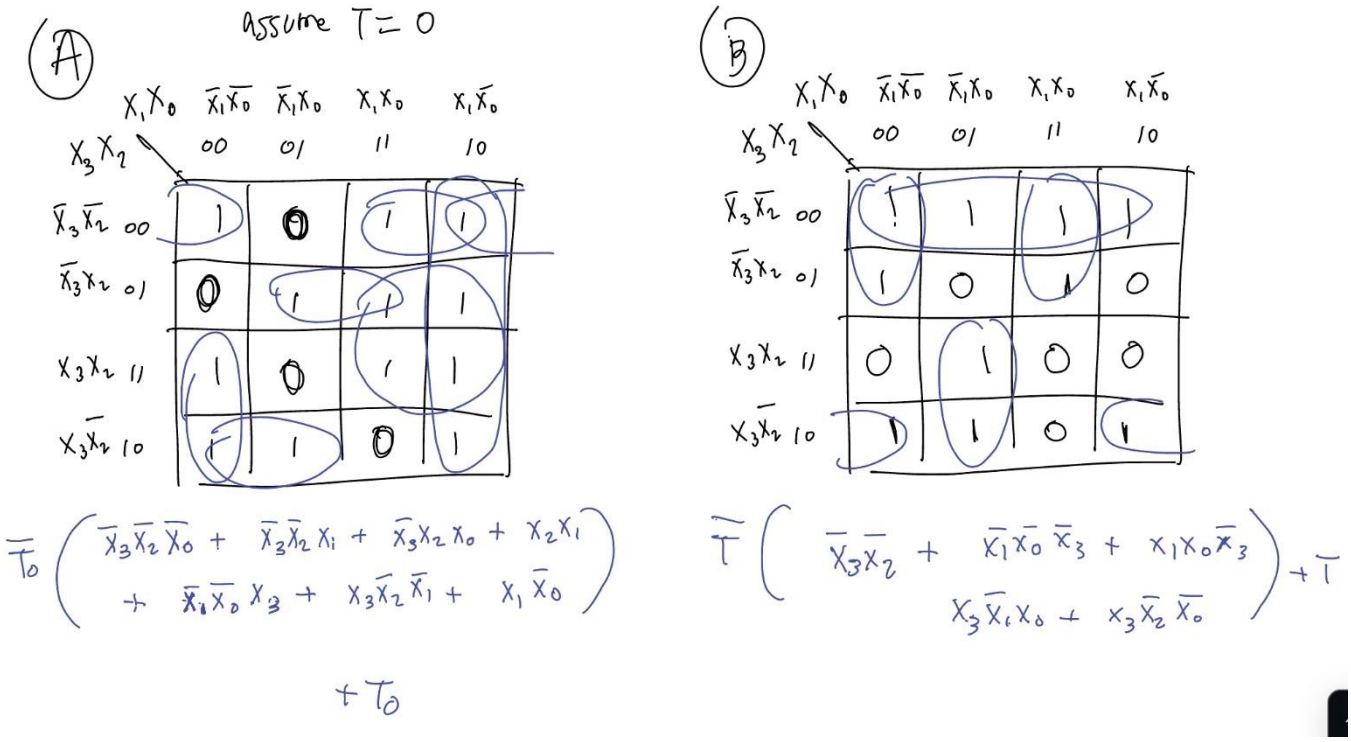


Figure 13: K-Maps for Part 3

Table 7: Voltage Table for Part 3

T (L)	X3 (H)	X2 (H)	X1 (H)	X0 (H)	A (L)	B (L)	C (L)
H	L	L	L	L	L	L	L

H	L	L	L	H	H	L	L
H	L	L	H	L	L	L	H
H	L	L	H	H	L	L	L
H	L	H	L	L	H	L	L
H	L	H	L	H	L	H	L
H	L	H	H	L	L	H	L
H	L	H	H	H	L	L	L
H	H	L	L	L	L	L	L
H	H	L	L	H	L	L	L
H	H	L	H	L	L	L	L
H	H	L	H	H	H	H	L
H	H	H	L	L	L	H	H
H	H	H	L	H	H	L	L
H	H	H	H	L	L	H	H
H	H	H	H	H	L	H	H
L	*	*	*	*	L	L	L

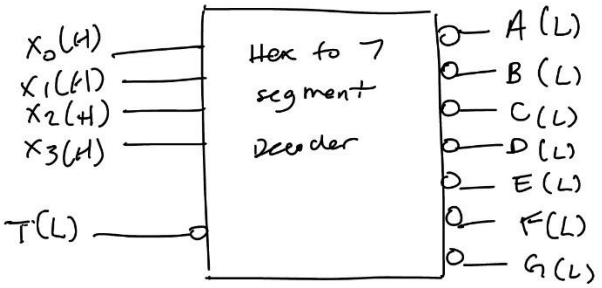


Figure 14: Block Diagram of Hex to 7-seg Decoder for Part 3

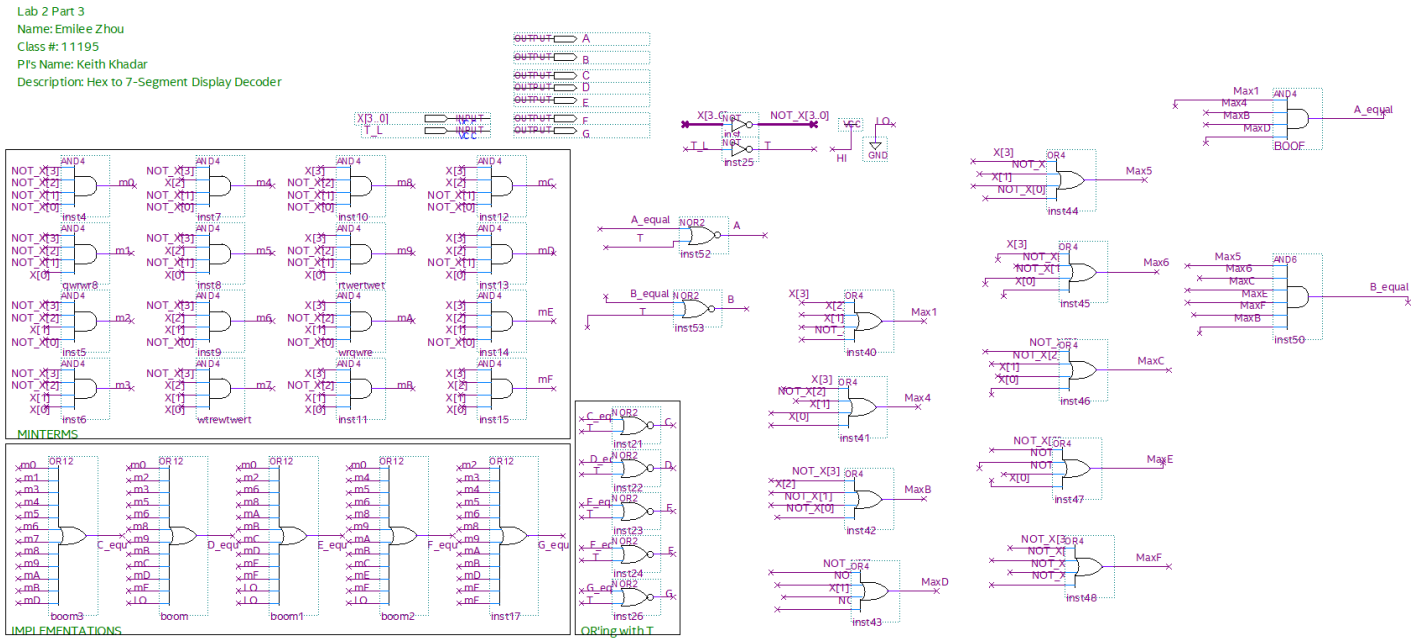


Figure 15: BDF of Hex to 7-Segment Display Decoder for Part 3

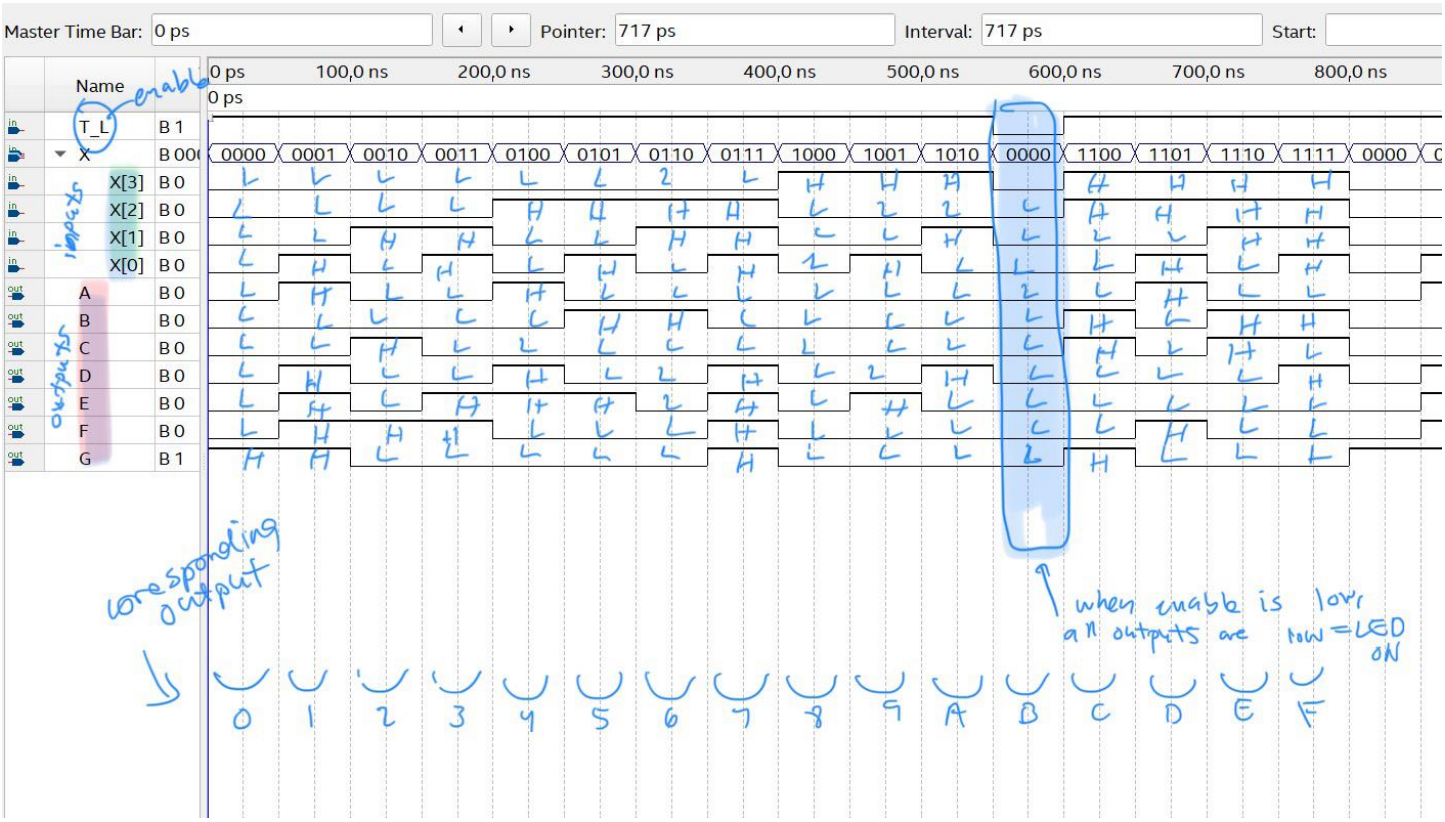


Figure 16: Functional Simulation for Part 3

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservati
A	Output	PIN_C14	7	B7_N0	PIN_E8	2.5 V (default)		12mA (default)	2 (default)		
B	Output	PIN_E15	7	B7_N0	PIN_D5	2.5 V (default)		12mA (default)	2 (default)		
C	Output	PIN_C15	7	B7_N0	PIN_B5	2.5 V (default)		12mA (default)	2 (default)		
D	Output	PIN_C16	7	B7_N0	PIN_B2	2.5 V (default)		12mA (default)	2 (default)		
E	Output	PIN_E16	7	B7_N0	PIN_D6	2.5 V (default)		12mA (default)	2 (default)		
F	Output	PIN_D17	7	B7_N0	PIN_C5	2.5 V (default)		12mA (default)	2 (default)		
G	Output	PIN_C17	7	B7_N0	PIN_C4	2.5 V (default)		12mA (default)	2 (default)		
S0	Input	PIN_Y6	3	B3_N0	PIN_A3	2.5 V (default)		12mA (default)			
S1	Input	PIN_Y5	3	B3_N0	PIN_A2	2.5 V (default)		12mA (default)			
T_L	Input	PIN_AB2	3	B3_N0	PIN_E9	2.5 V (default)		12mA (default)			
X[3]	Input	PIN_AB3	3	B3_N0	PIN_D7	2.5 V (default)		12mA (default)			
X[2]	Input	PIN_AA5	3	B3_N0	PIN_B4	2.5 V (default)		12mA (default)			
X[1]	Input	PIN_AA6	3	B3_N0	PIN_B3	2.5 V (default)		12mA (default)			
X[0]	Input	PIN_AA7	3	B3_N0	PIN_C6	2.5 V (default)		12mA (default)			
Y	Output	PIN_AA2	3	B3_N0	PIN_F7	2.5 V (default)		12mA (default)	2 (default)		
<<new node>>											

Figure 17: Pin Assignments for Part 3

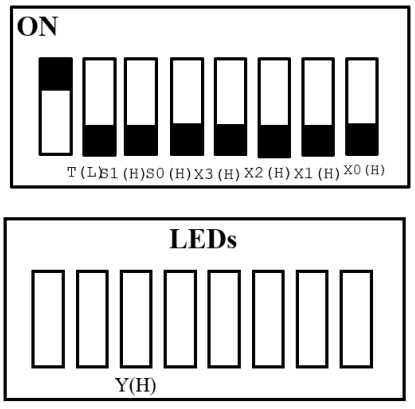


Figure 18: Switch and LED Legend for Part 3

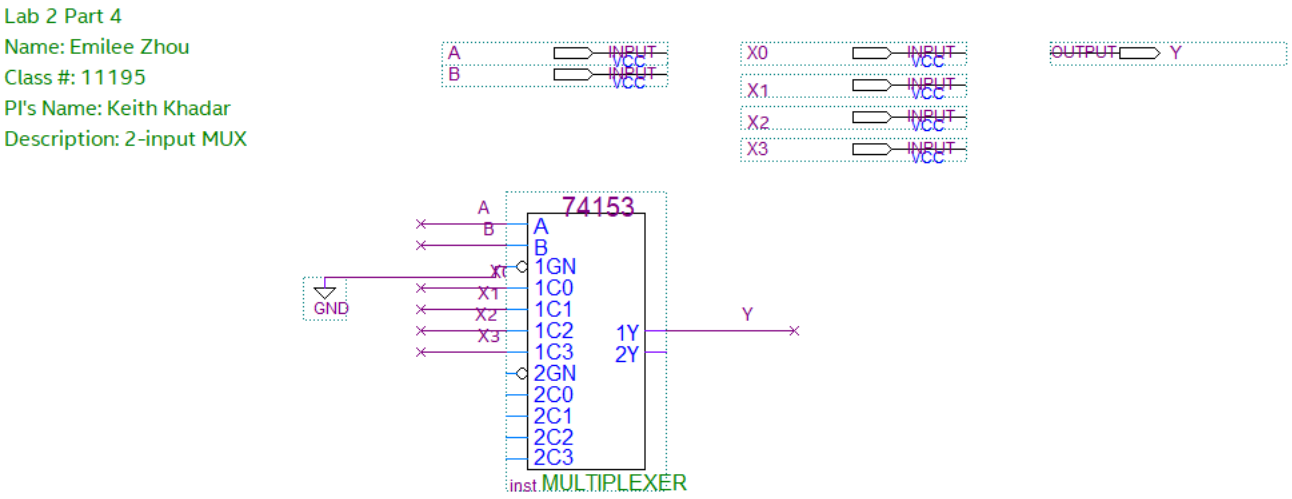


Figure 19: BDF of Double 4-input MUX

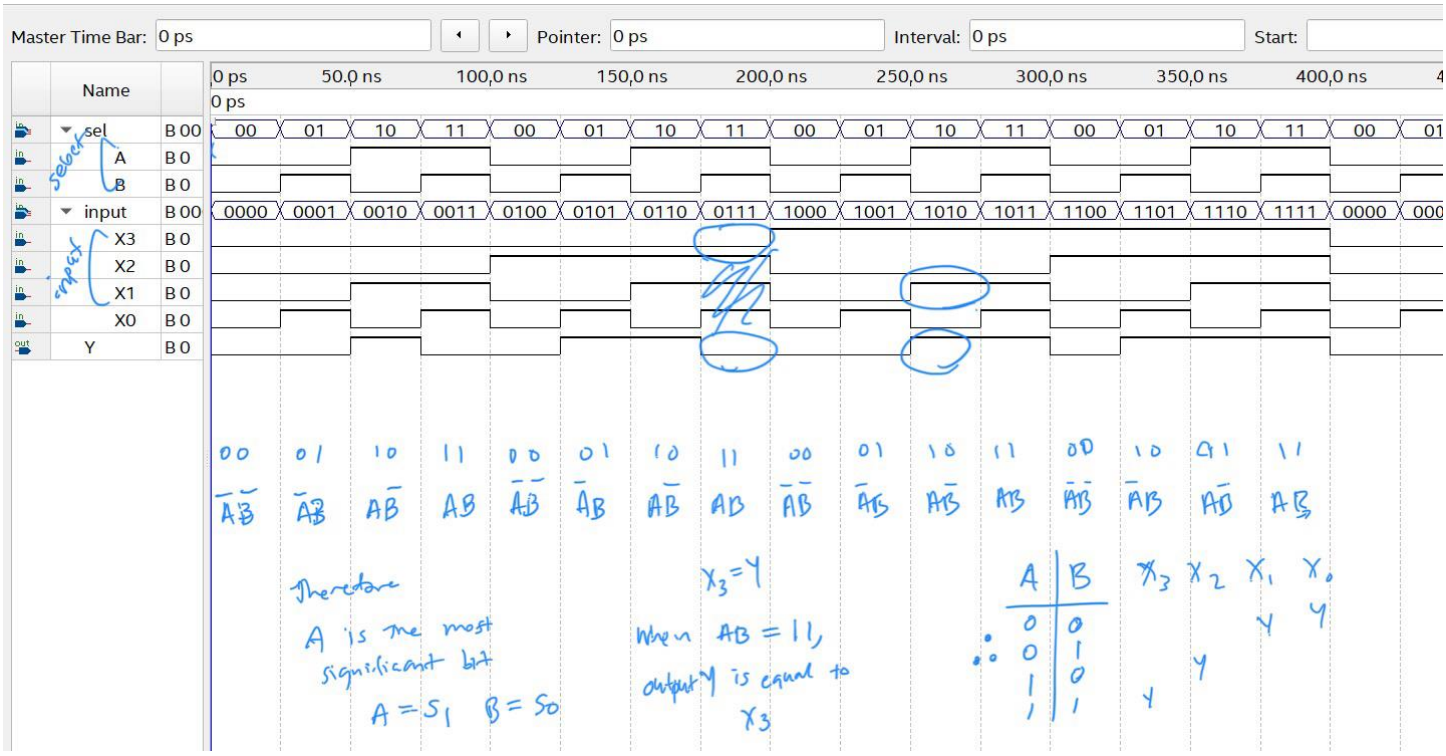


Figure 20: Functional Simulation for Part 4

Table 8: Truth Table for Part 4

V	W	X	Z	/V	/X	/X*Z	(W+/X*Z)	/V*(W+/X*Z)	/V*/W*/X	F
0	0	0	0	1	1	0	0	0	1	1
0	0	0	1	1	1	1	1	1	1	1
0	0	1	0	1	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0
0	1	0	0	1	1	0	1	1	0	1
0	1	0	1	1	1	1	1	1	0	1
0	1	1	0	1	0	0	1	1	0	1
0	1	1	1	1	0	0	1	1	0	1
1	0	0	0	0	1	0	0	0	0	0
1	0	0	1	0	1	1	1	0	0	0
1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0
1	1	0	0	0	1	0	1	0	0	0
1	1	0	1	0	1	1	1	0	0	0
1	1	1	0	0	0	0	1	0	0	0
1	1	1	1	0	0	0	1	0	0	0

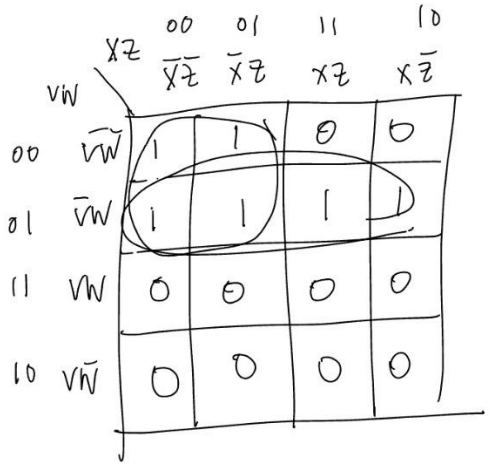


Figure 21: MSOP and K-Map for Part 4

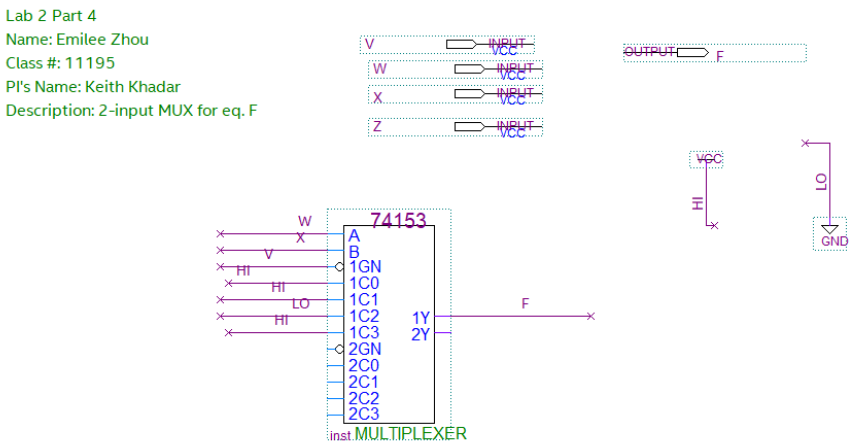


Figure 22: BDF of F for Part 4

Table 9: Voltage Table for Part 4

V(L)	W(H)	X(H)	Z(H)	F(H)
L	*	*	*	L
H	L	L	*	H
H	L	H	*	L
H	H	L	*	H
H	H	H	*	H

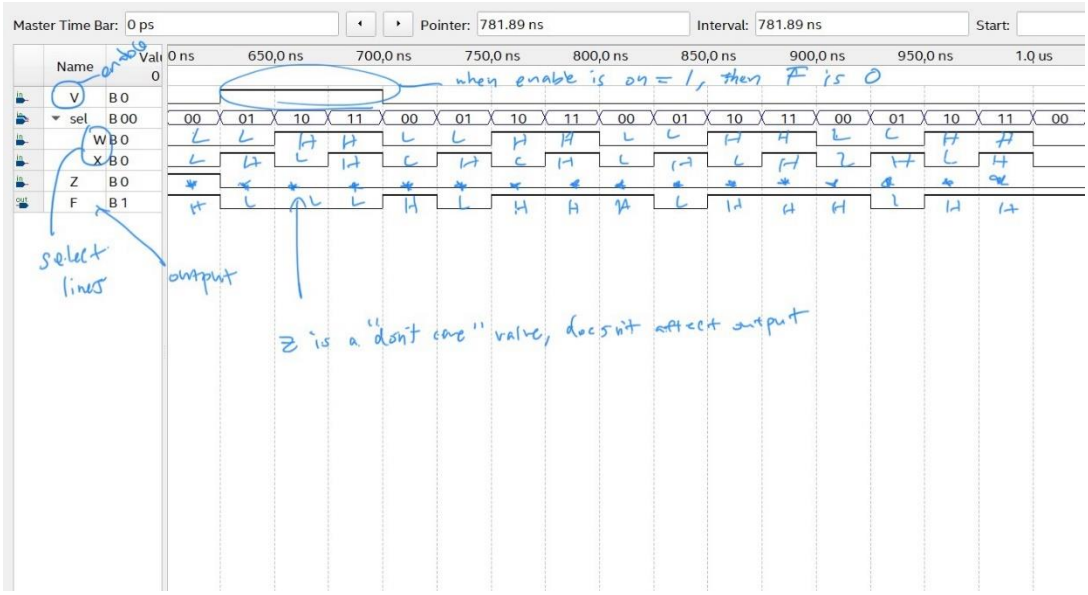


Figure 23: Functional Simulation for Part 4