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Lab 6 Quiz

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Time Limit: 60 minutes

Part 1:

Modify your Lab6 Part2 CPU to start at the address 0x4A10. Implement a program based on the pseudocode below. You should make the necessary hardware modifications, write a short assembly program, create a MIF file, and simulate. You MUST use the ROM creation tool and not the VHDL ROM alternative for this quiz. You will demonstrate the simulation.

A = 3

B = 2

A = A+B

Repeat the previous instruction indefinitely.

Part 2

On paper, you will design a new instruction for your CPU. You do not need to implement it. Draw the necessary modifications to your ASM on your paper. You do not need to show the entire ASM, but you should show the relevant ASM path for your instruction.

Use the Op Code 111 for this instruction “JOVR addr”

This instruction makes the PC jump to the specified address if the sum of registers A and B is more than 16. Otherwise, it skips to the next instruction.

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Hint: You can use any output of the RALU as an input to the controller.

On the following page, some helpful tables and diagrams are provided.

As usual, submit your .qar files, an image of your bdf, and an image of your simulation to Quiz 6 – Generic on Canvas. Anything else should be submitted to Quiz 6 – Phone.

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Table 1: Input source MUXs for Registers A and B.

MSA/ MSB1	MSA/ MSB0	Bus Selected as Input to REGA/REGB
0	0	INPUT Bus
0	1	REGA Bus
1	0	REGB Bus
1	1	OUTPUT Bus

Table 3: ALU function selection MUX (for MUX C).

MSC2:0	Action
000	REGA Bus to OUTPUT Bus
001	REGB Bus to OUTPUT Bus
010	complement of REGA Bus to OUTPUT Bus
011	bit wise AND REGA/REGB Bus to OUTPUT Bus
100	bit wise OR REGA/REGB Bus to OUTPUT Bus
101	sum of REGA Bus & REGB Bus to OUTPUT Bus
110	shift REGA Bus left one bit to OUTPUT Bus
111	shift REGA Bus right one bit to OUTPUT Bus **without** sign extension

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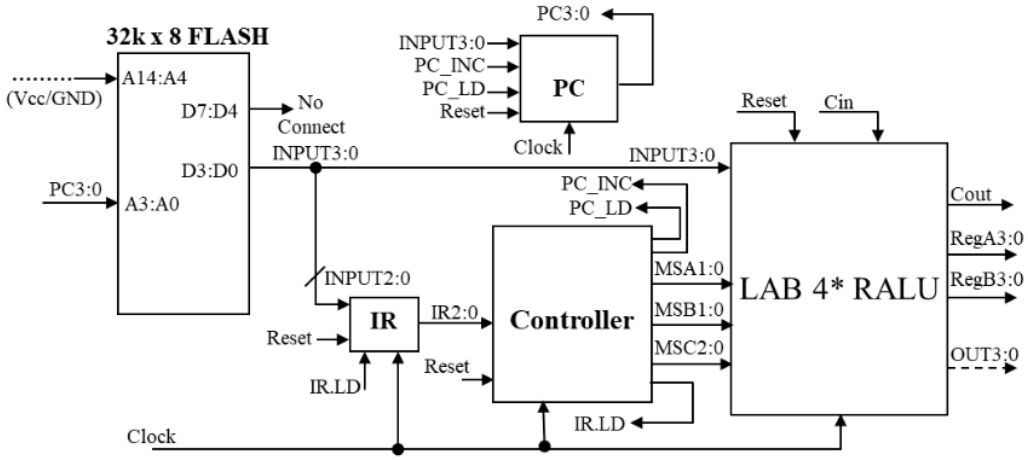

Figure 3. Block diagram of system hardware.