EEL 3701C: Digital Logic & Computer Systems
Revision **0**
Lab **2** Report: **MSI Circuits**

Poche, Natalie
Class #: 11198
PI Name: Jaiden Magnan
February 13, 2025

REQUIREMENTS NOT MET

Part 1: Did not use GPIO to power circuit design.

Part 2: Did not create a physical copy of the LED.

Part 3: Did not create a Quartus design, Did not create a combined Quartus file. Did not create equations.

Part 4: Create a 74'153 MUX in Quartus. Design circuit with MUX 74'153, simulate Quartus design

VIDEO FILE LINK

https://youtu.be/JOJ_mgJ6wPU

PROBLEMS ENCOUNTERED

For some reason when creating lab 1, the light would stay on and just change from bright to dim with the switches. Additionally, When I turned the switch for S_0 on high, it would render the other two switches useless and change the light to brighter and when it was turned low, both the switch for D_1 and D_0 could change the brightness when it should have only been D_0. I also had problems trying to upload my designs onto the D10-Lite and use them, I could upload them, but I'm not sure about how to wire things to test it. Did not have time this week to go to office hours.

FUTURE WORK/APPLICATIONS

Using a MUX can be great for making more complicated designs and giving users greater options or control over future designs.

PRE-LAB QUESTIONS OR EXERCISES

PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)

Each section of the pre-lab requirements should be completed separately, and in order. Include each of the following items in order. Note that some of these items will not apply to every lab. Anything scanned or copied ***must be clear and legible***.

- Logic equations. (Note that logic equations do not contain activation levels.)
- **All** tables and figures should have captions with Figure/Table numbers and a description of for which part of the lab it references, e.g., ***Table 3****: Truth Table for Part B*.
- Truth tables and voltage tables (and/or next-state truth tables).
- When applicable, include Karnaugh Maps (i.e., K-Maps).
- Include hand-drawn circuits (when required). Label all input and output activation-levels and intermediate equations in the circuits.
- Include screenshots of the BDF designs of circuits.
  - Label all input and output activation-levels, i.e., use _L suffix for active-low signals and no suffix for active-high signals. **Add chip and pin numbers to any schematic that will be constructed.**
  - Images should be large enough so that inputs, outputs, labels, and parts are clearly visible and distinguishable to any reader.
  - Each BDF should have the following info on the top left corner (similar to the top right of this page):

    Last Name, First Name
    Lab #, Part #
    Class #
    PI Name:
    Description: (short description of what is to be accomplished in the design; perhaps an equation)

  - In Windows, I use the ***Snipping Tool***, which is now built into Windows. Just type "snip" in the Windows search box and then select ***Snipping Tool***.
- When necessary, include ASM Charts. These can be hand-drawn, but clear and legible. We recommend that you use resources like https://www.draw.io/ to create computer-generated ASMs.
- Truth tables or next-state truth tables should have the following characteristics.
  - Can be either typed or hand-written and scanned (must be clear and legible)
  - Must be in **counting order** (i.e., inputs of 000, 001, 010, 011, …, 111)
  - Clearly distinguish inputs from outputs (see the example below that uses a thick line)
  - If you are designing a state machine or a controller, clearly indicate and separate signal values both before the clock and after the clock (i.e., Q1 and $Q1^+$, respectively)
  - Tip: divide rows into consecutive groups of 4 (or 2 or 8) to make it easier for both you and your PI to read.
  - **Example**

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Table: Caption for above table. It should reference the part of the lab, e.g., "Table 3: Truth Table for Part B."

- Voltage tables should have the following characteristics.
  - Must be in counting order (i.e., inputs of LLL, LLH, LHL, … , HHH)
  - Use similar formatting to truth tables (described above)

- **Example**

A(H)	B(H)	C(L)	Y(L)
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

- Include **meaningfully annotated** functional simulations.
  - Using the grouping tool, ***group as many signals together as possible*** (when it makes sense to group them)! If you are simulating a basic logic equation, group all the inputs together. If you are simulating a circuit that includes MSI elements, group signals of the form X_{N-0}. The most-significant bit should appear first, ending with the least-significant bit. If you are simulating an ALU, group the buses together as just described.
  - Not every row of your voltage table must be annotated in the waveform simulation, but your choices of rows that you annotate must be ***encompassing***
  - If you are designing a state machine or a controller, your CLK signal should appear ***at the top*** of your inputs and outputs. The general order is CLK -> Reset -> state bits -> inputs -> outputs.
  - ***Tip***: Use Microsoft Paint to annotate your waveforms. An alternative is to print out the waveforms, annotate them by hand, then scan and upload
  - ***Hint***: Consider a truth table where the output is true in significantly less cases than it is false (or vice versa). If the output signal is active-high, it would be wise to annotate only the cases where the output voltage is HIGH.
- Include every line of VHDL programs, including both ***architecture*** and ***behavior*** sections.
- Include every line of any **MIF** files. If these are associated with assembly language programs, you can either put the assembly code as comments or separately include assembly language programs

Part 1: Introduction to Multiplexers

S_0	D_0	D_1	Y
0	0	*	0
0	1	*	1
1	*	0	0
1	*	1	1

Table 1: Lab 2 Part 1.1 - Truth Table for 2-input multiplexer(MUX)

$Y = (/S_0 * D_0) + (S_0 * D_1)$

Table 2: Lab 2 Part 1.2 - Logic Equation for 2-input multiplexer

S_0(H)	D_0(L)	D_1(H)	Y(H)
L	L	*	L
L	H	*	H
H	*	L	L
H	*	H	H

Table 3: Lab 2 Part 1.3 - Voltage Table for 2-input multiplexer

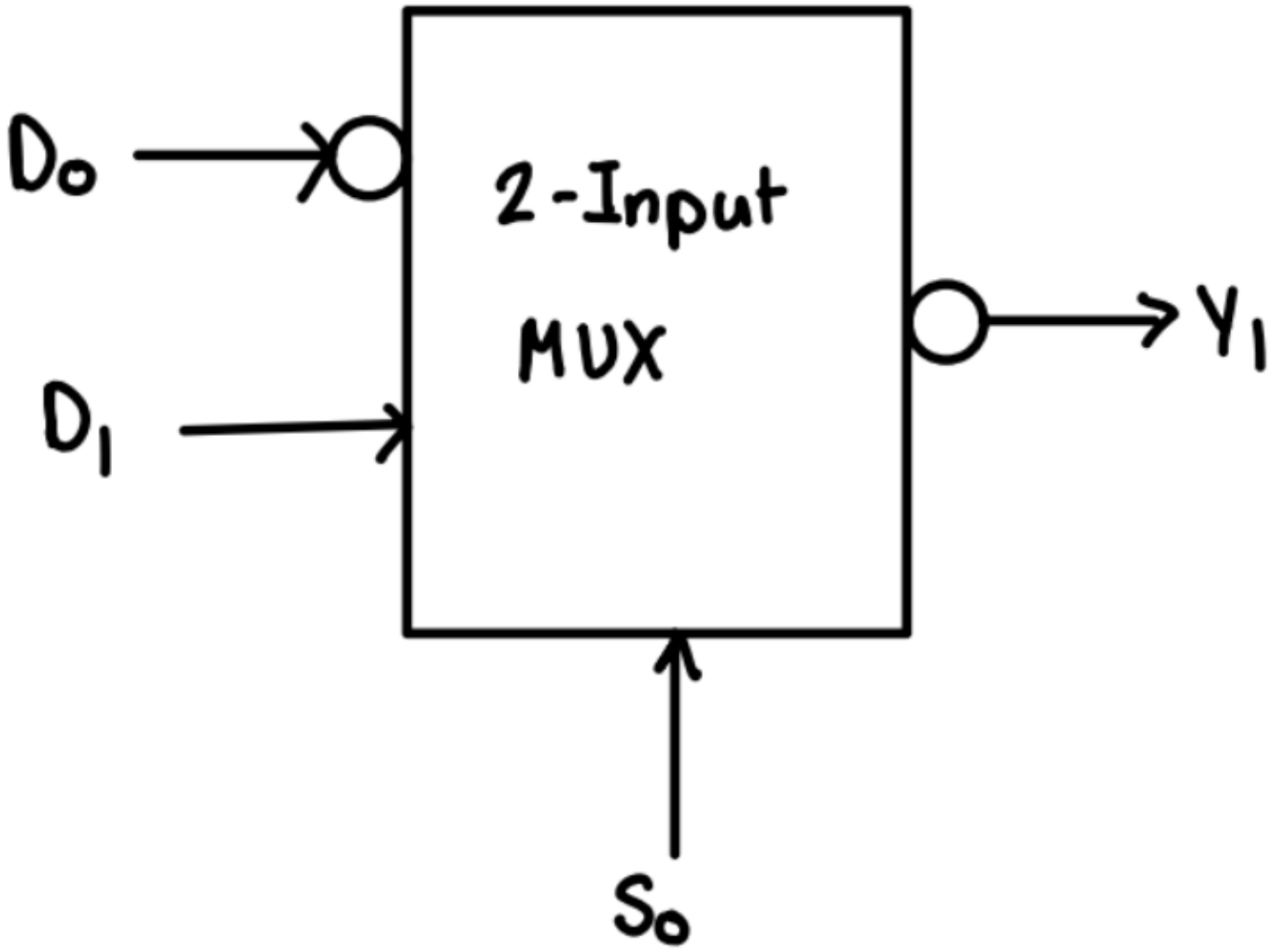


Table 4: Lab 2 Part 1.4 - 2-Input MUX Functional Block Diagram

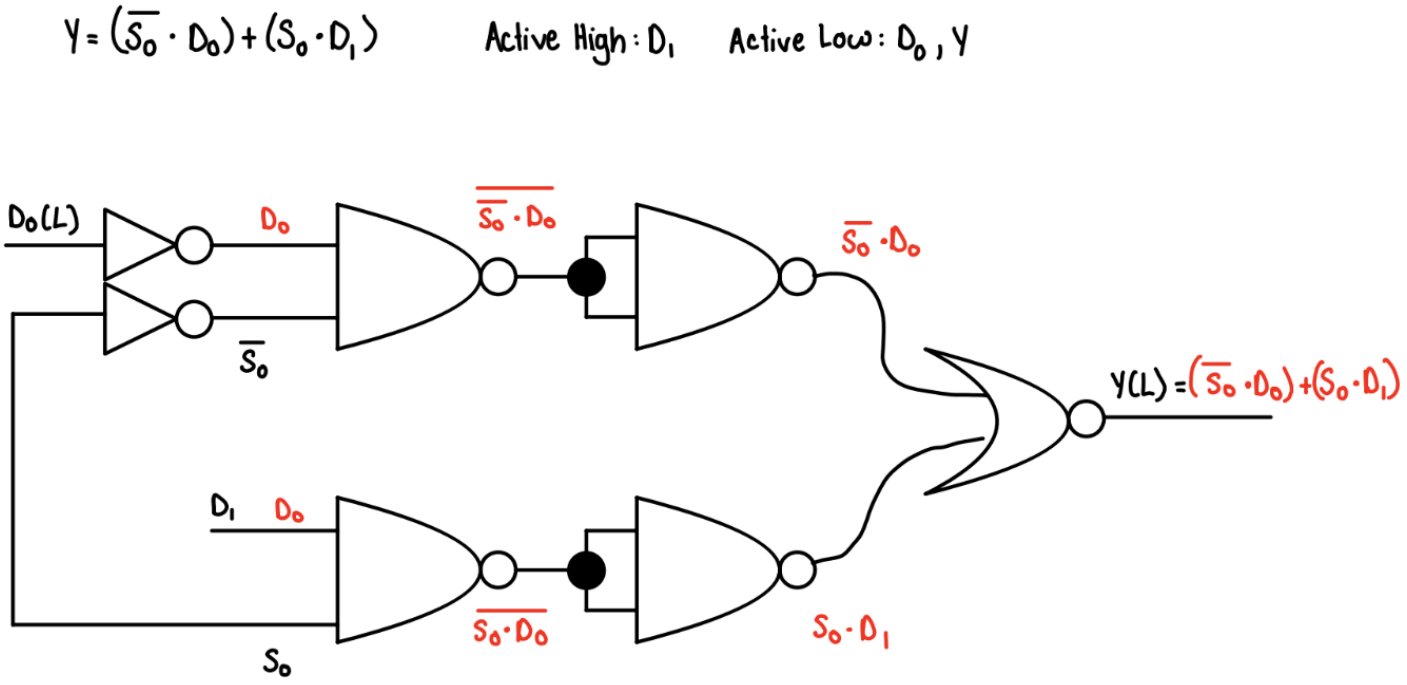


Table 5: Lab 2 Part 1.5 - Create 2-input MUX Circuit Design

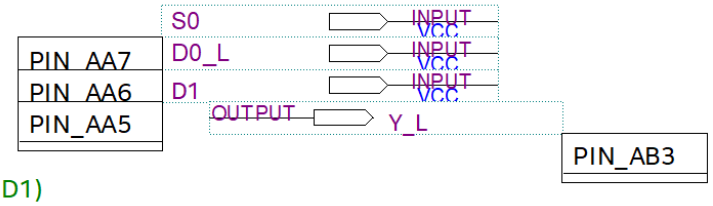
Lab 2, Part A

Name: Natalie Poche

Class #: 11198

PI Name: Jaiden Magnan

Description: 2-Input Multiplexer (MUX), Y = (/S0 * D0) + (S0 * D1)



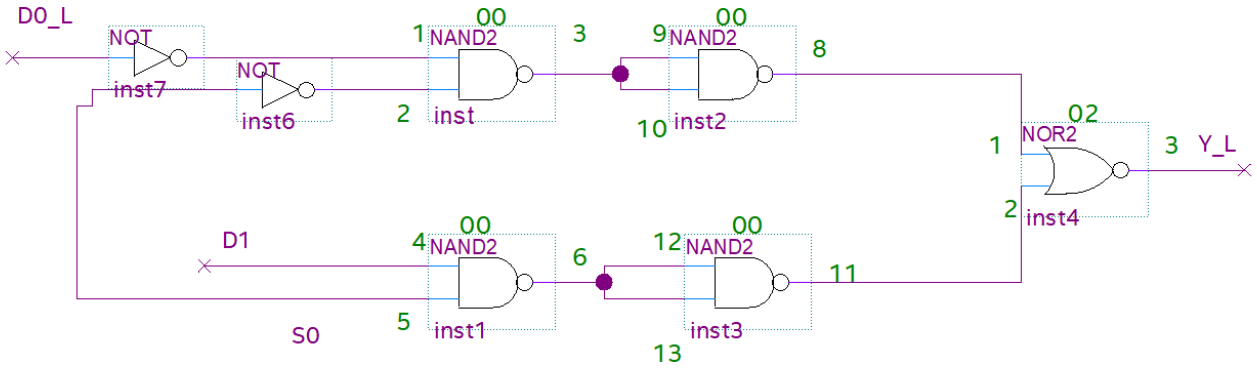


Table 6: Lab 2 Part 1.6 - BDF of 2-Input Multiplexer Circuit Diagram

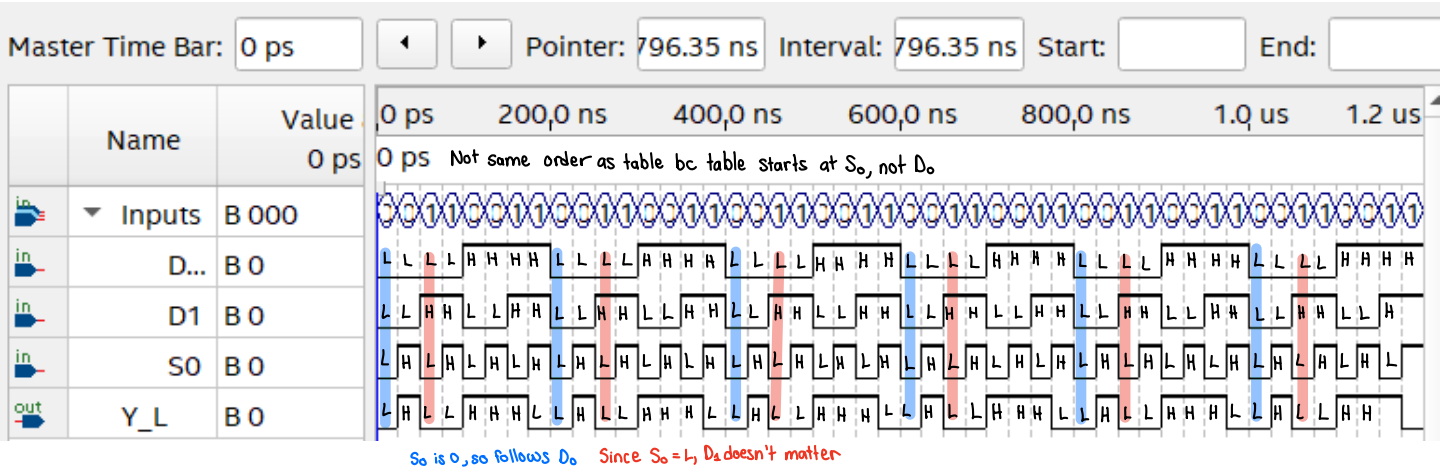


Table 7: Lab 2 Part 1.7 - Functional Simulation of 2-Input Multiplexer Circuit

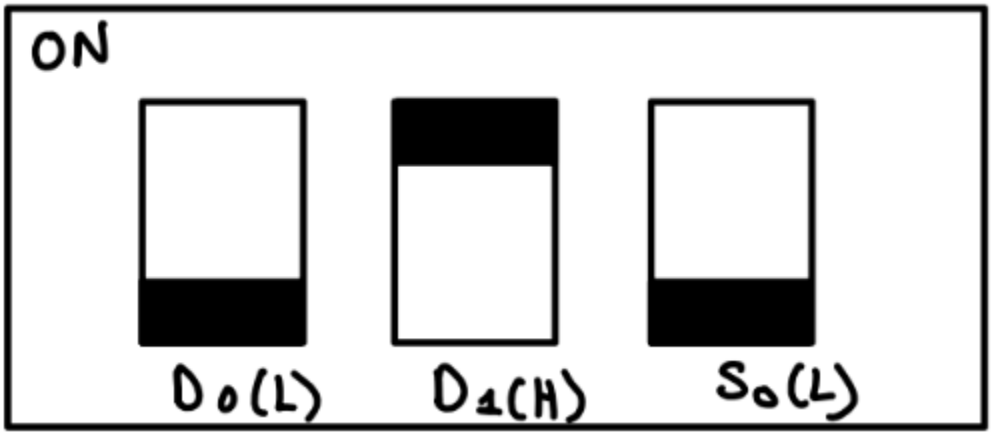


Table 8: Lab 2 Part 1.10 - 2-Input MUX Switch Legend

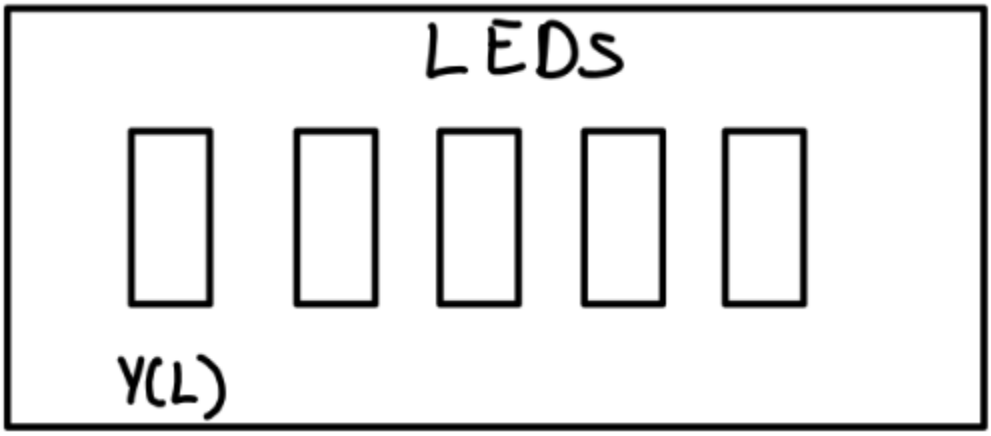


Table 9: Lab 2 Part 1.10 - 2-Input MUX LED Legend

Part 2: Four-Input Multiplexer Design

S_0	S_1	D_0	D_1	D_2	D_3	Y
0	0	0	*	*	*	0
0	0	1	*	*	*	1
0	1	*	0	*	*	0
0	1	*	1	*	*	1
1	0	*	*	0	*	0
1	0	*	*	1	*	1
1	1	*	*	*	0	0
1	1	*	*	*	1	1

Table 10: Lab 2 Part 2.1 – Truth Table for 4-input multiplexer (MUX)

$$Y = (/S_0 * /S_1 * D_0) + (/S_0 * S_1 * D_1) + (S_0 * /S_1 * D_2) + (S_0 * S_1 * D_3)$$

Table 11: Lab 2 Part 2.2 - Logic Equation from 4-input MUX Truth Table

S_0(H)	S_1(H)	D_0(L)	D_1(H)	D_2(L)	D_3(H)	Y(H)
L	L	L	*	*	*	L
L	L	H	*	*	*	H
L	H	*	L	*	*	L
L	H	*	H	*	*	H
H	L	*	*	L	*	L
H	L	*	*	H	*	H
H	H	*	*	*	L	L
H	H	*	*	*	H	H

Table 12: Lab 2 Part 2.3 - Voltage Table for 4-input multiplexer

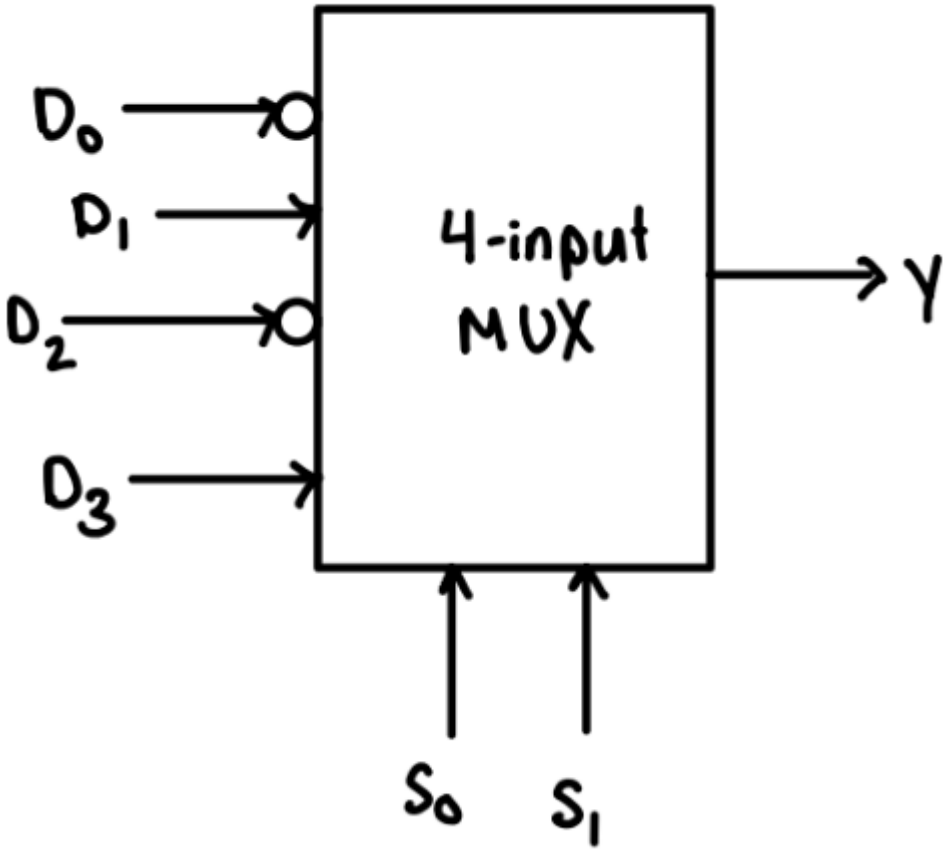


Table 13: Lab 2 Part 2.4 - 4-Input MUX Functional Block Diagram

Lab 2, Part B

Name: Natalie Poche

Class #: 11198

PI Name: Jaiden Magnan

Description: 4-input MUX, Y = (/S0 * /S1 * D0) + (/S0 * S1 * D1) + (S0 * S1 * D2) + (S0 * S1 * D3)

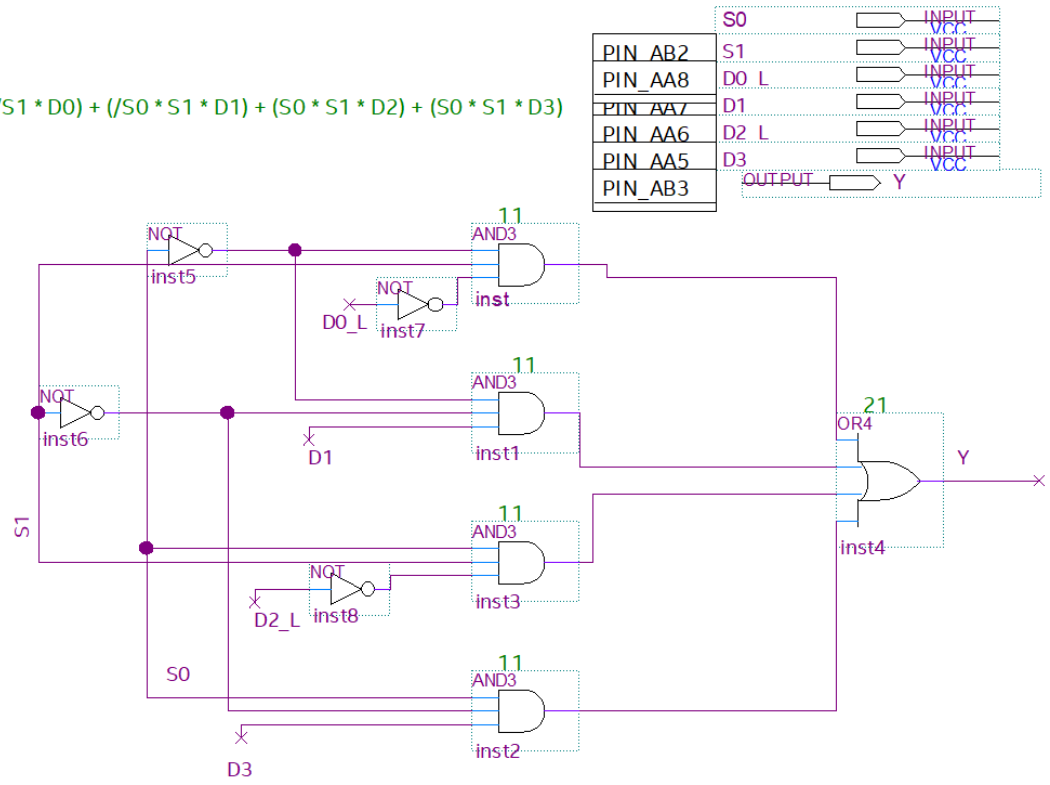


Table 14: Lab 2 Part 2.5 - BDF of 4-Input MUX Circuit Diagram

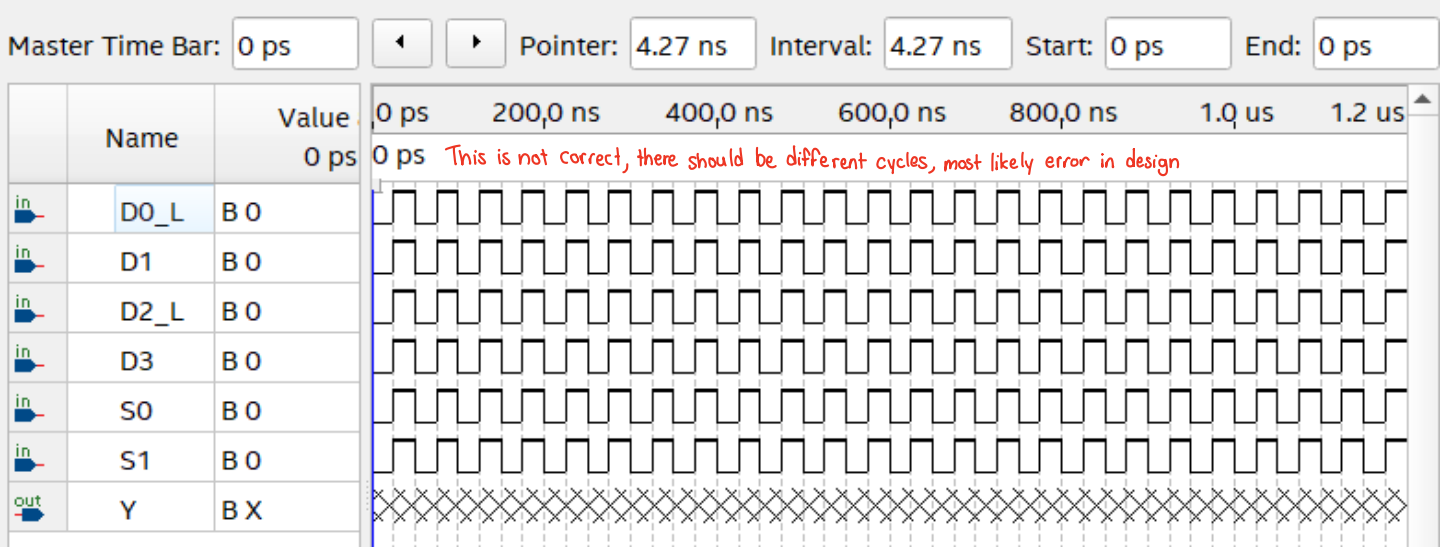


Table 15: Lab 2 Part 2.6 - 4-Input MUX Simulation

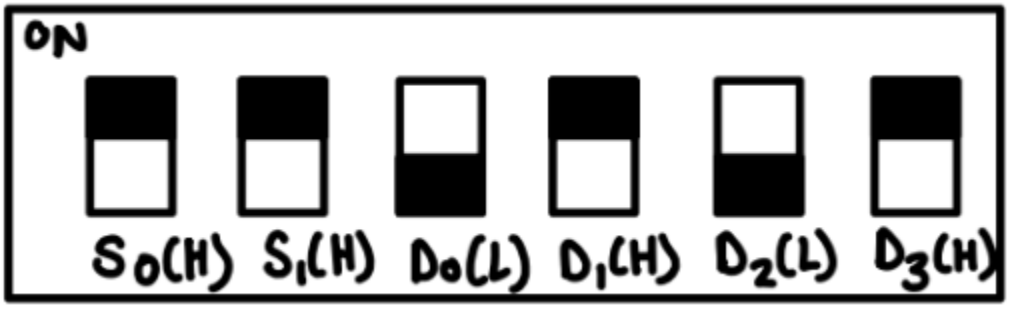


Table 16: Lab 2 Part 2.9 - 4-Input MUX Switch Legend

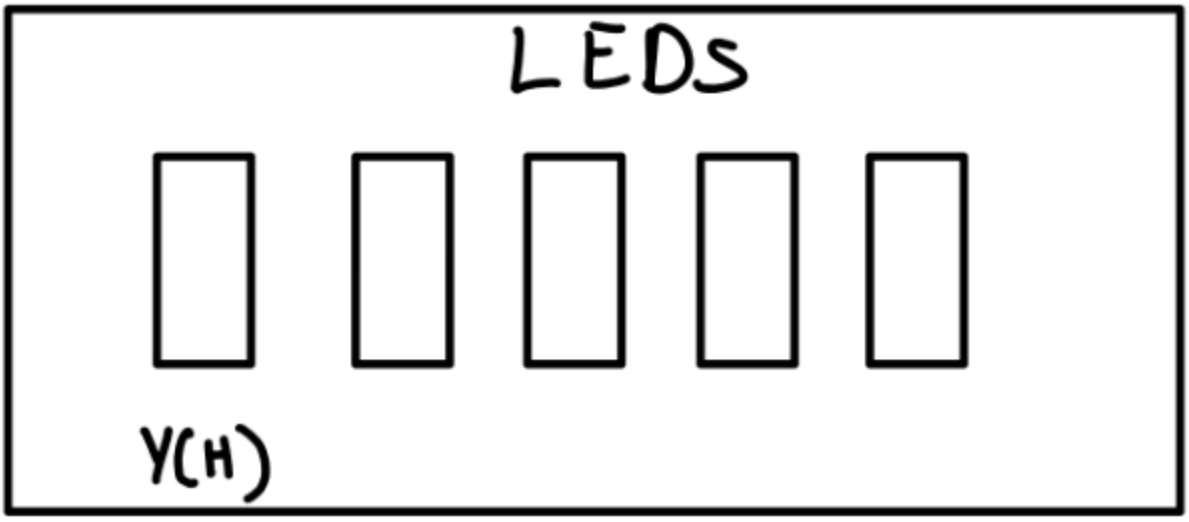


Table 17: Lab 2 Part 2.9 - 4-Input MUX LED Legend

Part 3: Decoder Design

X_0	X_1	X_2	X_3	T	A	B	C	D	E	F	G
0	0	0	0	0	1	1	1	1	1	1	0
0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	1	0	0	1	1	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	0	0	1	1
0	1	0	0	1	1	1	1	1	1	1	1
0	1	0	1	0	1	0	1	1	0	1	1
0	1	0	1	1	1	1	1	1	1	1	1
0	1	1	0	0	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	1	1
0	1	1	1	0	1	1	1	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1

1	0	0	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	0	1	1
1	0	0	1	1	1	1	1	1	1	1	1
1	0	1	0	0	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1
1	0	1	1	0	0	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1
1	1	0	0	0	1	0	0	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1
1	1	0	1	0	1	0	0	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1

Table 18: Lab 2 Part 3.1 - Truth Table for Hex to 7-Segment Decoder

Y =

X_0(H)	X_1(H)	X_2(H)	X_3(H)	T(L)	A(L)	B(L)	C(L)
L	L	L	L	L	H	H	H
L	L	L	L	H	H	H	H
L	L	L	H	L	L	H	H
L	L	L	H	H	H	H	H
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	H
L	L	H	H	L	H	H	H
L	L	H	H	H	H	H	H
L	H	L	L	L	L	H	H
L	H	L	L	H	H	H	H
L	H	L	H	L	H	L	H
L	H	L	H	H	H	H	H
L	H	H	L	L	H	L	H
L	H	H	L	H	H	H	H
L	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	H
H	L	L	L	H	H	H	H
H	L	L	H	L	H	H	H
H	L	L	H	H	H	H	H
H	L	H	L	L	H	H	H
H	L	H	L	H	H	H	H
H	L	H	H	L	L	L	H
H	L	H	H	H	H	H	H
H	H	L	L	L	H	L	L
H	H	L	L	H	H	H	H
H	H	L	H	L	H	L	L

H	H	L	H	H	H	H	H
H	H	H	L	L	L	H	H
H	H	H	L	H	H	H	H
H	H	H	H	L	H	L	L
H	H	H	H	H	H	H	H

Table 19: Lab 2 Part 3.3 - Voltage Table for ABC

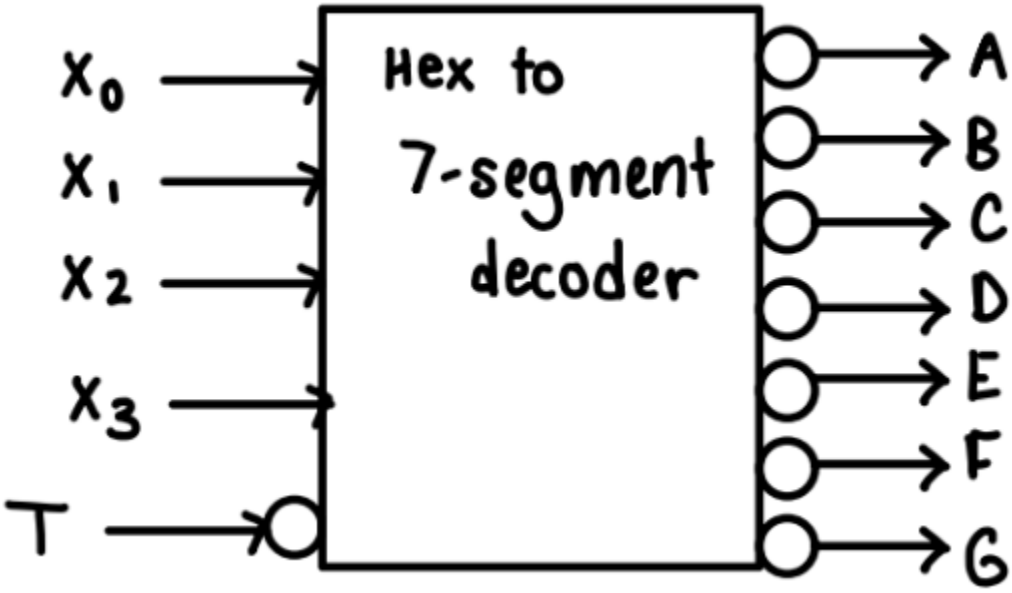


Table 20: Lab 2 Part 2.4 - Hex to 7-Segment Decoder Functional Block Diagram

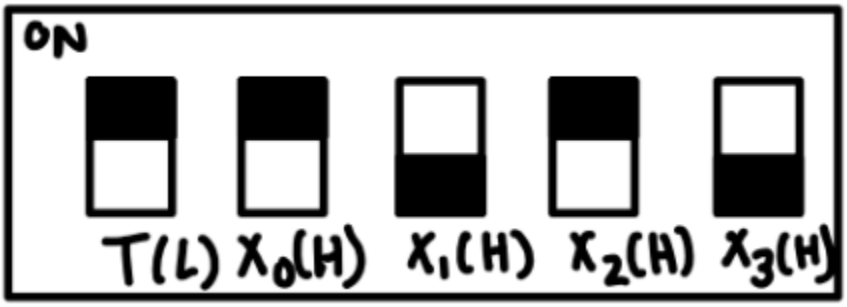


Table 21: Lab 2 Part 3.13 - Hex to 7-Segment Decoder Switch Legend

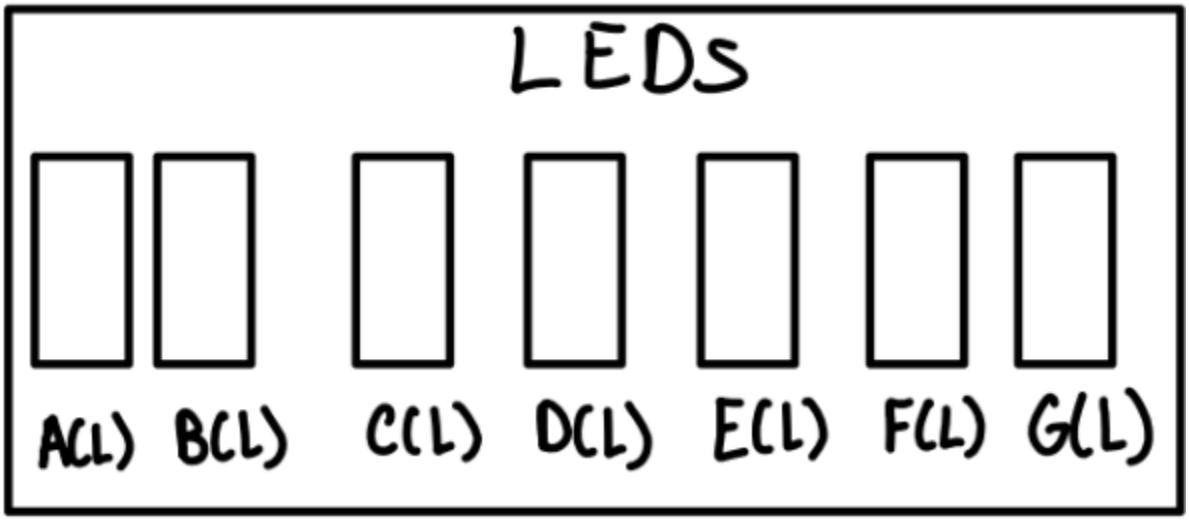


Table 22: Lab 2 Part 3.13 - Hex to 7-Segment Decoder LED Legend

Part 4: MUX Implementation of a Logic Equation

V	W	X	Z	/X * Z	W + /X * Z	/V * (W + /X* Z)	/V*/W*/X	F
0	0	0	0	0	0	0	1	1
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0
0	1	0	0	0	1	1	0	1
0	1	0	1	1	1	1	0	1
0	1	1	0	0	1	1	0	1
0	1	1	1	0	1	1	0	1
1	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	0	0
1	0	1	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	0	0	0
1	1	0	1	1	1	0	0	0
1	1	1	0	0	1	0	0	0
1	1	1	1	0	1	0	0	0

Table 23: Lab 2 Part 4.2 - Truth Table for F = /V(W + /X*Z)+/V*/W*/X*

V	W	X	Z	F
L	L	L	L	H
L	L	L	H	H
L	L	H	L	L
L	L	H	H	L
L	H	L	L	H
L	H	L	H	H
L	H	H	L	H
L	H	H	H	H
H	L	L	L	L

H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	L

Table 24: Lab 2 Part 4.5 - Voltage Table from F = /V(W+/X*Z)+/V*/W*/X*