Lab 3 Help Session

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EEL3701C: Digital Logic and Computer System

UF | Electrical & Computer Engineering
UNIVERSITY of FLORIDA

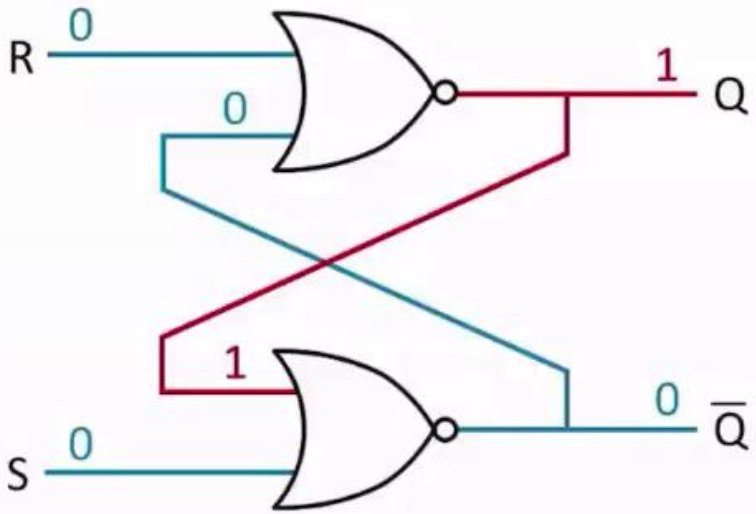
Overview

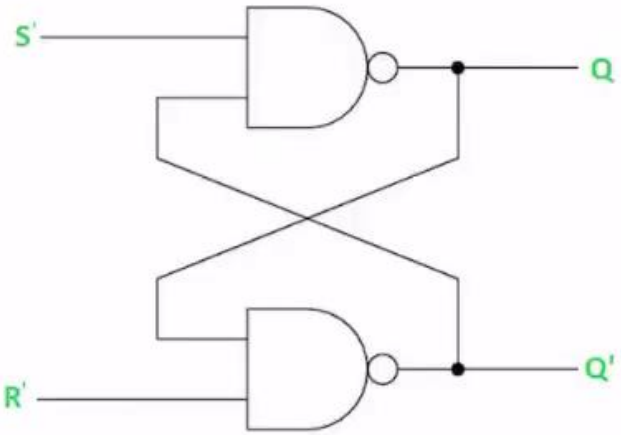
- Debouncing
  - SR Latch
  - Breadboarding
- Counter Design
  - NSTT
  - Types of FFs
  - Quartus Implementation of a Counter

SR Latch

SR Latch

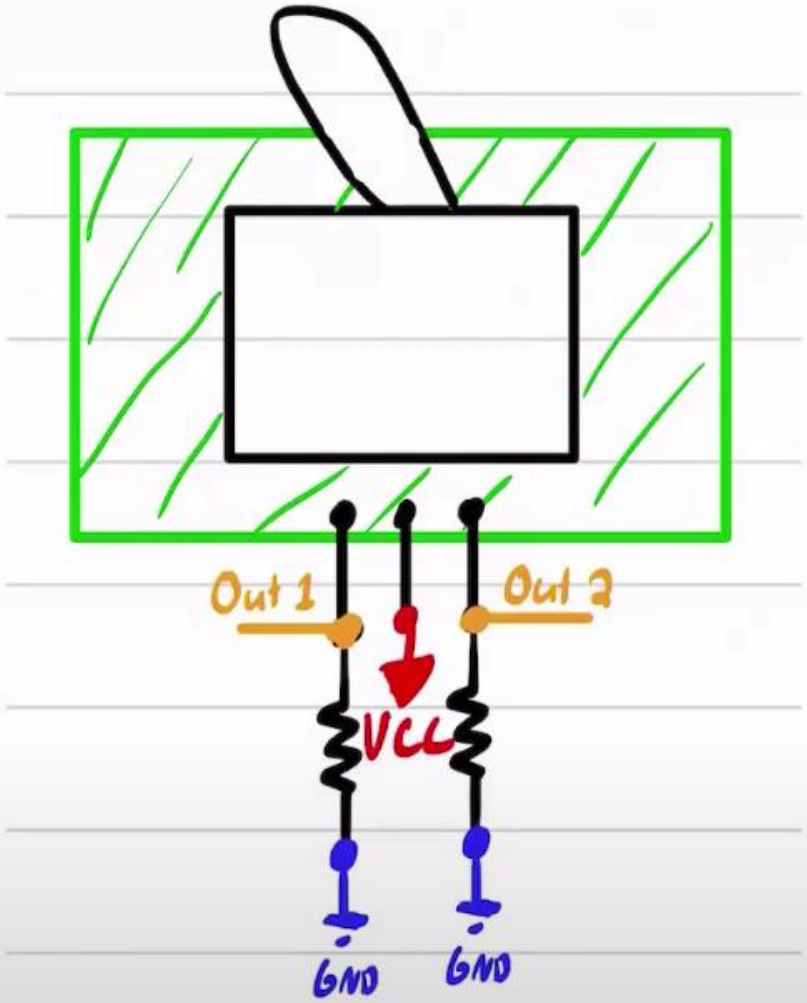
S	R	Q	$\overline{Q}$
0	0	1 0	0 1
0	1	0	1
1	0	1	0
1	1	0	0

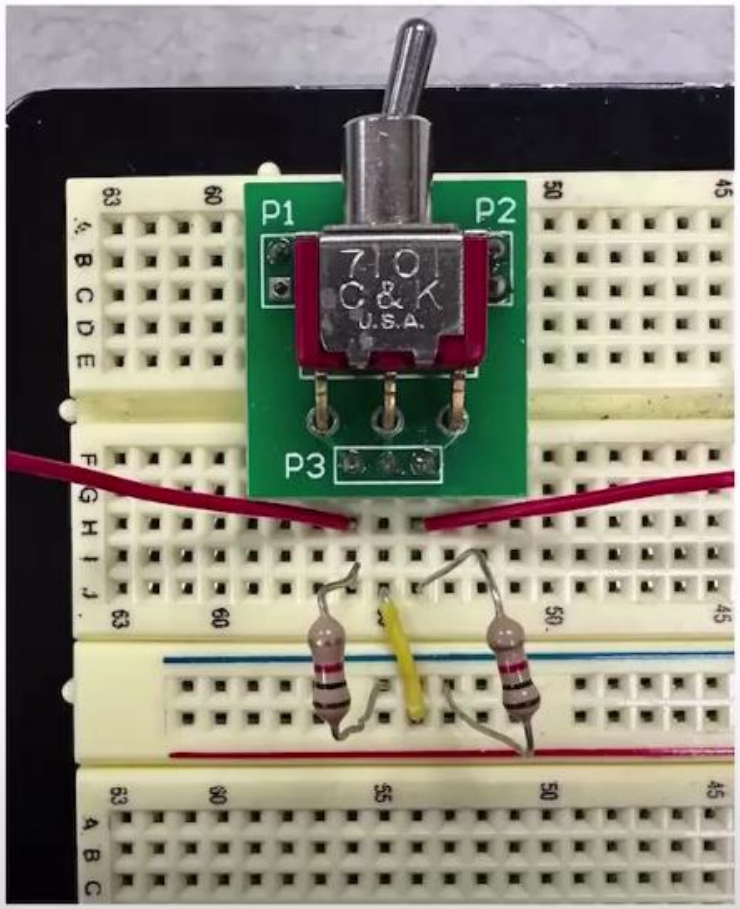




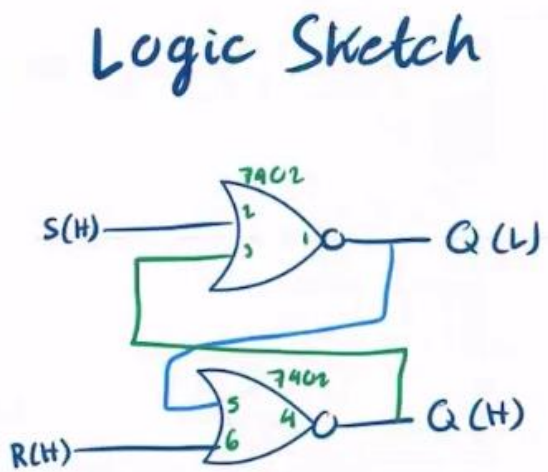
S	R	Qn+1
0	0	0 (Hold)
0	1	0 (Reset)
1	0	1 (Set)
1	1	Forbidden

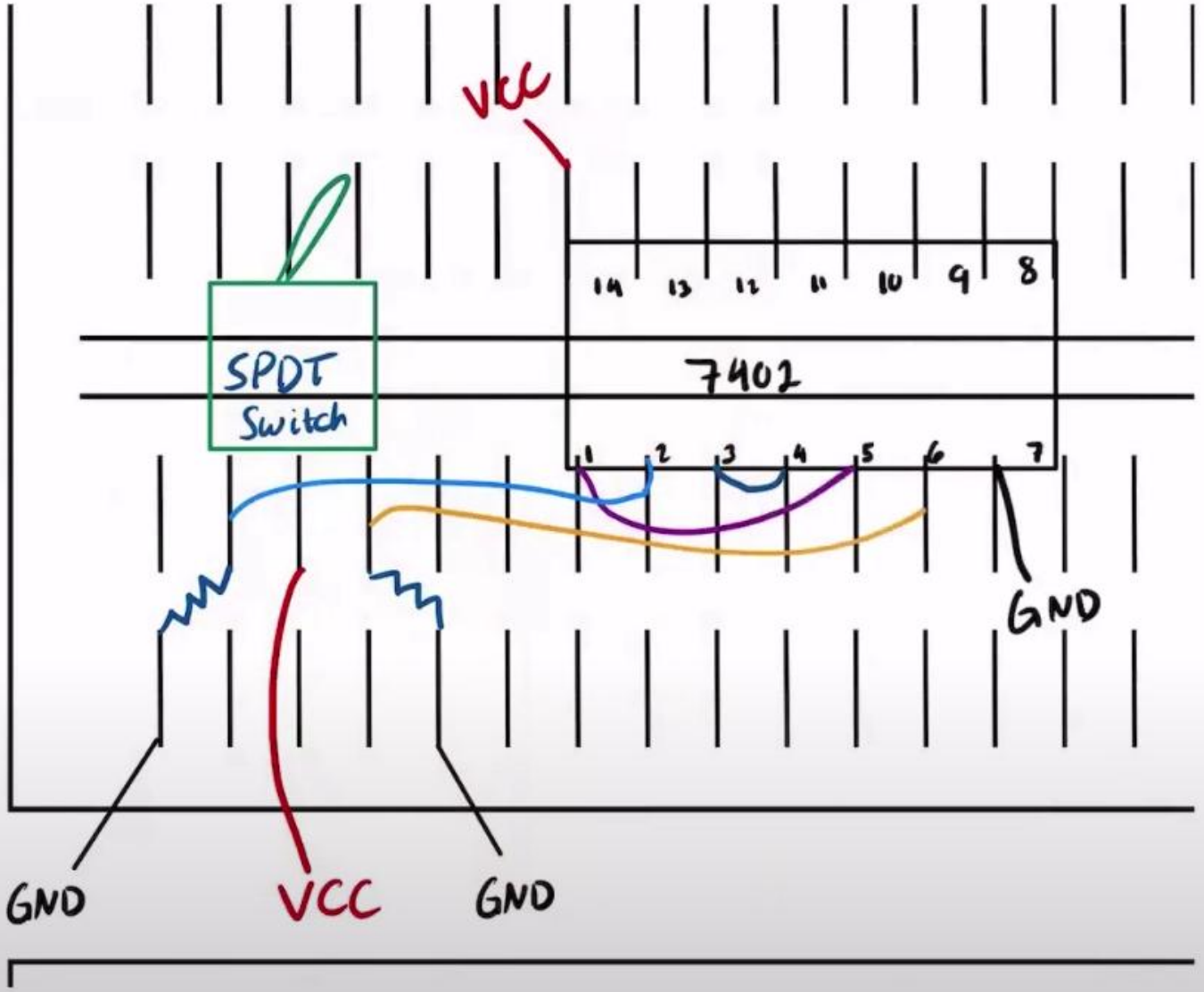
SR Latch - Breadboard



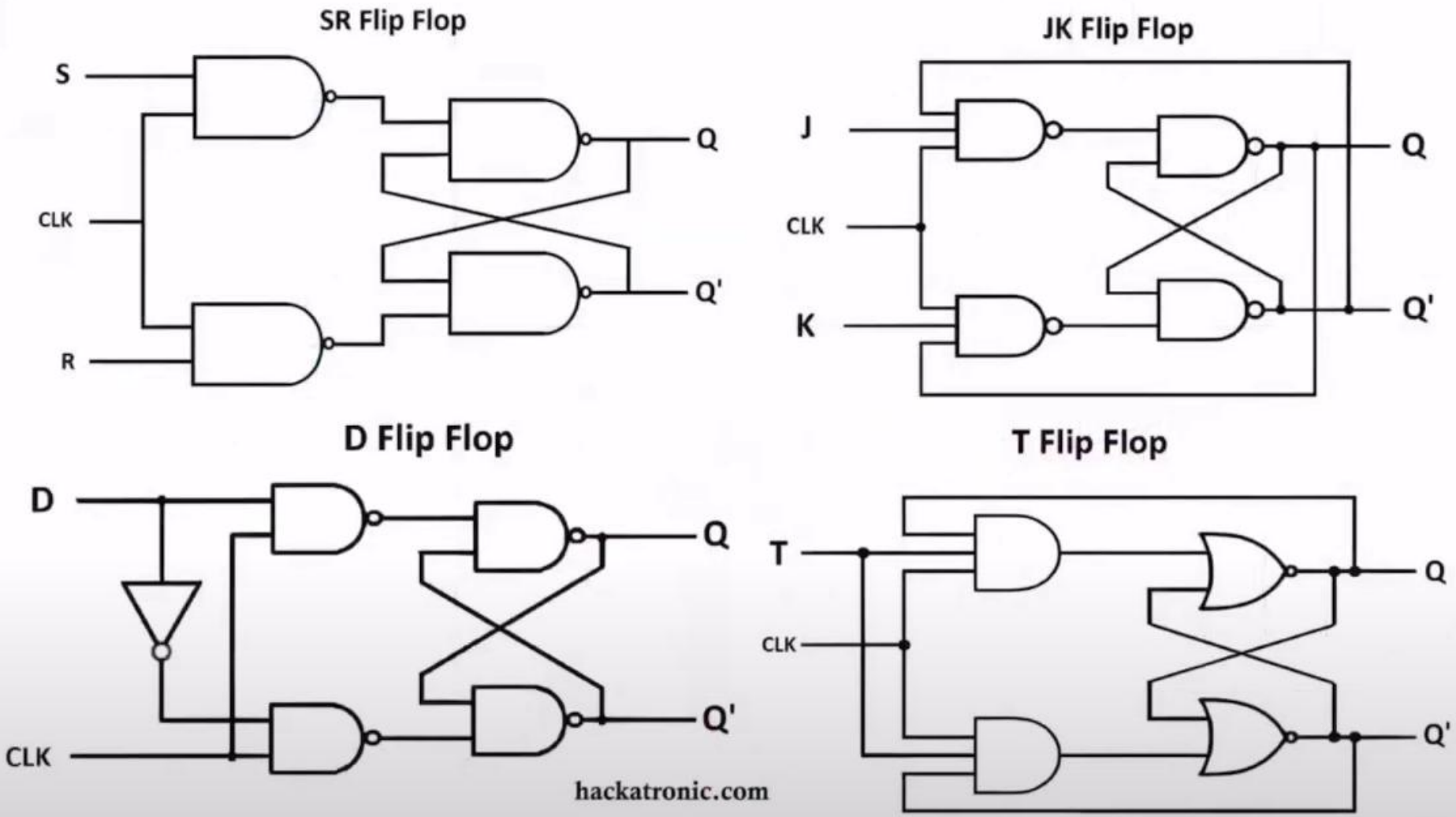


More S-R Latch





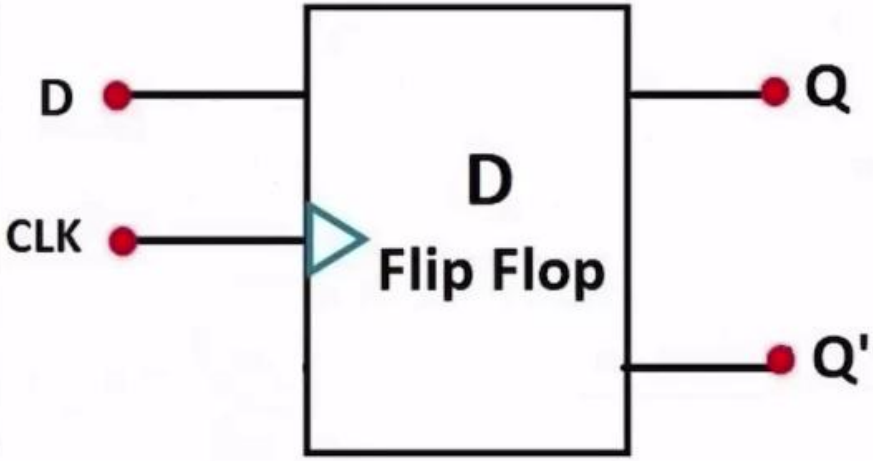
Types of FFs (Built from SSIs)



D Flip Flop

Truth Table of DFlip Flop

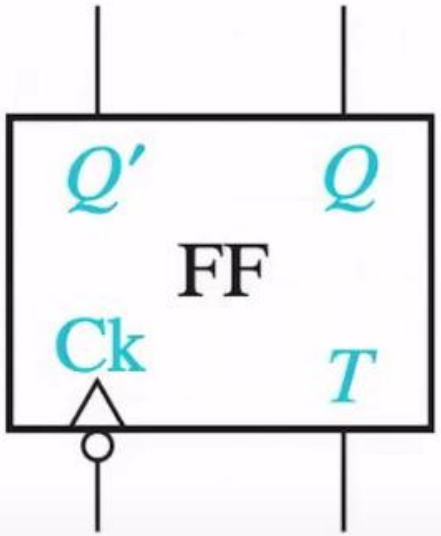
D	CLK	Q	Q`
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



hackatronic.com

D Flip Flip:
Input of D at Clock = Output (Q)

T Flip Flop



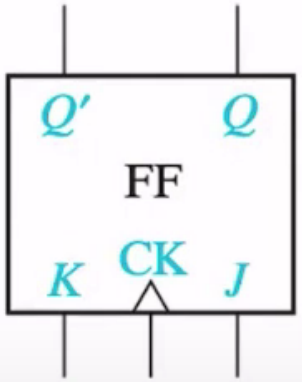
(a)

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

(b)

T Flip Flip:
When T is true, the input at D is toggled.

JK Flip Flop



(a) J-K flip-flop

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b) Truth table and characteristic equation

$$Q^+ = JQ' + K'Q$$

JK Flip Flip:

J = Set K = Reset

Possible Combinations

Nothing True → Output = Input
J → Output = 1
K → Output = 0
Both True → Output = Toggled Input

Counter Design

1 → 5 → 0 → 4 → 1

001 → 101 → 000 → 100 → 001

Show synchronous vs asynchronous

1) NSTT
2) K-Maps
3) FF Equations
4) Design
5) Simulate
6) Build

Next State Truth Table

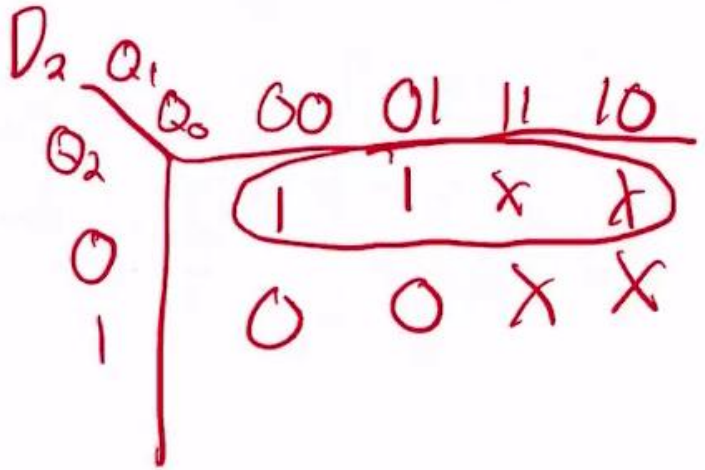
1 → 5 → 0 → 4 → 1 ←

Q_2 Q_1 Q_0	Q_2^+ Q_1^+ Q_0^+
0 0 0	1 0 0
0 0 1	1 0 1
0 1 0	X X X
0 1 1	X X X
1 0 0	0 0 1
1 0 1	0 0 0
1 1 0	X X X
1 1 1	X X X

Next State Truth Table

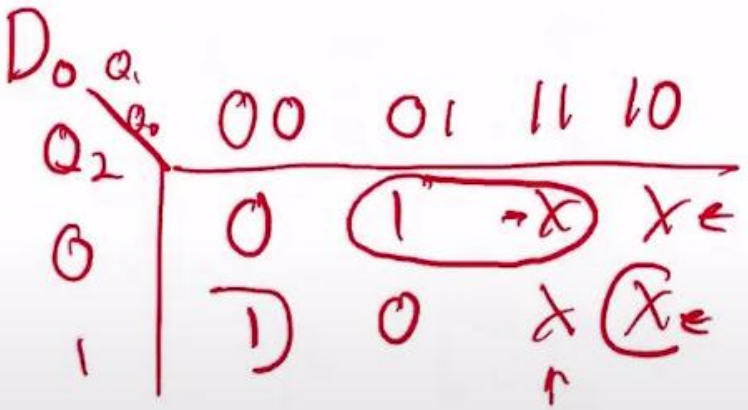
1 → 5 → 0 → 4 → 1 ←

Q_2 Q_1 Q_0	D_2: Q_2^+	D_1: Q_1^+	D_0: Q_0^+
0 0 0	1	0	0
0 0 1	1	0	1
0 1 0	X	X	X
0 1 1	X	X	X
1 0 0	0	0	1
1 0 1	0	0	0
1 1 0	X	X	X
1 1 1	X	X	X



$D_2 = \overline{Q_2}$

$Q \rightarrow GND$



$D_0 = \overline{Q_2}\,Q_0 + Q_2\,\overline{Q_0}$

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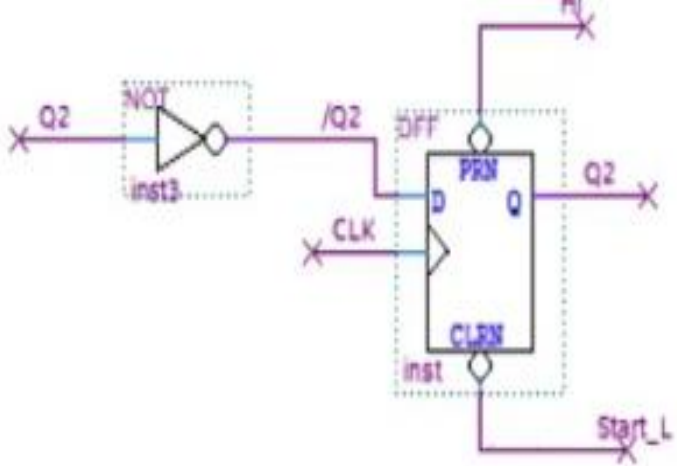
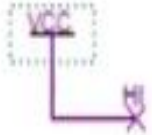
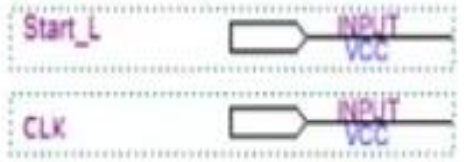
PI: Landon A

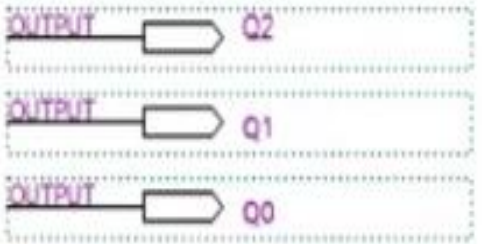
Date: 02/18/24

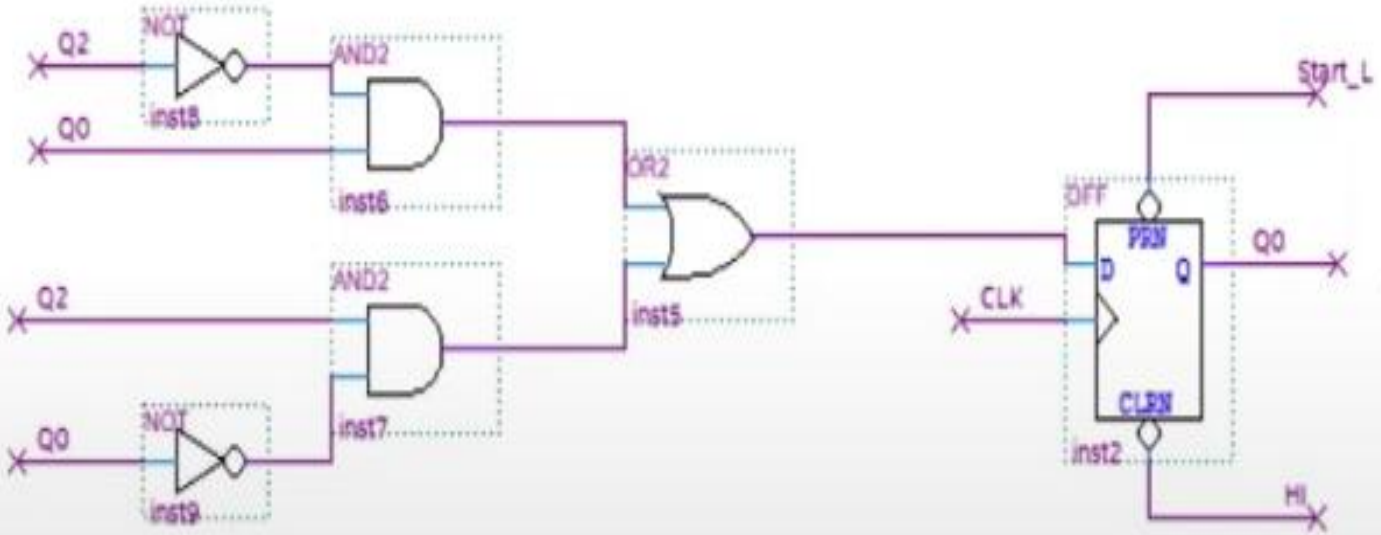
Descirption Counter

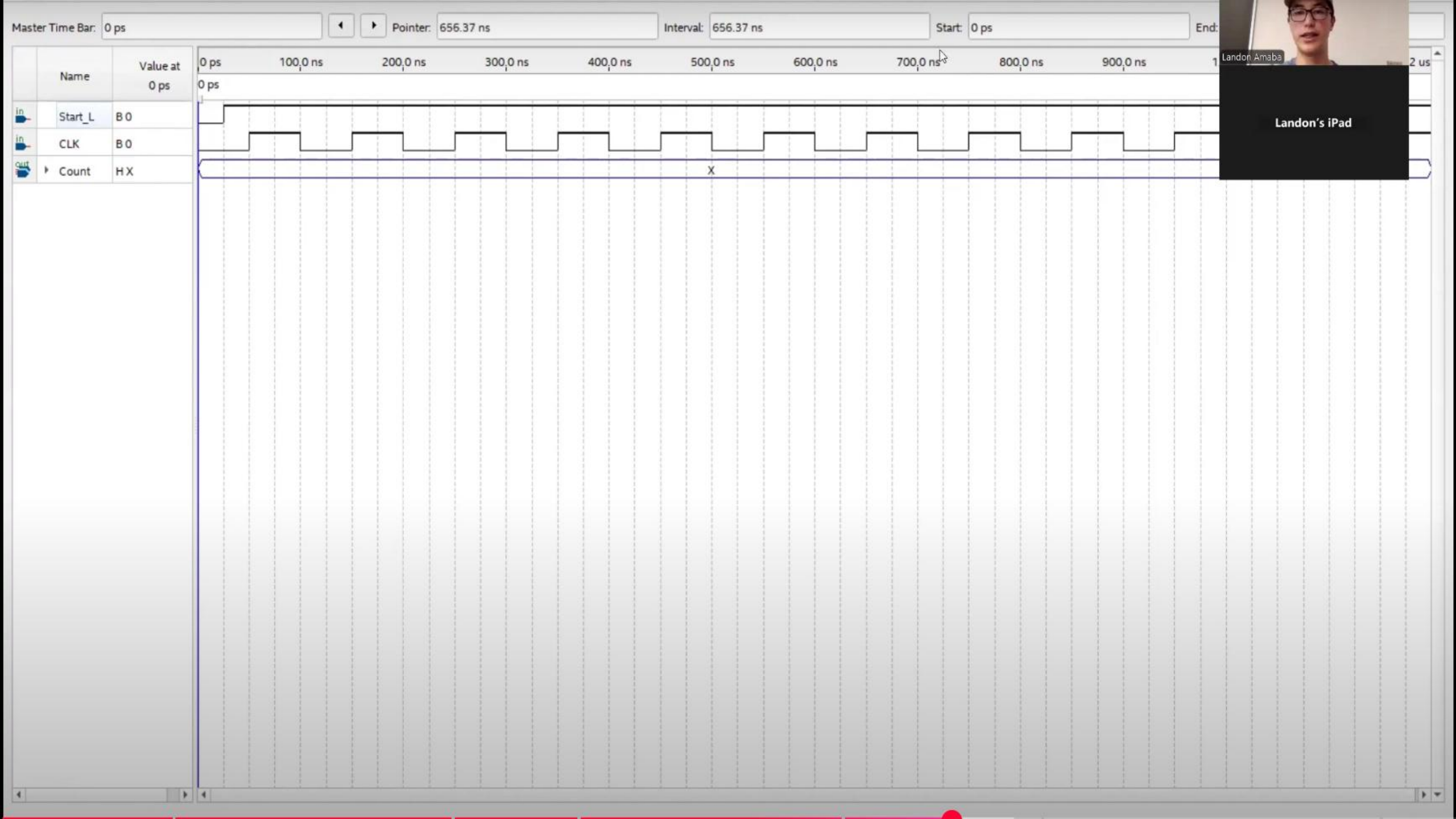











Master Time Bar: 0 ps
Pointer: 656.37 ns
Interval: 656.37 ns
Start: 0 ps
End:
Name
Value at 0 ps
Start_L
B 0
CLK
B 0
Count
H X
0 ps
100.0 ns
200.0 ns
300.0 ns
400.0 ns
500.0 ns
600.0 ns
700.0 ns
800.0 ns
900.0 ns
2 us
X
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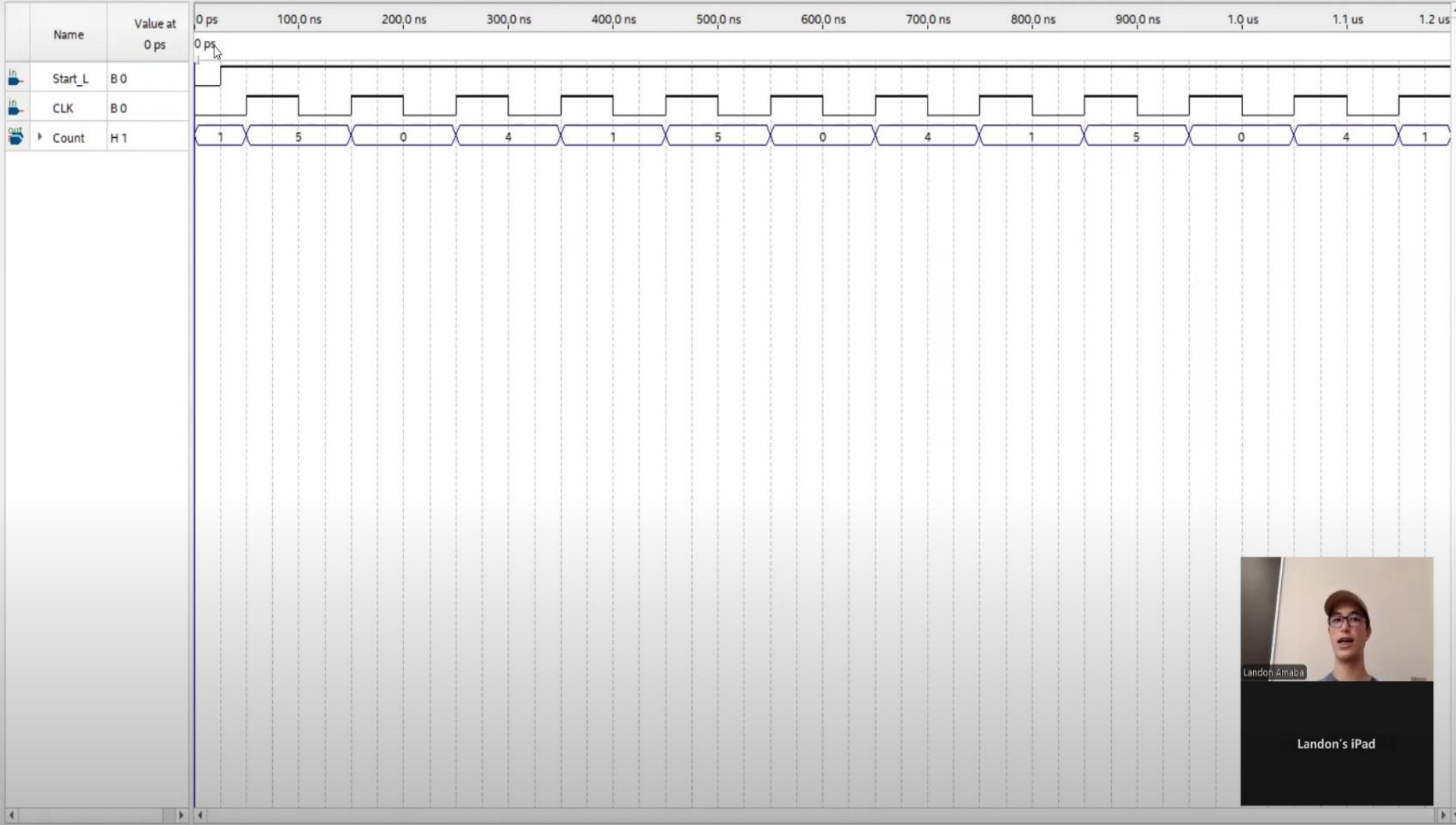
Landon's iPad


Name
Value at
0 ps
0 ps
100.0 ns
200.0 ns
300.0 ns
400.0 ns
500.0 ns
600.0 ns
700.0 ns
800.0 ns
900.0 ns
1.0 us
1.1 us
1.2 us
Start_L
B 0
CLK
B 0
Count
H 1
1
5
0
4
1
5
0
4
1
5
0
4
1
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Landon's iPad

Quartus Demo

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	J_0	K_0
0	0	0	1	0	0	1	0	X
0	0	1	1	0	1	1	x	0
0	1	0	x	x	x	x	x	x
0	1	1	x	x	x	x	x	x
1	0	0	0	0	1	1	1	X
1	0	1	0	0	0	1	x	1
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

$D_2 = \overline{Q_2}$

$T_2 = Q_2$

$J_0 = Q_2$

$K_0 = Q_2$

00
01
00 = X0
10
10
11 = 1X
01
11 = X1

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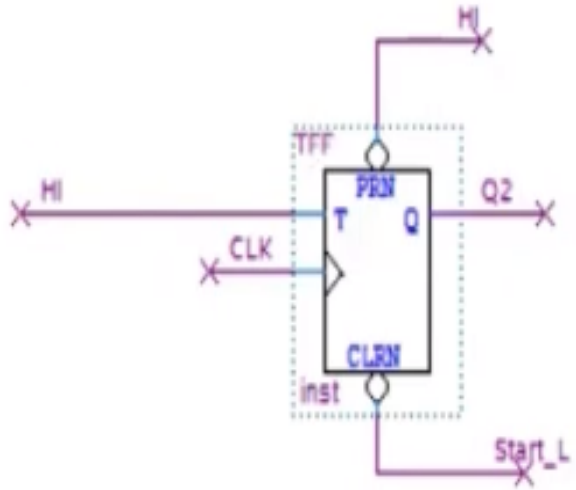
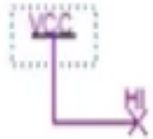
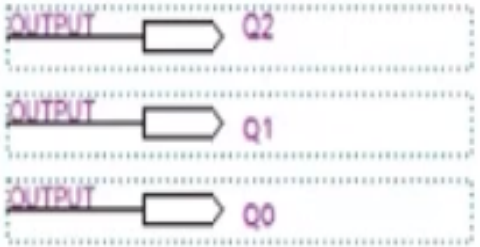
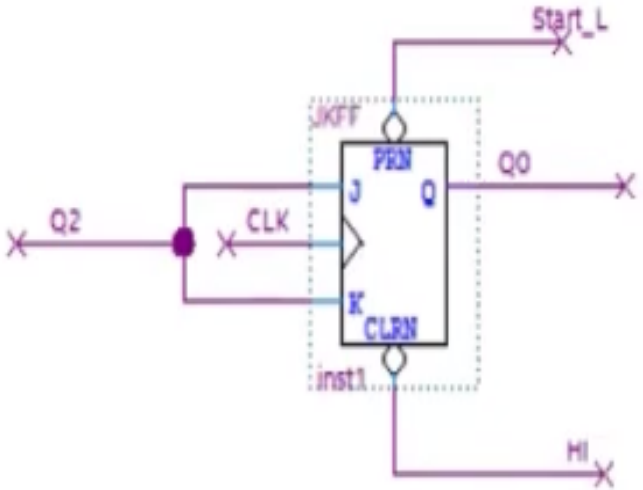
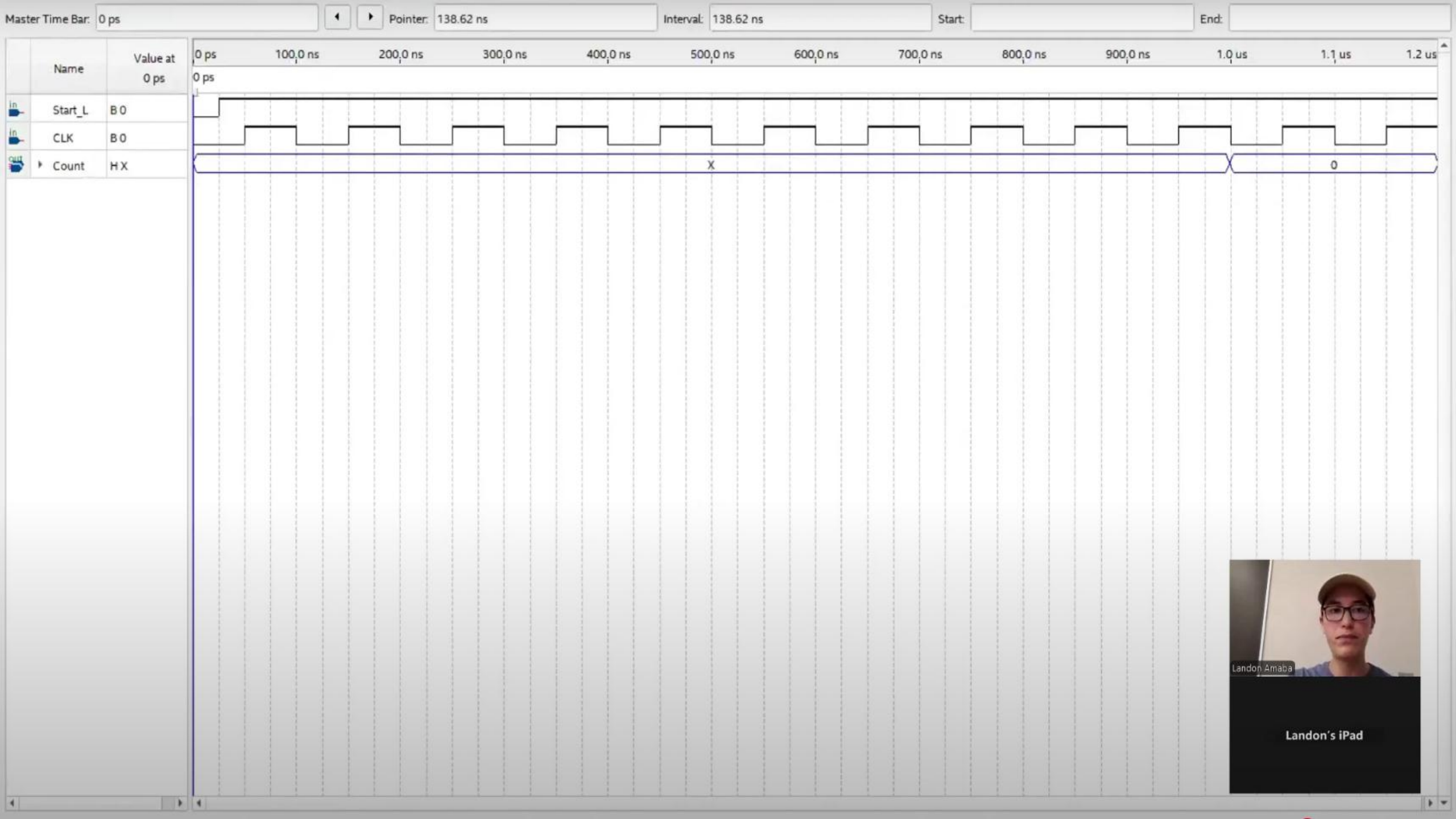
Descirption Counter with JK










Master Time Bar: 0 ps
Pointer: 138.62 ns
Interval: 138.62 ns
Start:
End:
Name
Value at 0 ps
0 ps
100.0 ns
200.0 ns
300.0 ns
400.0 ns
500.0 ns
600.0 ns
700.0 ns
800.0 ns
900.0 ns
1.0 us
1.1 us
1.2 us
Start_L
B 0
CLK
B 0
Count
H X
X
0
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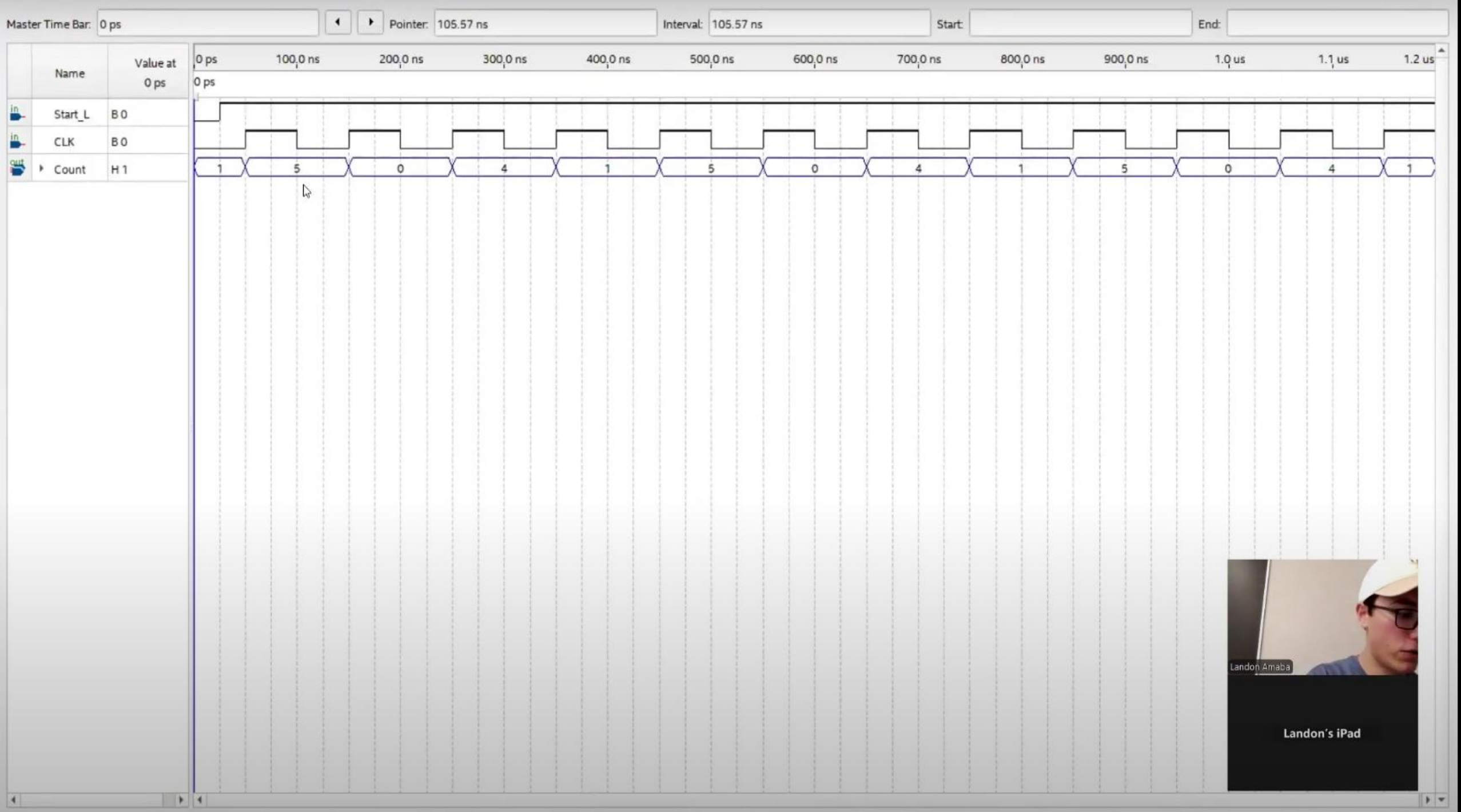
Master Time Bar: 0 ps
Pointer: 105.57 ns
Interval: 105.57 ns
Start:
End:
Name
Value at 0 ps
Start_L
B 0
CLK
B 0
Count
H 1
0 ps
100.0 ns
200.0 ns
300.0 ns
400.0 ns
500.0 ns
600.0 ns
700.0 ns
800.0 ns
900.0 ns
1.0 us
1.1 us
1.2 us
1 5 0 4 1 5 0 4 1 5 0 4 1
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