
REQUIREMENTS NOT MET

N/A

PROBLEMS ENCOUNTERED

When switching between devices from MAX V back to MAX X, there were some compilation errors, where I would have to select from “Device | Available Devices” in order to successfully compile when switching back from MAX V.

HOMework EXERCISES

<insert copy of homework problem numbers from homework document, as well as an answer directly following each of the questions (if not applicable, write “N/A”); also specify the Roth textbook version number you used; all scans must be clear and legible>

I. Creating a Project In Quartus

a. A New Project Design Creation

- i. N/A
- ii. N/A
- iii. N/A
- iv. N/A
- v. N/A
- vi. N/A
- vii. N/A
- viii. N/A

b. Configuring Quartus Window

- i. N/A
- ii. N/A

II. Designing

a. Creating A BDF

- i. N/A
- ii. N/A
- iii. N/A

b. Adding Text

- i. N/A
- ii. N/A
- iii. N/A
- iv. N/A
- v. N/A
- vi. N/A
- vii. N/A
- viii. N/A

c. Component Selection Process and Moving Components

- i. N/A
- ii. N/A
- iii. N/A
- iv. N/A
- v. N/A
- vi. N/A
- vii. N/A
- viii. N/A
- ix. N/A
- x. N/A
- xi. N/a
- xii. N/A

d. Adding/Deleting Wires

- i. N/A
- ii. N/A
- iii. N/A
- iv. N/A
- v. N/A
- vi. N/A

e. Adding Input and Output Ports

- i. N/A
- ii. N/A
- iii. N/A
- iv. N/A
- v. N/A
- vi. N/A

Homework 1 Tutorial
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Description: $Y = A * /B + /C$

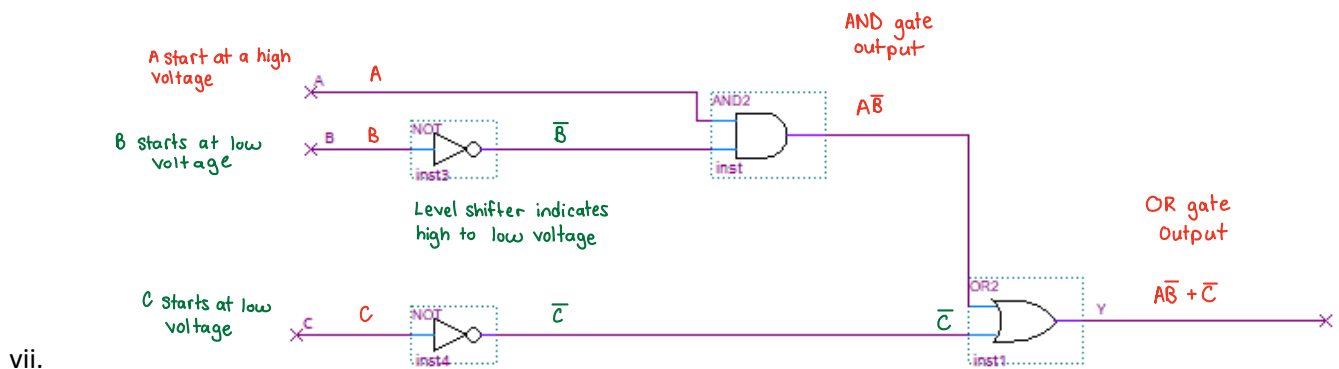
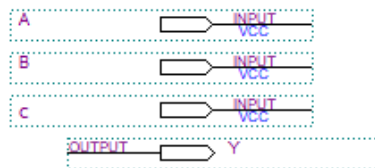


Figure 1: BDF with inputs and outputs

f. Full Compilation (for programming your PLD)

- i. N/A
- ii. N/A

g. Functional Compilation (for simulation only)

- i. N/A
- ii. N/A

III. Simulating

a. Creating a VWF (Vector Waveform)

- i. N/A
- ii. N/A

b. Adding Signals

- i. N/A
- ii. N/A
- iii. N/A

c. Changing Grid Size and End Table Time

- i. N/A
- ii. N/A
- d. Manually Changing VWF

i. N/A

ii. N/A

iii. N/A

iv. N/A

v. N/A
- e. Functional and Timing Simulation

i. N/A

A_H	B_L	C_L	Y_H = A * /B + /C
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Figure 2: Logic Table for $Y = A * /B + /C$

A_H	B_L	C_L	Y_H = A * /B + /C
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

Figure 3: Voltage Table for $Y = A * /B + /C$

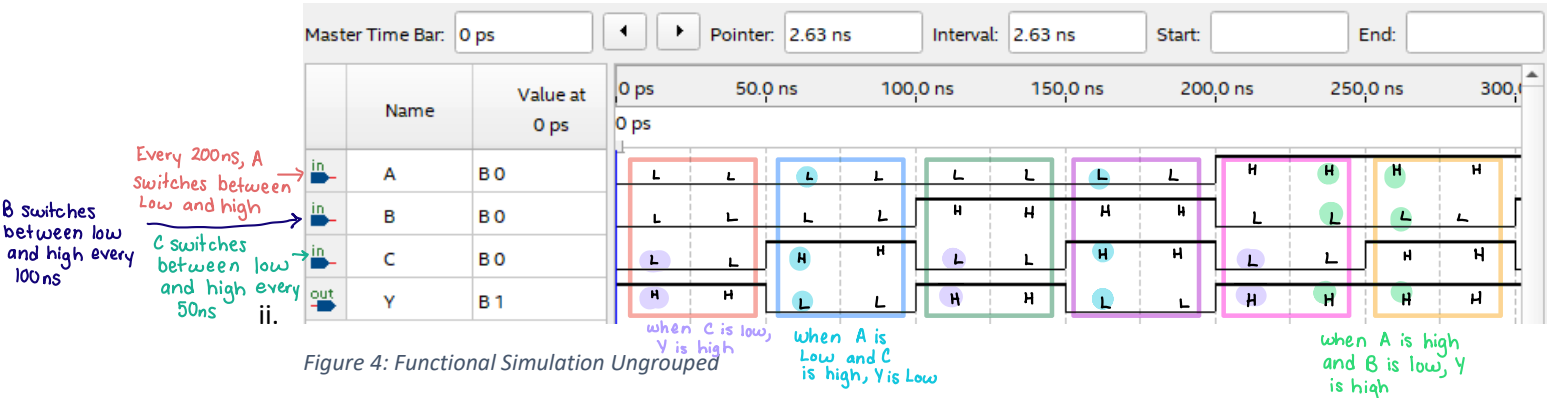
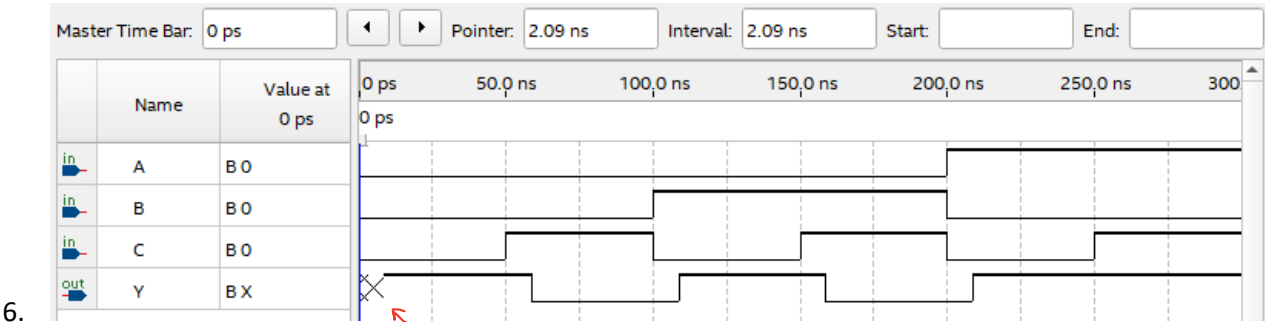


Figure 4: Functional Simulation Ungrouped

- iii. N/A
1. N/A
2. N/A
3. N/A

4. N/A
5. N/A



- Figure 5: Time Simulation Ungrouped
- iv. N/A

v. N/A

vi. N/A

vii. N/A
- f. Grouping Signals and Using Count Value and Clock Value
- i. N/A

ii. N/A

iii. N/A

iv. N/A

v. N/A

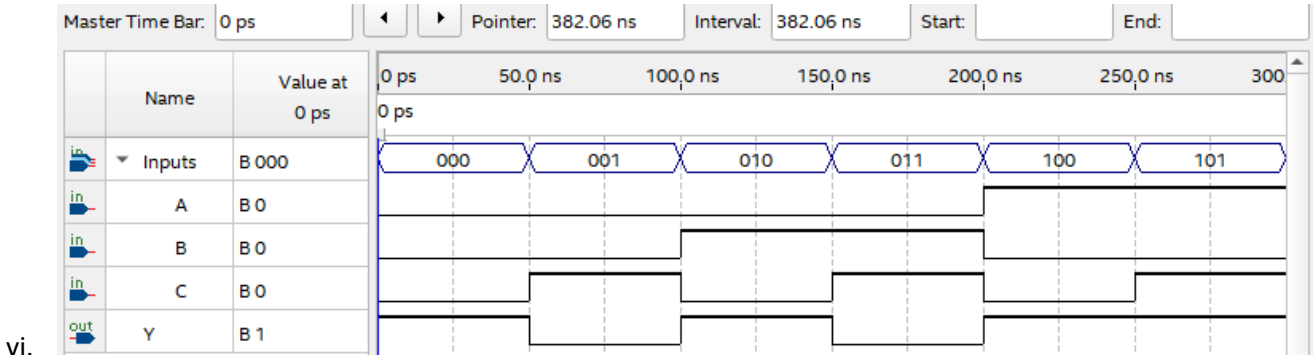


Figure 6: Functional Simulation Grouped

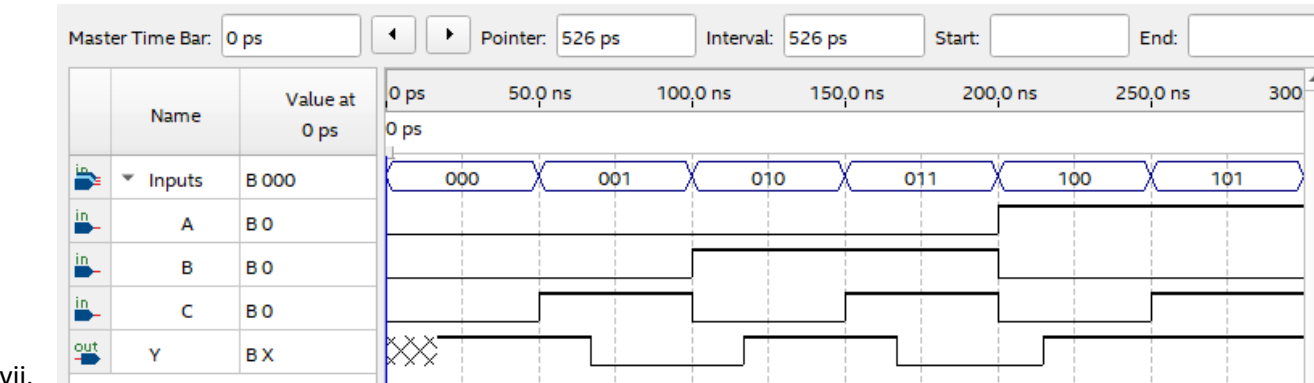


Figure 7: Time Simulation Grouped

V. Archiving Your Project

- a. Archiving your project into a qar file
 - i. N/A
 - ii. N/A
- b. Un-archiving (restoring) your project into a qar file
 - i. N/A
 - ii. N/A
 - iii. N/A