EEL 3701C: Digital Logic & Computer Systems
Revision **0**
Lab 3 Report: **Introduction to State Machines**

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REQUIREMENTS NOT MET

The 3-bit counter doesn't properly do the sequence numbers, but it does count up and down.

VIDEO FILE LINK

<Place the link to your video ***here***. I suggest YouTube, OneDrive, DropBox, Google Drive, or iCloud. Verify that the link works!>

PROBLEMS ENCOUNTERED

Had some problems trying to get the simulation to run properly in Quartus and realized it was wiring issues. Additionally, there were times my DE10 would not want to show up on Quartus, but would show up in device manager.

FUTURE WORK/APPLICATIONS

Debounced switch circuits are important to improve reliability and accuracy when making circuits so results stay consistent. 3-Bit and 2-bit counters are one of the very basics in circuits and figuring out this is good practice for more complicated designs in the future.

PRE-LAB QUESTIONS OR EXERCISES

PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)

Each section of the pre-lab requirements should be completed separately, and in order. Include each of the following items in order. Note that some of these items will not apply to every lab. Anything scanned or copied ***must be clear and legible***.

- Logic equations. (Note that logic equations do not contain activation levels.)
- **All** tables and figures should have captions with Figure/Table numbers and a description of for which part of the lab it references, e.g., ***Table 3****: Truth Table for Part B.*
- Truth tables and voltage tables (and/or next-state truth tables).
- When applicable, include Karnaugh Maps (i.e., K-Maps).
- Include hand-drawn circuits (when required). Label all input and output activation-levels and intermediate equations in the circuits.
- Include screenshots of the BDF designs of circuits.
  - Label all input and output activation-levels, i.e., use _L suffix for active-low signals and no suffix for active-high signals. **Add chip and pin numbers to any schematic that will be constructed.**
  - Images should be large enough so that inputs, outputs, labels, and parts are clearly visible and distinguishable to any reader.
  - Each BDF should have the following info on the top left corner (similar to the top right of this page):

    Last Name, First Name
    Lab #, Part #
    Class #
    PI Name:
    Description: (short description of what is to be accomplished in the design; perhaps an equation)

  - In Windows, I use the ***Snipping Tool***, which is now built into Windows. Just type "snip" in the Windows search box and then select ***Snipping Tool***.
- When necessary, include ASM Charts. These can be hand-drawn, but clear and legible. We recommend that you use resources like https://www.draw.io/ to create computer-generated ASMs.
- Truth tables or next-state truth tables should have the following characteristics.
  - Can be either typed or hand-written and scanned (must be clear and legible)
  - Must be in **counting order** (i.e., inputs of 000, 001, 010, 011, …, 111)
  - Clearly distinguish inputs from outputs (see the example below that uses a thick line)
  - If you are designing a state machine or a controller, clearly indicate and separate signal values both before the clock and after the clock (i.e., Q1 and $Q1^+$, respectively)
  - Tip: divide rows into consecutive groups of 4 (or 2 or 8) to make it easier for both you and your PI to read.
  - **Example**

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Table: Caption for above table. It should reference the part of the lab, e.g., "Table 3: Truth Table for Part B."

- Voltage tables should have the following characteristics.
  - Must be in counting order (i.e., inputs of LLL, LLH, LHL, … , HHH)
  - Use similar formatting to truth tables (described above)

- **Example**

A(H)	B(H)	C(L)	Y(L)
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

- Include **meaningfully annotated** functional simulations.
  - Using the grouping tool, ***group as many signals together as possible*** (when it makes sense to group them)! If you are simulating a basic logic equation, group all the inputs together. If you are simulating a circuit that includes MSI elements, group signals of the form X_{N-0}. The most-significant bit should appear first, ending with the least-significant bit. If you are simulating an ALU, group the buses together as just described.
  - Not every row of your voltage table must be annotated in the waveform simulation, but your choices of rows that you annotate must be ***encompassing***
  - If you are designing a state machine or a controller, your CLK signal should appear ***at the top*** of your inputs and outputs. The general order is CLK -> Reset -> state bits -> inputs -> outputs.
  - ***Tip***: Use Microsoft Paint to annotate your waveforms. An alternative is to print out the waveforms, annotate them by hand, then scan and upload
  - ***Hint***: Consider a truth table where the output is true in significantly less cases than it is false (or vice versa). If the output signal is active-high, it would be wise to annotate only the cases where the output voltage is HIGH.
- Include every line of VHDL programs, including both ***architecture*** and ***behavior*** sections.
- Include every line of any **MIF** files. If these are associated with assembly language programs, you can either put the assembly code as comments or separately include assembly language programs

1. Debounced Switch Circuit

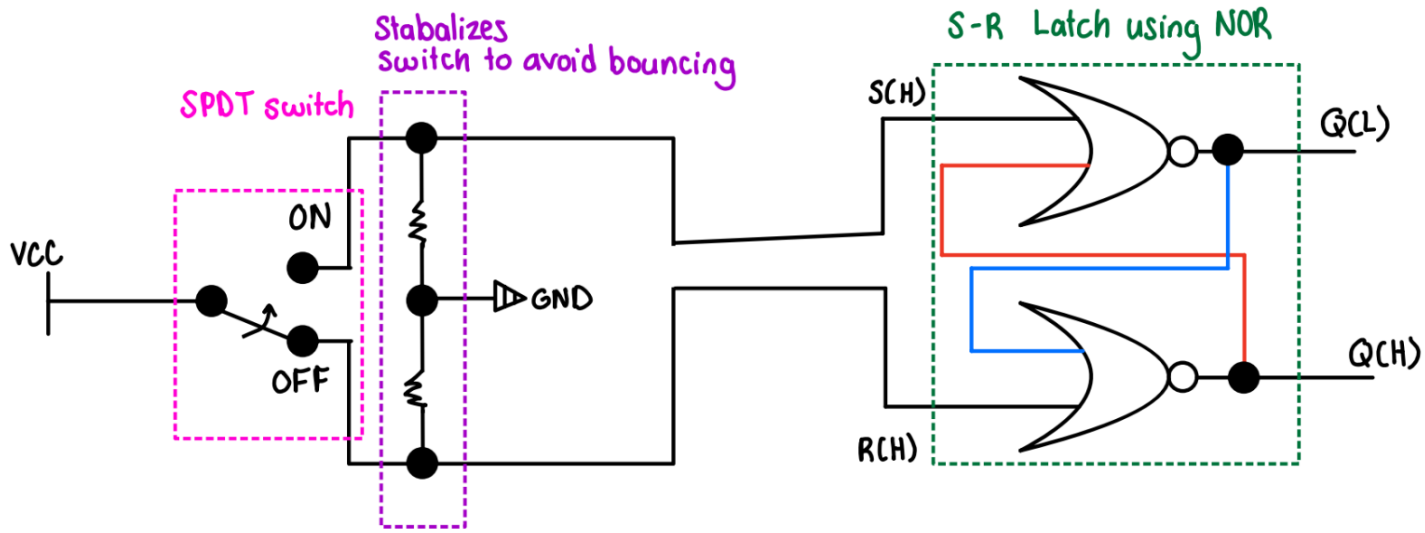


Figure 1: Lab 3 Part 1.1 - On Paper design for debounced switch circuit with clock input using SPDT and 2 NOR gates

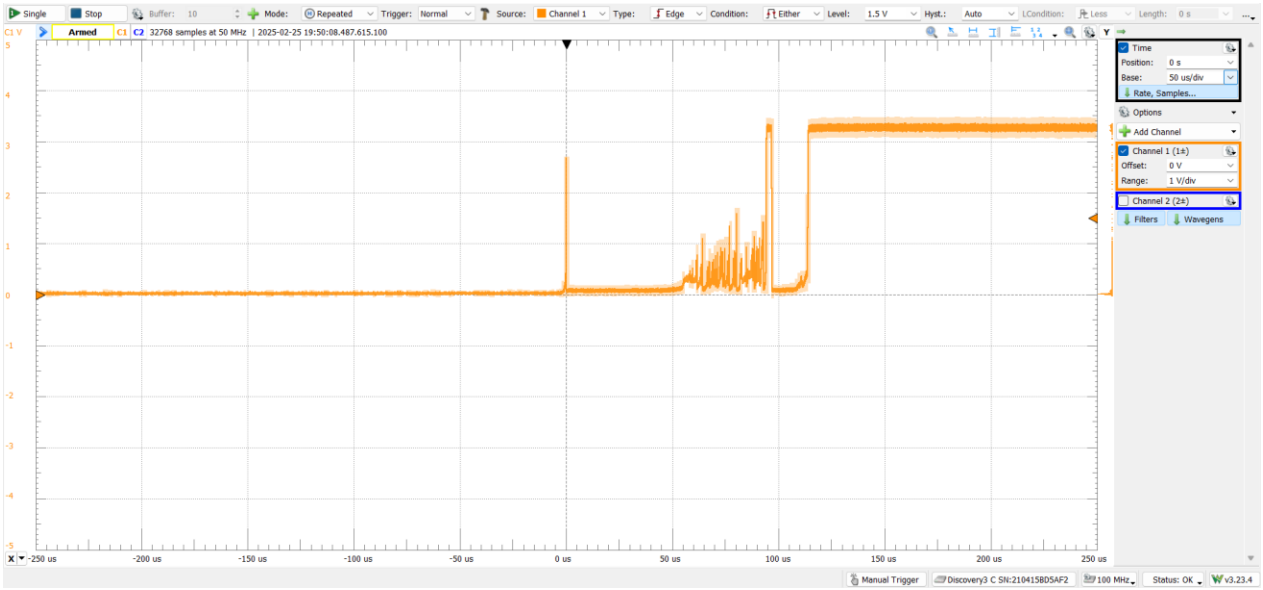


Figure 2: Lab 3 Part 1.3 - Bouncing with Time Base 50 us/div Screenshot 1

Interpretation of if it was a 5-bit counter from 0-31 counts: 1 clock

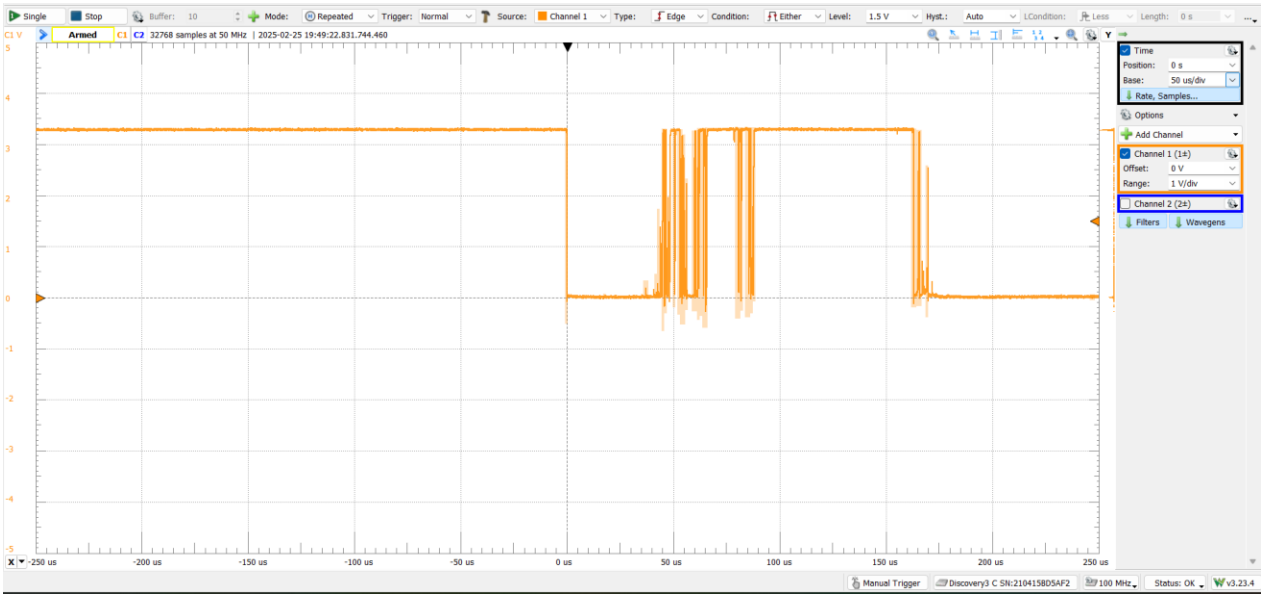


Figure 3: Lab 3 Part 1.3 - Bouncing with Time Base 50 us/div Screenshot 2

Interpretation of if it was a 5-bit counter from 0-31 counts: 7 clocks

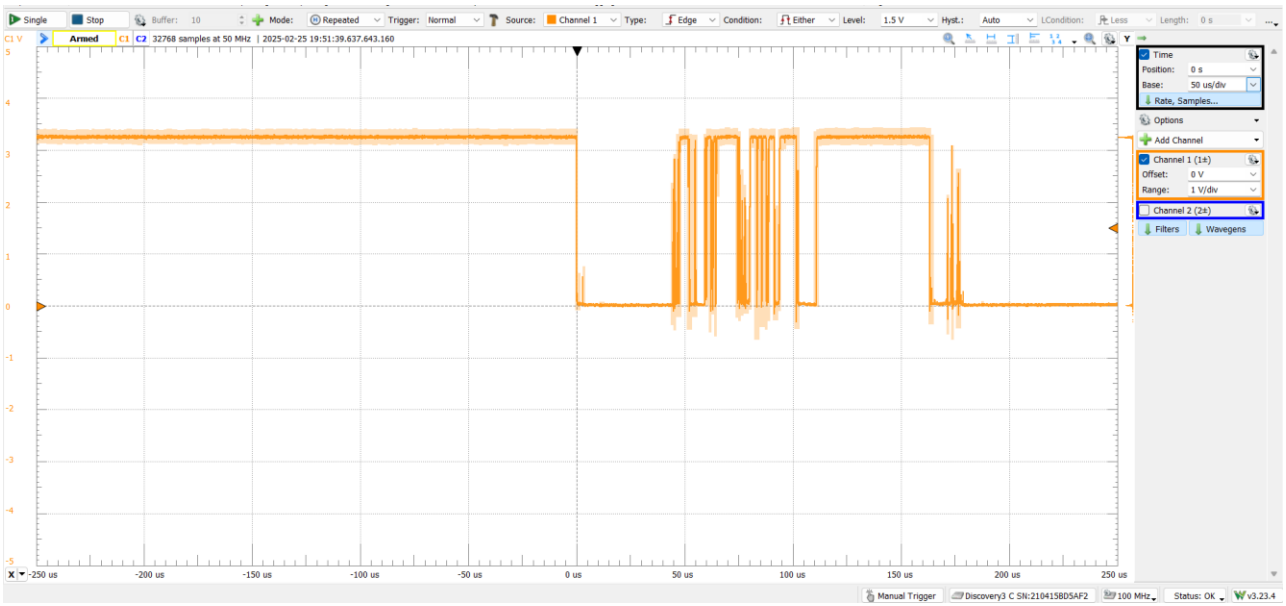


Figure 4: Lab 3 Part 1.3 - Bouncing with Time Base 50 us/div Screenshot 3

Interpretation of if it was a 5-bit counter from 0-31 counts: 9 clocks

Figure 5: Lab 3 Part 1.4 - Debounced Switch Circuit with the SPDT at 50 us/div Screenshot 1

Figure 6: Lab 3 Part 1.4 - Debounced Switch Circuit with the SPDT at 50 us/div Screenshot 2

Figure 7: Lab 3 Part 1.5 - Bouncing with Internal NOR gates, Time Base 50 us/div Screenshot 1

Figure 8: Lab 3 Part 1.5 - Bouncing with Internal NOR gates, Time Base 50 us/div Screenshot 2

2. Two-Bit Counter Design

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	1
1	0	0	0
1	1	1	0

Figure 9: Lab 3 Part 2.1.a - Next State Truth Table for Counter

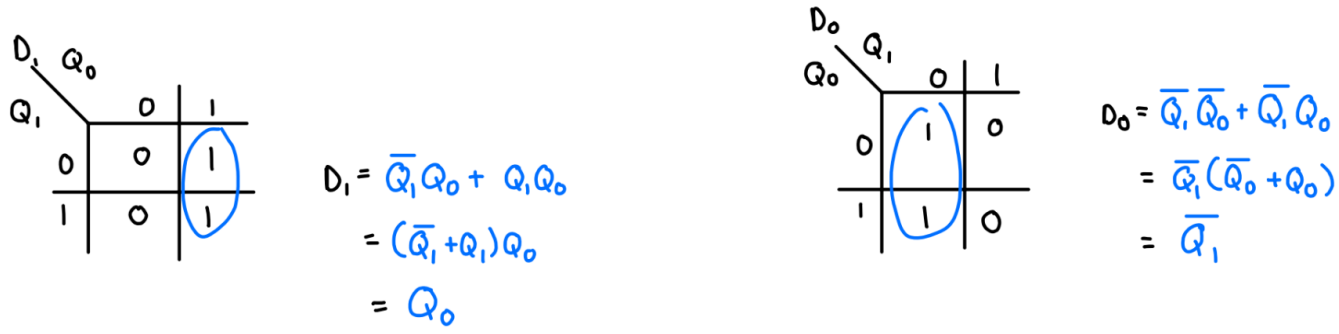


Figure 10: Lab 3 Part 2.1.b - D-Flip-Flops to determine next state equations and MPOS equations.

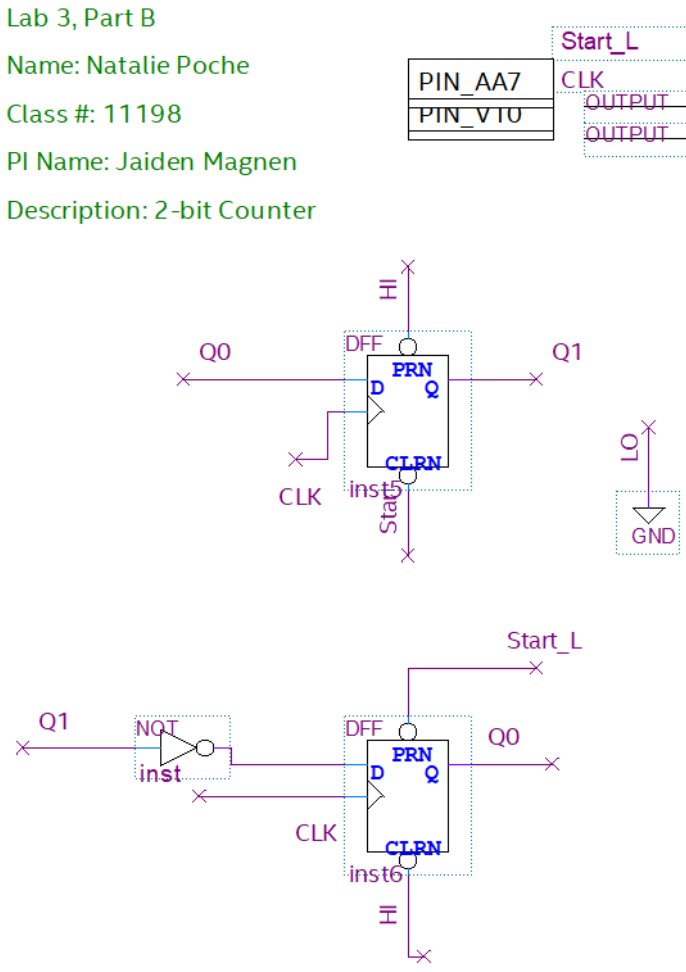


Figure 11: Lab 3 Part 2.1.c - Quartus 2 bit counter

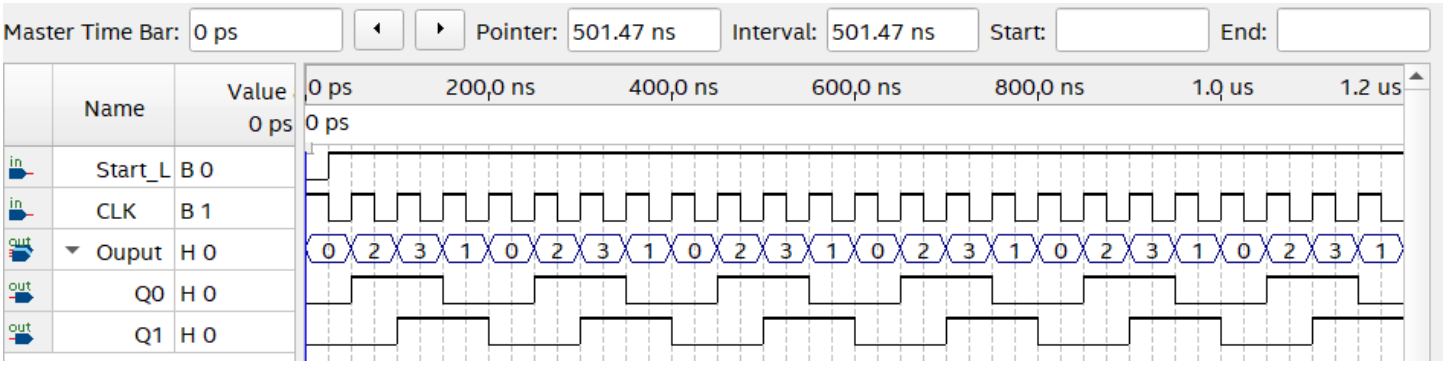


Figure 12: Lab 3 Part 2.1.e - Functional Simulation of 2 bit counter

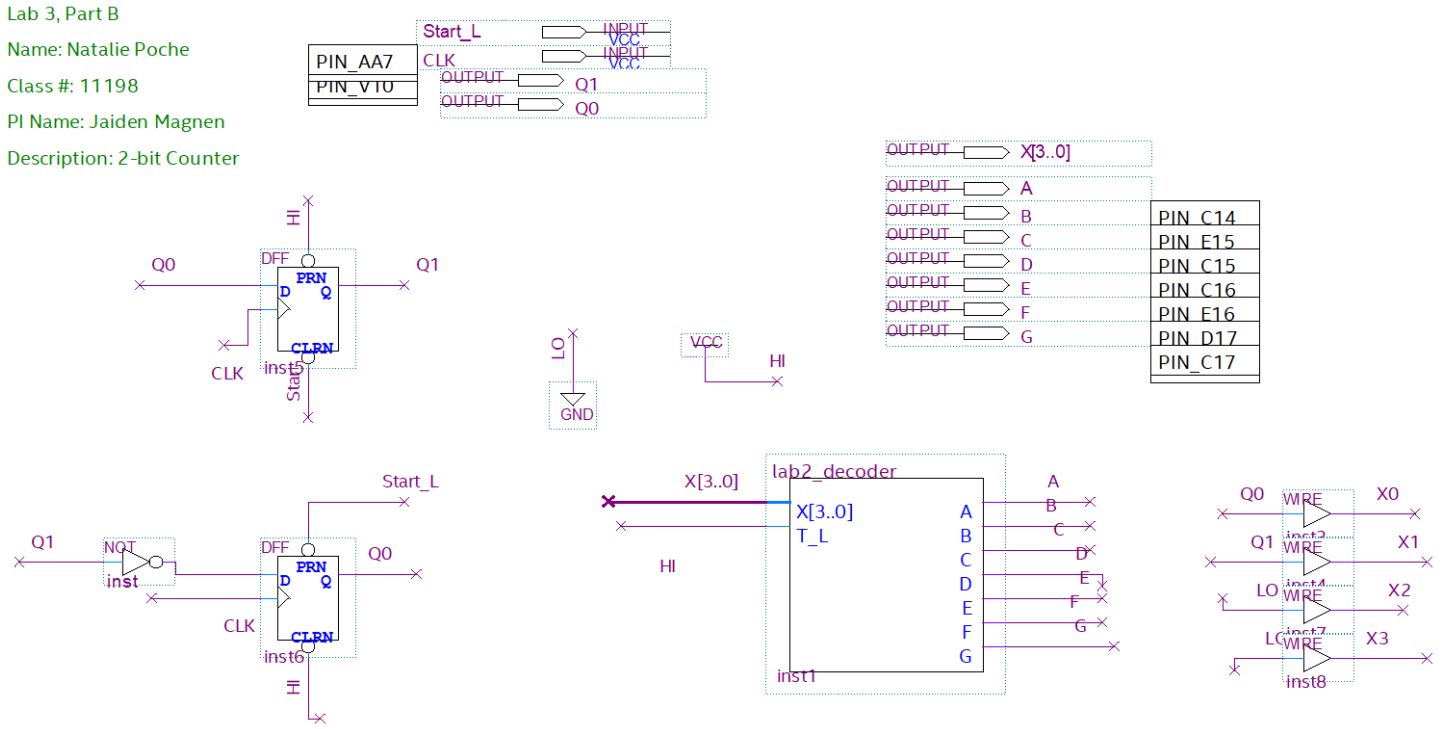


Figure 13: Lab 3 Part 2.2 - BDF of 2-bit counter with hex decoder

Clock	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Expected	2	3	1	0	2	3	1	0	2	3
Actual	2	1	2	1	2	0	3	2	1	1

Figure 14: Lab 3 Part 2.4.f - Table with toggle flip SPST switch to compare expectations and actual results

Analysis of Results:

A Debounced switch circuit has more consistent results that are closer to the expectation than an undebounced switch circuit.

3. Three-Bit Counter Design

F	B	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	Sp
0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	0
0	0	0	1	0	0	1	0	0
0	0	0	1	1	0	1	1	1
0	0	1	0	0	1	0	0	0
0	0	1	0	1	1	0	1	0
0	0	1	1	0	1	1	0	0
0	0	1	1	1	1	1	1	0
0	1	0	0	0	0	1	0	0
0	1	0	0	1	X	X	X	0
0	1	0	1	0	1	1	1	0
0	1	0	1	1	1	0	0	1
0	1	1	0	0	0	0	0	1
0	1	1	0	1	X	X	X	0
0	1	1	1	0	X	X	X	0
0	1	1	1	1	0	1	1	0
1	0	0	0	0	1	0	0	0
1	0	0	0	1	X	X	X	0
1	0	0	1	0	0	0	0	0
1	0	0	1	1	1	1	1	1
1	0	1	0	0	0	1	1	0
1	0	1	0	1	X	X	X	0
1	0	1	1	0	X	X	X	0
1	0	1	1	1	0	1	0	0
1	1	0	0	0	X	X	X	0
1	1	0	0	1	X	X	X	0
1	1	0	1	0	X	X	X	0
1	1	0	1	1	X	X	X	1
1	1	1	0	0	X	X	X	1
1	1	1	0	1	X	X	X	0
1	1	1	1	0	X	X	X	0
1	1	1	1	1	X	X	X	0

Figure 15: Lab 3 Part 3.1 - Next State Truth Table

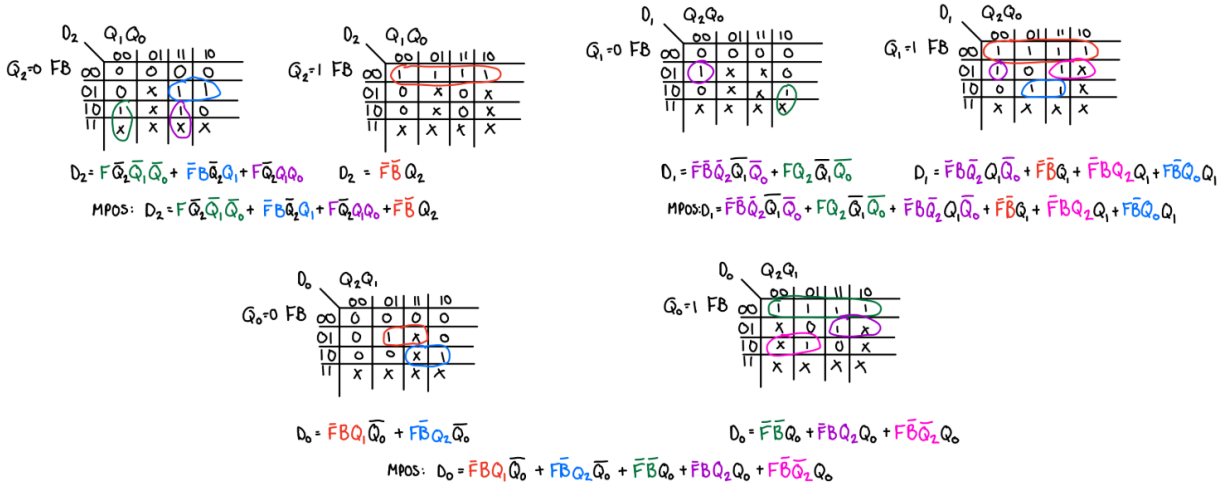


Figure 16: Lab 3 Part 3.2 - K-Maps and MPOS for 3-bit next state equations

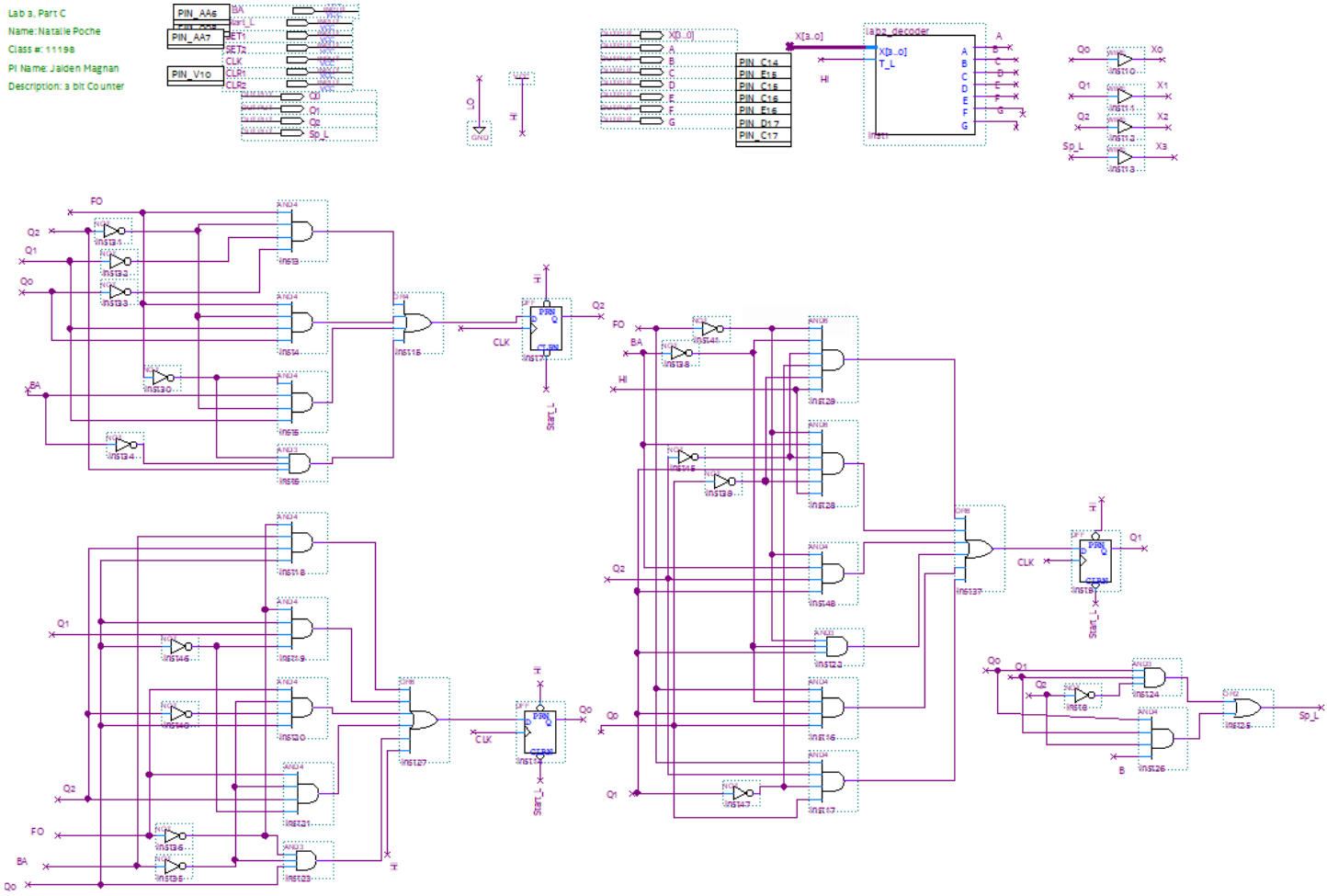


Figure 17: Lab 3 Part 3.4 - BDF of 3 bit Counter

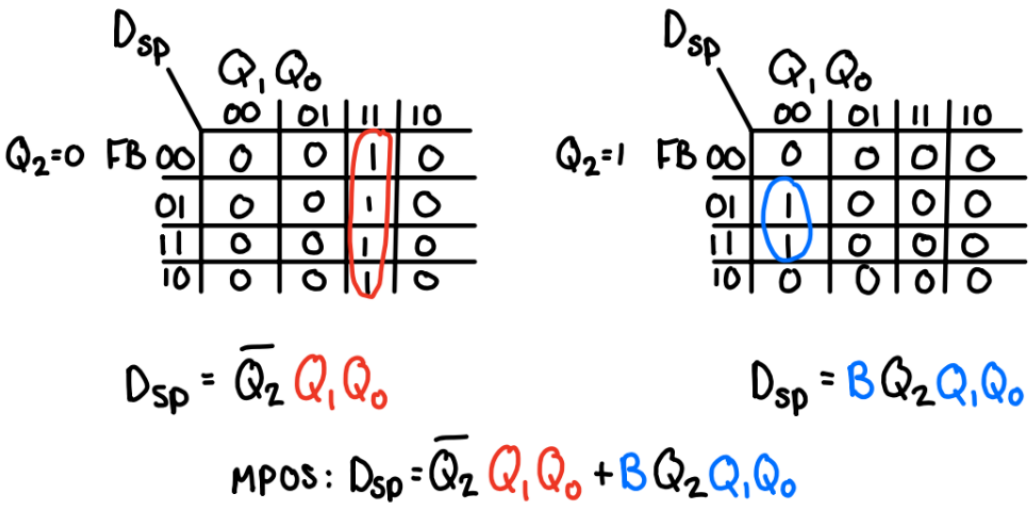
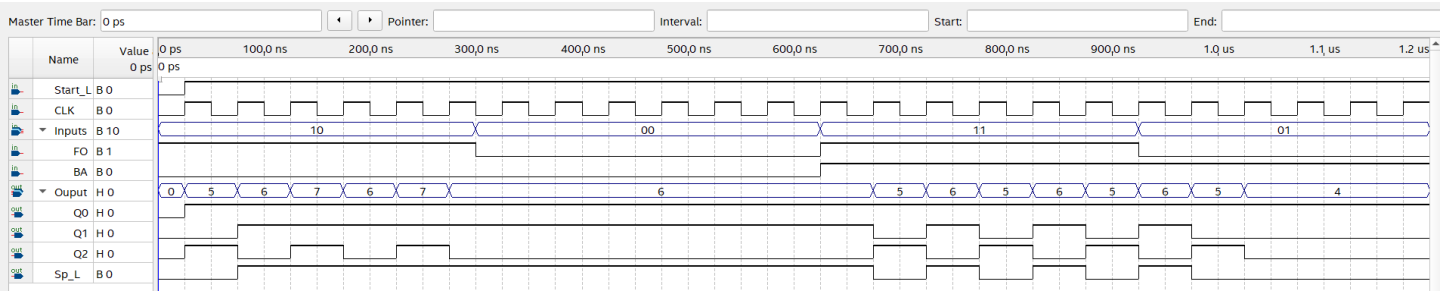


Figure 18: Lab 3 Part 3.3 - K-Map of Sp for 3-bit Counter and MPOS



4. Two-Bit Counter with Alternate Flip Flops

Q_1	Q_0	Q_1^+	Q_0^+	T_1	J_0	K_0
0	0	0	1	0	1	X
0	1	1	1	1	X	0
1	0	0	0	1	0	X
1	1	1	0	0	X	1

Figure 19: Lab 3 Part 4 - Next State Truth Table with J-K and T-FF

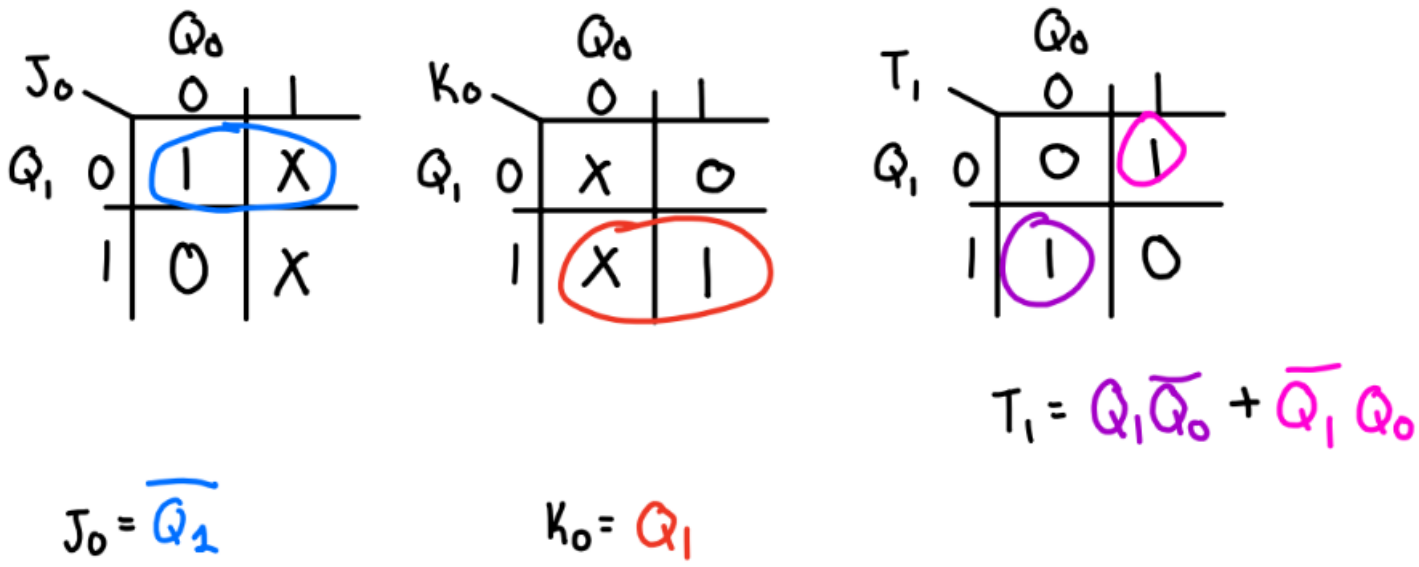


Figure 20: Lab 3 Part 4 - J-K and T Tables with Equations for 2 bit Counter

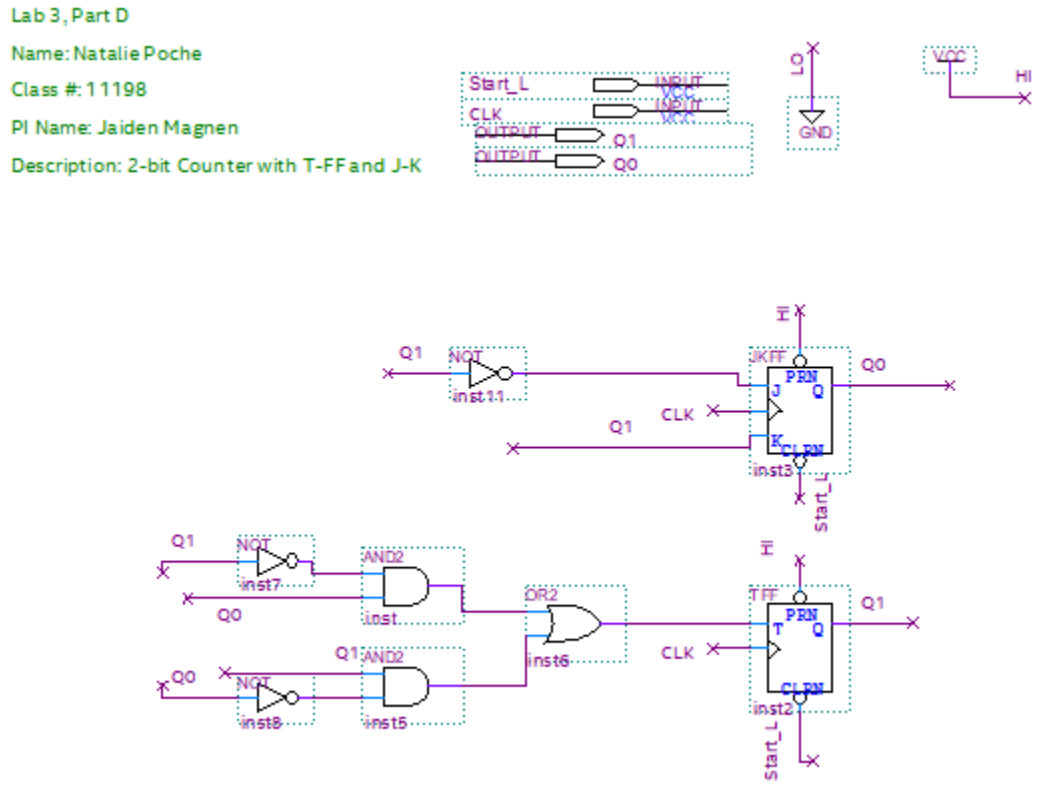


Figure 21: Lab 3 Part 4 - BDF of 2-bit counter with J-K FF and T-FF

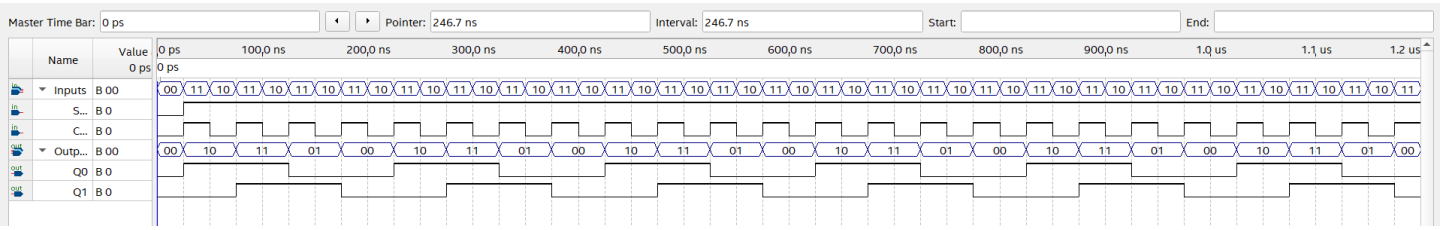


Figure 22: Lab 3 Part 4 - Functional Simulation of 2-bit counter with J-K FF and T - FF