EEL3701C – Digital Logic and Computer Systems University of Florida Electrical & Computer Engineering Dept.

Poche, Natalie Class #: 11198 February 16, 2025

REQUIREMENTS NOT MET

Homework 5 Report: DAD Tutorial

<insert any requirements not met, i.e., problems not solved, if applicable (if not applicable, write "N/A")>

PROBLEMS ENCOUNTERED

<insert a brief summary of all problems encountered>

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THE ABOVE SHOULD BE LIMITED TO THE FIRST PAGE, AND NOTHING ELSE SHOULD BE INCLUDED, WHICH ALSO IMPLIES THAT THIS SENTENCE OF TEXT SHOULD BE REMOVED.

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HOMEWORK EXERCISES

- 1. Complete Exercises in DAD WaveForms Tutorial
 - a. Exercise 1: Simple Circuit using Switches and LEDs

A	В	C
0	0	1
0	1	0
1	0	0
1	1	0

Table 1: Exercise 1 - NOR Gate Truth Table, C = /(A + B)

A(H)	B(H)	C(H)
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

Table 2: Exercise 1 - NOR Gate Voltage Table, C = /(A + B)



Table 3: Exercise 1 - Static I/O Results from NOR Gate

b. Exercise 2: Pattern Generator

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Table 4: Exercise 2 - Results from Pattern Generator Input 0



Table 5: Exercise 2 - Results from Pattern Generator Input 1

c. Exercise 3: Buses

A	В	C
0	0	1
0	1	0
1	0	0
1	1	0

Table 6: Exercise 3 - NOR Gate Truth Table, C = /(A + B)

A(H)	B(H)	C(H)
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

Table 7: Exercise 3 - NOR Gate Voltage Table, C = /(A + B)

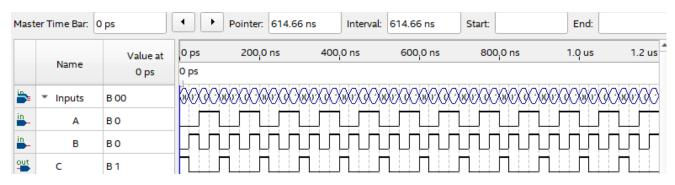


Table 8: Exercise 3 - Quartus Functional Simulation of NOR Gate

d. Logic Analyzer



Table 9: Logic Analyzer for Output 3

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e. Setting Up a Bus



Table 10: Exercise 4 - Pattern Generator in Binary Count and Logic Analyzer with no Clock or Enable



Table 11: Exercise 4 - Pattern Generator in Binary Count and Logic Analyzer with Clock DIO4 High and Enable DIO3 Rising

f. Pattern Generator Bus and Logic Analysis Bus

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Table 12: NOR Gate Truth Table, C = /(A + B)

A(H)	B(H)	C(H)
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

Table 13: NOR Gate Voltage Table, C = /(A + B)

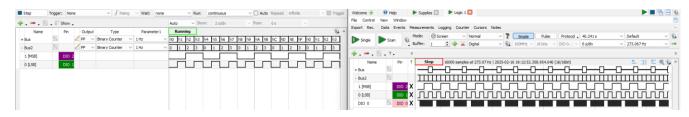


Table 14: Logic Analysis of NOR Gate

g. Kk;l

2. Quartus

a.

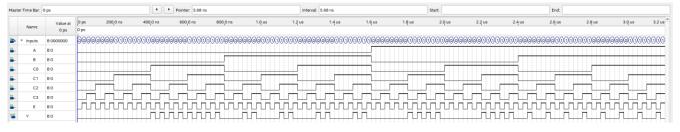


Table 15: Quartus Functional Smulation of MUX

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Revision: 0

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None Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-255-20-4500 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-255-20-4500 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-255-20-4500 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-255-20-4500 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-255-20-4500 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-255-20-4500 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-250 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-250 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-250 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-250 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-250 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004-250 (16/18/01) |

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- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 12025-02-16 20:2004 (16/18/01) |

- But | Pin T Stop | 16000 samples at 273.07 fe | 10000 samples at 273.07 fe | 10

Table 16: WaveForm Logic Analysis of MUX

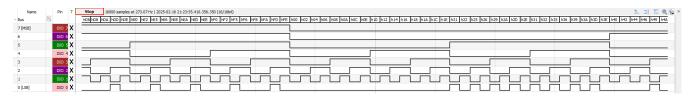


Table 17: Waveform Logic Analysis of MUX

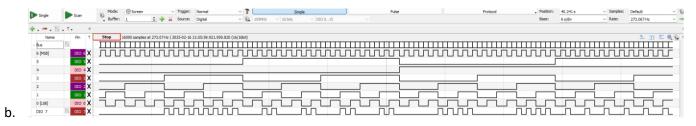


Table 18: MUX Logic Analysis of MUX with specified inputs

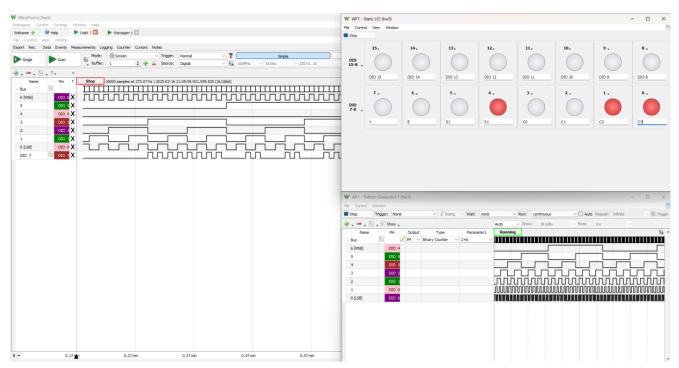


Table 19: MUX Logic Analysis of MUX with More of the Setup