REQUIREMENTS NOT MET

N/A

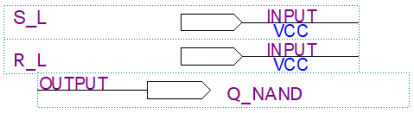
PROBLEMS ENCOUNTERED

N/A

HOMEWORK EXERCISES

1. Use a Quartus Simulation to Show that an S-R latch can be made using two NAND gates.

hw7, Part A
Name: Natalie Poche
Class #: 111938
PI Name: Jaiden Magnan
Description: Make S-R latch with two NAND gates



a.

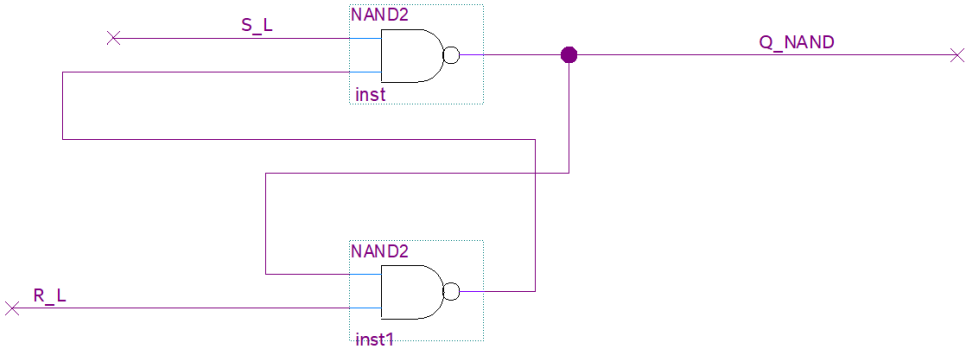


Figure 1: Homework 7 - Part 1: BDF of S-R latch with Two NAND gates

b.

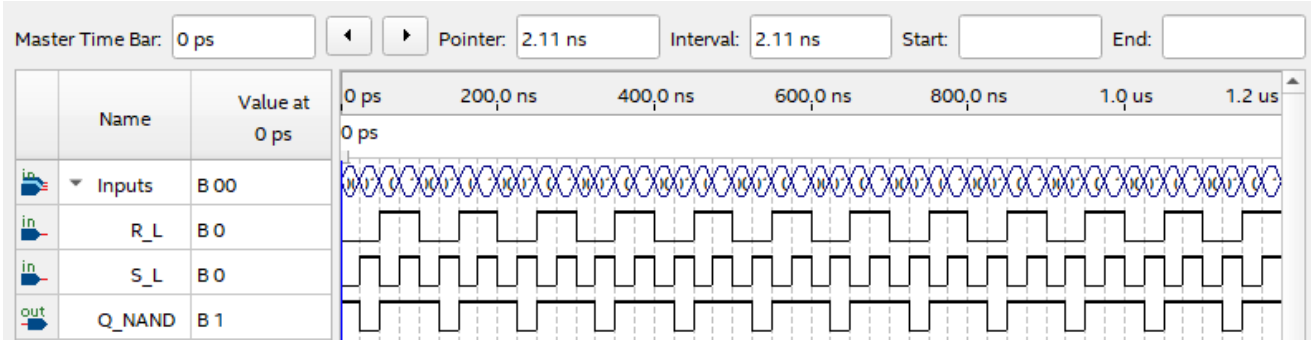
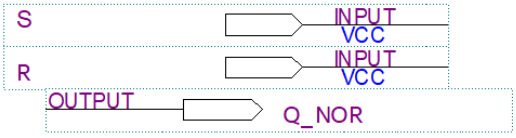


Figure 2: Homework 7 - Part 1: Functional Simulation of S-R latch with two NAND gates

2. Use a Quartus Simulation to Show that an S-R latch can be made using two NOR gates.

hw7, Part B
Name: Natalie Poche
Class #: 11198
PI Name: Jaiden Magnan
Description: S-R latch using 2 NOR gates



a.

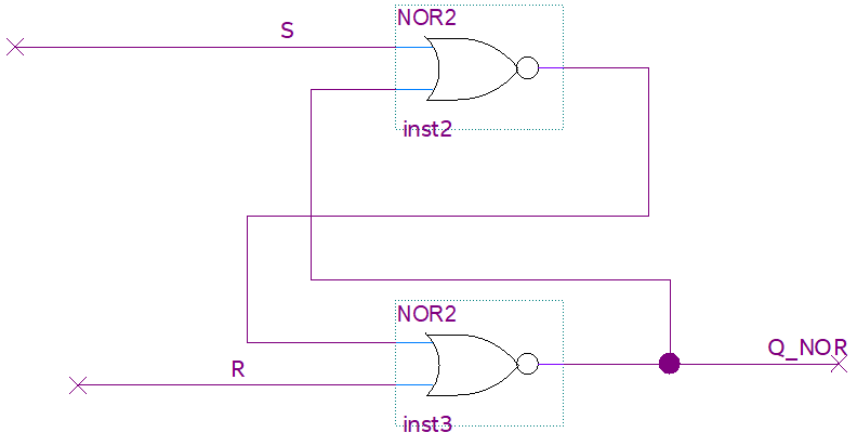


Figure 3: Homework 7 - Part 2: BDF of S-R latch with Two NOR gates

b.

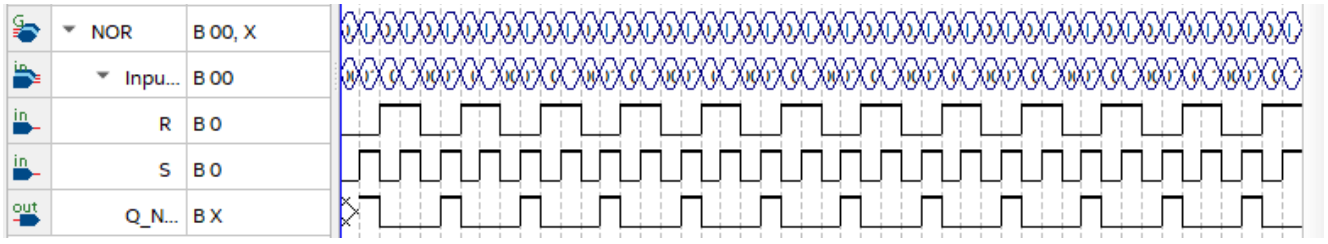
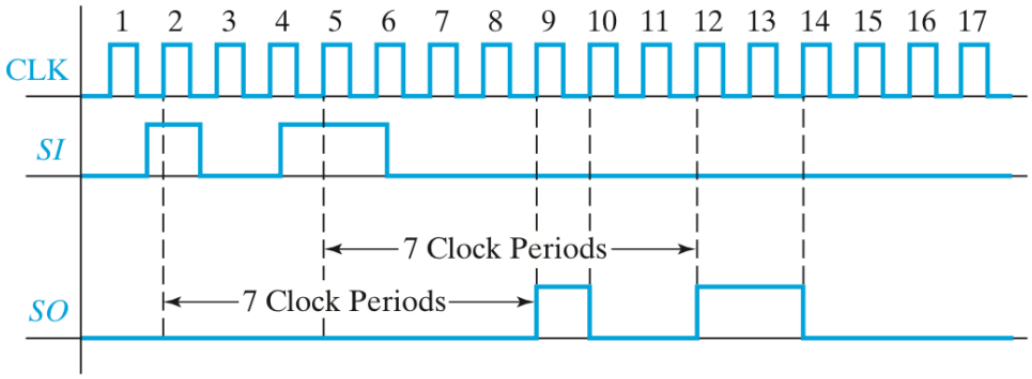


Figure 4: Homework 7 - Part 2: Functional Simulation of S-R latch with Two NOR gates

3. Derive the characteristic equations and excitation tables for each type of flip-flop.

FIGURE 12-9
Typical Timing Diagram for Shift Register of Figure 12-8



D Flip Flop

D	Q^+
0	0
1	1

$Q^+ = D$

D-FF Excitation Table

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

T Flip Flop

T	Q^+
0	Q
1	/Q

$Q^+ = T*/Q + /T*Q$

T-FF Excitation Table

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

SR Flip Flop

R	T	Q^+
0	0	Q
0	1	0
1	0	1

$Q^+ = S + /R*Q$

SR-FF Excitation Table

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK Flip Flop

J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	/Q

$Q^+ = J*/Q + /K*Q$

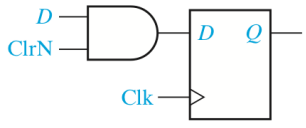
JK-FF Excitation Table

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

4. 7th edition Roth Textbook Problem 11.26

11.26 The ClrN and PreN inputs introduced in Section 11.8 are called asynchronous because they operate independently of the clock (i.e., they are not synchronized with the clock). We can also make flip-flops with synchronous clears or preset inputs.

A D-flip-flop with an active-low synchronous ClrN input may be constructed from a regular D flip-flop as follows.



Fill in the timing diagram. For Q_1, assume a synchronous ClrN as above, and for Q_2, assume an asynchronous ClrN as in Section 11.8. Assume $Q_1 = Q_2 = 0$ at the beginning.