University of Florida **EEL3701C – Digital Logic and Computer Systems** Poche, Natalie Electrical & Computer Engineering Dept. Revision: **X** Class #: 11198

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REQUIREMENTS NOT MET

N/A

PROBLEMS ENCOUNTERED

N/A

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HOMEWORK EXERCISES

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Poche, Natalie

Poche, Natalie

Homework # Report: Homework 10

```
-- Homework 10
-- Name: NaTalie Poche
-- Due: April 1, 2025
-- Description: VMDL Code
Hibrary teee;
use teee.std_logic_1164.a11;
    entity Combangic is port(
                                     Y_L: in std_logic;
                                         T co not T_L; -- Changes initial T_L to be opposite
                                                                                                                   on xi) and (not xi) and (no ((not xi) and (((not xi) and (xi) and (((not xi) and (xi) and (((xi) xi) and ((not xi) and (((xi) xi) and ((not xi) and (((xi) xi) and ((not xi) and (((xi) xi) and ((xi) xi) and ((
```

Figure 1: Homework 10 - VDHL of Code for Combinational Logic Block for Hex to 7-Segment Decoder

X[3..0]

T_L

Revision: 2

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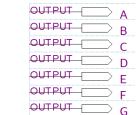
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Homework 10

Name: Natalie Poche

Class #: 11198

Description: combinational logic block with VDHL code for Hex to 7-Segment Decoder



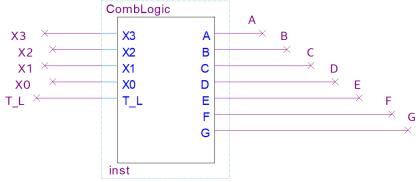


Figure 2: Homework 10 - BDF of Combinational Logic Block for Hex to 7-Segment Decoder

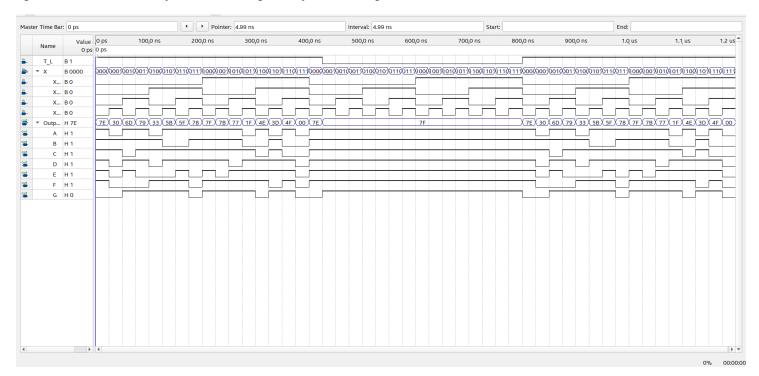


Figure 3: Homework 10 - Functional Simulation of Hex to 7-Segment Decoder