**REQUIREMENTS NOT MET**

N/A

**PROBLEMS ENCOUNTERED**

When switching between devices from MAX V back to MAX X, there were some compilation errors, where I would have to select from “Device | Available Devices” in order to successfully compile when switching back from MAX V.

**HOMEWORK EXERCISES**

<insert copy of homework problem numbers from homework document, as well as an answer directly following each of the questions (if not applicable, write “N/A”); also specify the Roth textbook version number you used; all scans must be clear and legible>

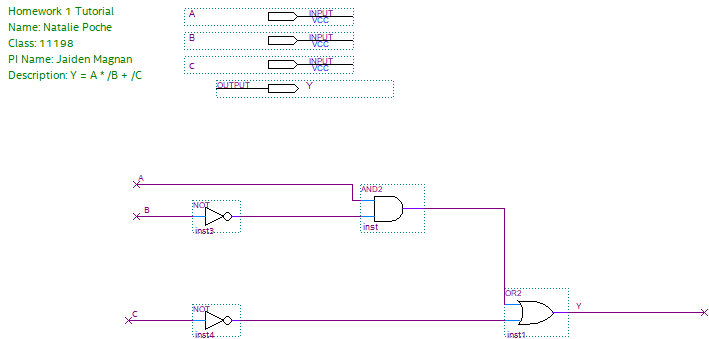
1. Creating a Project In Quartus
   1. A New Project Design Creation
      1. N/A
      2. N/A
      3. N/A
      4. N/A
      5. N/A
      6. N/A
      7. N/A
      8. N/A
   2. Configuring Quartus Window
      1. N/A
      2. N/A
2. Designing
   1. Creating A BDF
      1. N/A
      2. N/A
      3. N/A
   2. Adding Text
      1. N/A
      2. N/A
      3. N/A
      4. N/A
      5. N/A
      6. N/A
      7. N/A
      8. N/A
   3. Component Selection Process and Moving Components
      1. N/A
      2. N/A
      3. N/A
      4. N/A
      5. N/A
      6. N/A
      7. N/A
      8. N/A
      9. N/A
      10. N/A
      11. N/a
      12. N/A
   4. Adding/Deleting Wires
      1. N/A
      2. N/A
      3. N/A
      4. N/A
      5. N/A
      6. N/A
   5. Adding Input and Output Ports
      1. N/A
      2. N/A
      3. N/A
      4. N/A
      5. N/A
      6. N/A
      7. 

Figure : BDF with inputs and outputs

* 1. Full Compilation (for programming your PLD)
     1. N/A
     2. N/A
  2. Functional Compilation (for simulation only)
     1. N/A
     2. N/A

1. Simulating
   1. Creating a VWF (Vector Waveform)
      1. N/A
      2. N/A
   2. Adding Signals
      1. N/A
      2. N/A
      3. N/A
   3. Changing Grid Size and End Table Time
      1. N/A
      2. N/A
   4. Manually Changing VWF
      1. N/A
      2. N/A
      3. N/A
      4. N/A
      5. N/A
   5. Functional and Timing Simulation

|  |  |  |  |
| --- | --- | --- | --- |
| **A\_H** | **B\_L** | **C\_L** | **Y\_H** = A \* /B + /C |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

* + 1. N/A

Figure : Logic Table for Y = A \* /B + /C

|  |  |  |  |
| --- | --- | --- | --- |
| **A\_H** | **B\_L** | **C\_L** | **Y\_H** = A \* /B + /C |
| L | L | L | H |
| L | L | H | L |
| L | H | L | H |
| L | H | H | L |
| H | L | L | H |
| H | L | H | H |
| H | H | L | H |
| H | H | H | L |

Figure : Voltage Table for Y = A \* /B + /C

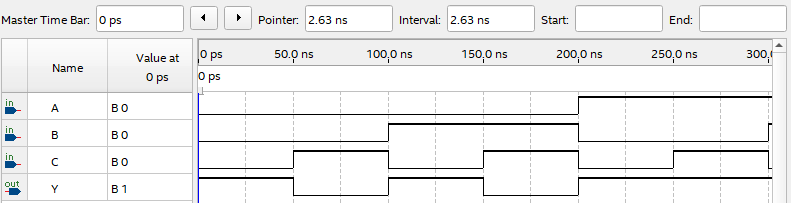
* + 1. 

Figure : Functional Simulation Ungrouped

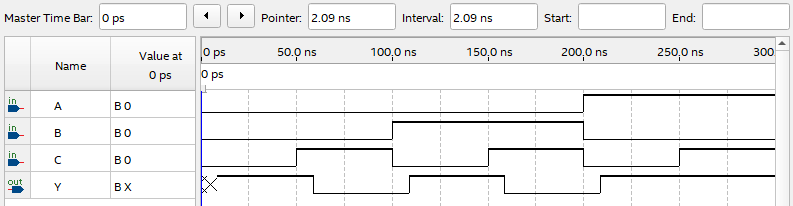
* + 1. N/A
       1. N/A
       2. N/A
       3. N/A
       4. N/A
       5. N/A
       6. 

Figure : Time Simulation Ungrouped

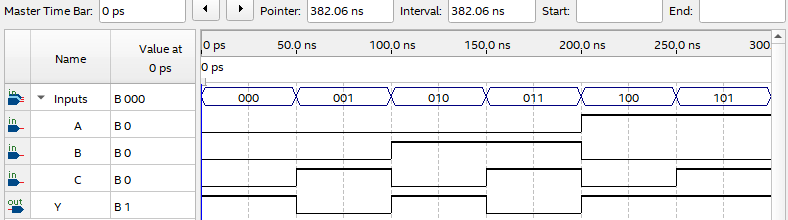
* + 1. N/A
    2. N/A
    3. N/A
    4. N/A
  1. Grouping Signals and Using Count Value and Clock Value
     1. N/A
     2. N/A
     3. N/A
     4. N/A
     5. N/A
     6. 

Figure : Functional Simulation Grouped

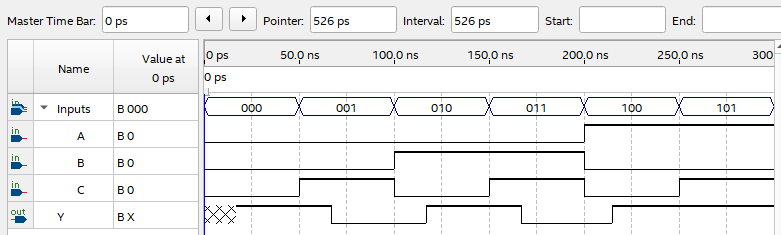
* + 1. 

Figure : Time Simulation Grouped

1. Archiving Your Project
   1. Archiving your project into a qar file
      1. N/A
      2. N/A
   2. Un-archiving (restoring) your project into a qar file
      1. N/A
      2. N/A
      3. N/A