



## 1. Description

### 1.1. Project

Project Name	Inverter
Board Name	NUCLEO-F303RE
Generated with:	STM32CubeMX 6.9.2
Date	11/24/2023

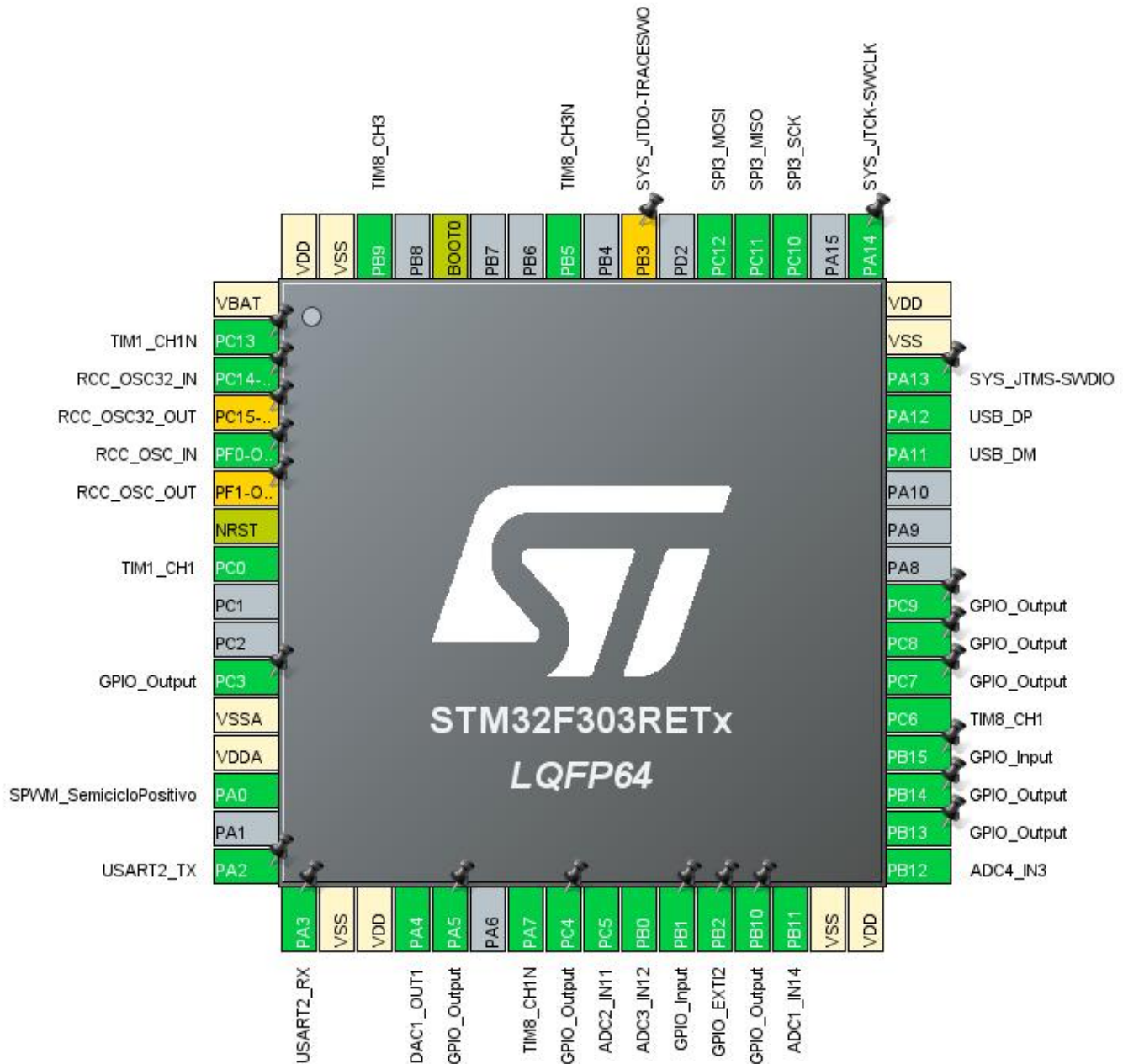
### 1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303RETx
MCU Package	LQFP64
MCU Pin number	64

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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## 2. Pinout Configuration



### 3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	TIM1_CH1N	
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT *	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	TIM1_CH1	
11	PC3 **	I/O	GPIO_Output	
12	VSSA	Power		
13	VDDA	Power		
14	PA0	I/O	TIM2_CH1	SPWM_SemicicloPositivo
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	DAC1_OUT1	
21	PA5 **	I/O	GPIO_Output	
23	PA7	I/O	TIM8_CH1N	
24	PC4 **	I/O	GPIO_Output	
25	PC5	I/O	ADC2_IN11	
26	PB0	I/O	ADC3_IN12	
27	PB1 **	I/O	GPIO_Input	
28	PB2	I/O	GPIO_EXTI2	
29	PB10 **	I/O	GPIO_Output	
30	PB11	I/O	ADC1_IN14	
31	VSS	Power		
32	VDD	Power		
33	PB12	I/O	ADC4_IN3	
34	PB13 **	I/O	GPIO_Output	
35	PB14 **	I/O	GPIO_Output	
36	PB15 **	I/O	GPIO_Input	
37	PC6	I/O	TIM8_CH1	
38	PC7 **	I/O	GPIO_Output	
39	PC8 **	I/O	GPIO_Output	
40	PC9 **	I/O	GPIO_Output	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
44	PA11	I/O	USB_DM	
45	PA12	I/O	USB_DP	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
51	PC10	I/O	SPI3_SCK	
52	PC11	I/O	SPI3_MISO	
53	PC12	I/O	SPI3_MOSI	
55	PB3 *	I/O	SYS_JTDO-TRACESWO	
57	PB5	I/O	TIM8_CH3N	
60	BOOT0	Boot		
62	PB9	I/O	TIM8_CH3	
63	VSS	Power		
64	VDD	Power		

\*\* The pin is affected with an I/O function

\* The pin is affected with a peripheral function but no peripheral mode is activated



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	Inverter
Project Folder	C:\Users\Danil\OneDrive\PROYECTOS\C\STM32\Inverter
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.4
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_USART2_UART_Init	USART2
5	MX_USB_DEVICE_Init	USB_DEVICE
6	MX_TIM2_Init	TIM2
7	MX_ADC1_Init	ADC1
8	MX_ADC3_Init	ADC3
9	MX_ADC4_Init	ADC4
10	MX_ADC2_Init	ADC2
11	MX_TIM1_Init	TIM1

Rank	Function Name	Peripheral Instance Name
12	MX_DAC1_Init	DAC1
13	MX_TIM3_Init	TIM3
14	MX_SPI3_Init	SPI3
15	MX_FATFS_Init	FATFS
16	MX_TIM7_Init	TIM7
17	MX_TIM8_Init	TIM8



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303RETx
Datasheet	DS10362_Rev5

### 1.2. Parameter Selection

Temperature	25
Vdd	3.6

### 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

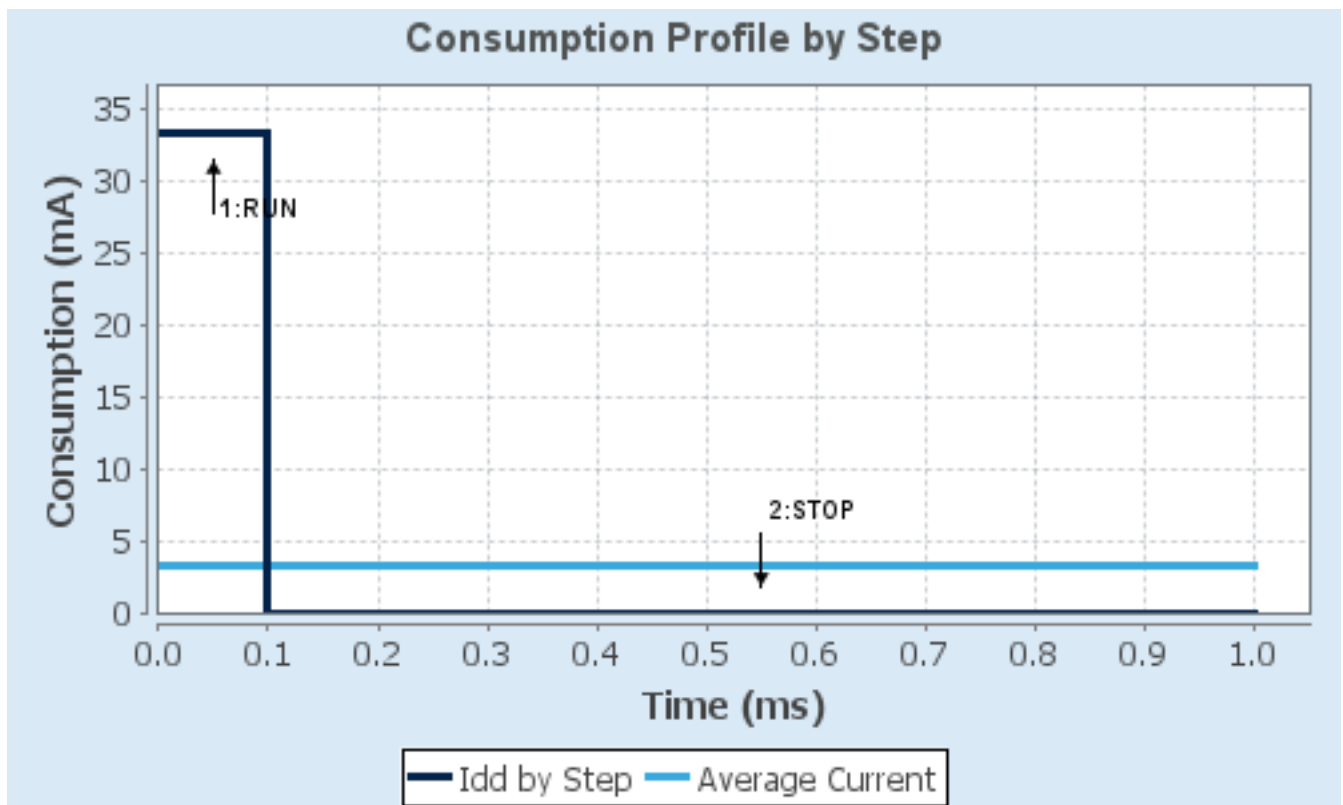
#### 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.6	3.6
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	No Scale	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	72 MHz	0 Hz
<b>Clock Configuration</b>	HSEBYP PLL	Regulator LP
<b>Clock Source Frequency</b>	8 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	33.24 mA	9.8 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	63.0	0.0
<b>Ta Max</b>	99.5	105
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	3.33 mA
Battery Life	1 month, 12 days, 1 hour	Average DMIPS	63.0 DMIPS

#### 1.6. Chart



## 2. Peripherals and Middlewares Configuration

### 2.1. ADC1

**mode: IN14**

#### 2.1.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode Independent mode

##### **ADC\_Settings:**

Clock Prescaler	<b>Synchronous clock mode divided by 1 *</b>
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	<b>Enabled *</b>
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	<b>Enabled *</b>
End Of Conversion Selection	<b>End of sequence of conversion *</b>
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

##### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
SequencerNbRanks	1
<u>Rank</u>	1
Channel	Channel 14
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

##### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions **Disable \***

##### **Analog Watchdog 1:**

Enable Analog WatchDog1 Mode false

##### **Analog Watchdog 2:**

Enable Analog WatchDog2 Mode false

##### **Analog Watchdog 3:**

Enable Analog WatchDog3 Mode false

## 2.2. ADC2

### IN11: IN11 Single-ended

#### 2.2.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode Independent mode

##### **ADC\_Settings:**

Clock Prescaler

**Synchronous clock mode divided by 1 \***

Resolution

ADC 12-bit resolution

Data Alignment

Right alignment

Scan Conversion Mode

Disabled

Continuous Conversion Mode

**Enabled \***

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests

**Enabled \***

End Of Conversion Selection

End of single conversion

Overrun behaviour

Overrun data overwritten

Low Power Auto Wait

Disabled

##### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions

Enable

Number Of Conversion

1

External Trigger Conversion Source

Regular Conversion launched by software

External Trigger Conversion Edge

None

SequencerNbRanks

1

Rank

1

Channel

Channel 11

Sampling Time

1.5 Cycles

Offset Number

No offset

Offset

0

##### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions

**Disable \***

##### **Analog Watchdog 1:**

Enable Analog WatchDog1 Mode

false

##### **Analog Watchdog 2:**

Enable Analog WatchDog2 Mode

false

##### **Analog Watchdog 3:**

Enable Analog WatchDog3 Mode

false

## 2.3. ADC3

### mode: IN12

#### 2.3.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode Independent mode

##### **ADC\_Settings:**

Clock Prescaler

**Synchronous clock mode divided by 1 \***

Resolution

ADC 12-bit resolution

Data Alignment

Right alignment

Scan Conversion Mode

Disabled

Continuous Conversion Mode

**Enabled \***

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests

**Enabled \***

End Of Conversion Selection

End of single conversion

Overrun behaviour

Overrun data overwritten

Low Power Auto Wait

Disabled

##### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions

Enable

Number Of Conversion

1

External Trigger Conversion Source

Regular Conversion launched by software

External Trigger Conversion Edge

None

SequencerNbRanks

1

Rank

1

Channel

Channel 12

Sampling Time

1.5 Cycles

Offset Number

No offset

Offset

0

##### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions

Enable

Number Of Conversions

0

##### **Analog Watchdog 1:**

Enable Analog WatchDog1 Mode

false

##### **Analog Watchdog 2:**

Enable Analog WatchDog2 Mode

false

##### **Analog Watchdog 3:**

Enable Analog WatchDog3 Mode

false

## 2.4. ADC4

### IN3: IN3 Single-ended

#### 2.4.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode Independent mode

##### **ADC\_Settings:**

Clock Prescaler

**Synchronous clock mode divided by 1 \***

Resolution

ADC 12-bit resolution

Data Alignment

Right alignment

Scan Conversion Mode

Disabled

Continuous Conversion Mode

**Enabled \***

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests

**Enabled \***

End Of Conversion Selection

End of single conversion

Overrun behaviour

Overrun data overwritten

Low Power Auto Wait

Disabled

##### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions

Enable

Number Of Conversion

1

External Trigger Conversion Source

Regular Conversion launched by software

External Trigger Conversion Edge

None

SequencerNbRanks

1

Rank

1

Channel

Channel 3

Sampling Time

1.5 Cycles

Offset Number

No offset

Offset

0

##### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions

Enable

Number Of Conversions

0

##### **Analog Watchdog 1:**

Enable Analog WatchDog1 Mode

false

##### **Analog Watchdog 2:**

Enable Analog WatchDog2 Mode

false

##### **Analog Watchdog 3:**

Enable Analog WatchDog3 Mode

false

## 2.5. DAC1

### mode: OUT1 Configuration

#### 2.5.1. Parameter Settings:

##### DAC Out1 Settings:

Output Buffer	Enable
Trigger	<b>Timer 2 Trigger Out event *</b>
Wave generation mode	Disabled

## 2.6. RCC

### High Speed Clock (HSE): BYPASS Clock Source

### Low Speed Clock (LSE) : BYPASS Clock Source

#### 2.6.1. Parameter Settings:

##### System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

##### RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

## 2.7. SPI3

### Mode: Full-Duplex Master

#### 2.7.1. Parameter Settings:

##### Basic Parameters:

Frame Format	Motorola
Data Size	<b>8 Bits *</b>
First Bit	MSB First

##### Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	<b>18.0 MBits/s *</b>
Clock Polarity (CPOL)	Low



Clock Phase (CPHA) 1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

## 2.8. SYS

### Debug: Serial Wire

Timebase Source: SysTick

## 2.9. TIM1

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1 CH1N**

### 2.9.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>720-1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>2000-1 *</b>
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

**Break And Dead Time management - BRK Configuration:**

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

**Break And Dead Time management - BRK2 Configuration:**

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

**Break And Dead Time management - Output Configuration:**

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable

Lock Configuration	Off
Dead Time	<b>255 *</b>
<b>Clear Input:</b>	
Clear Input Source	Disable
<b>PWM Generation Channel 1 and 1N:</b>	
Mode	PWM mode 1
Pulse (16 bits value)	<b>1000-1 *</b>
Output compare preload	Enable
Fast Mode	<b>Enable *</b>
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

## 2.10. TIM2

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

### 2.10.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	<b>3600-1 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

#### **Clear Input:**

Clear Input Source	Disable
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#### **PWM Generation Channel 1:**

Mode	PWM mode 1
Pulse (32 bits value)	<b>1200 *</b>
Output compare preload	<b>Disable *</b>
Fast Mode	Disable
CH Polarity	High

## 2.11. TIM3

**Clock Source : Internal Clock**

### 2.11.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>72 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>10 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	<b>Enable *</b>

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	<b>Update Event *</b>

## 2.12. TIM7

**mode: Activated**

### 2.12.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>300 *</b>
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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## 2.13. TIM8

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1 CH1N**

**Channel2: PWM Generation No Output**

**Channel3: PWM Generation CH3 CH3N**

**Channel4: PWM Generation No Output**

### 2.13.1. Parameter Settings:

### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>1 *</b>
Counter Mode	<b>Center Aligned mode1 *</b>
Counter Period (AutoReload Register - 16 bits value )	<b>800 *</b>
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	<b>Output Compare (OC1REF) *</b>
Trigger Event Selection TRGO2	<b>Output Compare (OC1REF) *</b>

### Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

### Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

### Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	<b>100 *</b>

### Clear Input:

Clear Input Source	Disable
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### PWM Generation Channel 1 and 1N:

Mode	<b>Assymetric PWM1 *</b>
Pulse (16 bits value)	<b>500 *</b>
Output compare preload	<b>Disable *</b>
Fast Mode	<b>Enable *</b>
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

### PWM Generation Channel 2:

Mode	<b>Assymetric PWM1 *</b>
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Pulse (16 bits value)	0
Output compare preload	<b>Disable *</b>
Fast Mode	<b>Enable *</b>
CH Polarity	High
CH Idle State	Reset

#### **PWM Generation Channel 3 and 3N:**

Mode	<b>Assymetric PWM1 *</b>
Pulse (16 bits value)	<b>500 *</b>
Output compare preload	<b>Disable *</b>
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

#### **PWM Generation Channel 4:**

Mode	<b>Assymetric PWM1 *</b>
Pulse (16 bits value)	0
Output compare preload	<b>Disable *</b>
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

## **2.14. USART2**

### **Mode: Asynchronous**

#### 2.14.1. Parameter Settings:

##### **Basic Parameters:**

Baud Rate	38400
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

##### **Advanced Features:**

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable

RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 2.15. USB

### mode: Device (FS)

#### 2.15.1. Parameter Settings:

##### Basic Parameters:

Speed	Full Speed 12MBit/s
Physical interface	Internal Phy

##### Power Parameters:

Low Power	Disabled
Link Power Management	Disabled

## 2.16. FATFS

### mode: User-defined

#### 2.16.1. Set Defines:

##### Version:

FATFS version	R0.11
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##### Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	<b>Enabled *</b>

##### Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Multilingual Latin 1 (OEM)
USE_LFN (Use Long Filename)	<b>Enabled with static working buffer on the BSS *</b>
MAX_LFN (Max Long Filename)	255

LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

#### Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

#### System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
WORD_ACCESS (Platform dependent access option)	Byte access
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
FS_LOCK (Number of files opened simultaneously)	<b>30 *</b>

## 2.17. USB\_DEVICE

### Class For FS IP: Communication Device Class (Virtual Port Com)

#### 2.17.1. Parameter Settings:

##### Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	<b>Disabled *</b>
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

##### Class Parameters:

USB CDC Rx Buffer Size	1024
USB CDC Tx Buffer Size	1024

#### 2.17.2. Device Descriptor:

##### Device Descriptor:

VID (Vendor Identifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

##### Device Descriptor FS:

PID (Product Identifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

**\* User modified value**



## 3. System Configuration

### 3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PB11	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC5	ADC2_IN11	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PB0	ADC3_IN12	Analog mode	No pull-up and no pull-down	n/a	
ADC4	PB12	ADC4_IN3	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PC13	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC0	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPWM_SemicicloPositivo
TIM8	PA7	TIM8_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM8_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
USB	PA11	USB_DM	n/a	n/a	n/a	
	PA12	USB_DP	n/a	n/a	n/a	
Single Mapped Signals	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	
GPIO	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

### 3.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	<b>Very High *</b>
ADC3	DMA2_Channel5	Peripheral To Memory	<b>Very High *</b>
ADC4	DMA2_Channel4	Peripheral To Memory	<b>Very High *</b>
ADC2	DMA2_Channel3	Peripheral To Memory	<b>Very High *</b>
DAC1_CH1	DMA1_Channel3	Memory To Peripheral	Low
TIM2_CH1	DMA1_Channel5	Memory To Peripheral	Low

#### ADC1: DMA1\_Channel1 DMA request Settings:

Mode: Normal  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: **Word \***  
 Memory Data Width: **Word \***

#### ADC3: DMA2\_Channel5 DMA request Settings:

Mode: Normal  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: **Word \***  
 Memory Data Width: **Word \***

#### ADC4: DMA2\_Channel4 DMA request Settings:

Mode: Normal  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: **Word \***  
 Memory Data Width: **Word \***

#### ADC2: DMA2\_Channel3 DMA request Settings:

Mode: Normal

Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: **Word \***  
Memory Data Width: **Word \***

*DAC1\_CH1: DMA1\_Channel3 DMA request Settings:*

Mode: **Circular \***  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: **Word \***  
Memory Data Width: **Word \***

*TIM2\_CH1: DMA1\_Channel5 DMA request Settings:*

Mode: **Circular \***  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Word  
Memory Data Width: Word

### 3.3. NVIC configuration

#### 3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
TIM1 update and TIM16 interrupts	true	0	0
TIM3 global interrupt	true	0	7
TIM7 global interrupt	true	0	0
DMA2 channel3 global interrupt	true	0	0
DMA2 channel4 global interrupt	true	0	0
DMA2 channel5 global interrupt	true	0	0
USB low priority interrupt remap	true	0	0
PVD interrupt through EXTI line 16		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
EXTI line2 and Touch Sense controller interrupts		unused	
ADC1 and ADC2 interrupts		unused	
USB high priority or CAN_TX interrupts		unused	
USB low priority or CAN_RX0 interrupts		unused	
TIM1 break and TIM15 interrupts		unused	
TIM1 trigger, commutation and TIM17 interrupts		unused	
TIM1 capture compare interrupt		unused	
TIM2 global interrupt		unused	
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26		unused	
TIM8 break global interrupt		unused	
TIM8 update interrupt		unused	
TIM8 trigger and commutation interrupt		unused	
TIM8 capture compare interrupt		unused	
ADC3 global interrupt		unused	

Interrupt Table	Enable	Preenmption Priority	SubPriority
SPI3 global interrupt		unused	
TIM6 global interrupt and DAC1 underrun interrupt		unused	
ADC4 interrupt		unused	
USB high priority interrupt remap		unused	
Floating point unit interrupt		unused	

### 3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
TIM1 update and TIM16 interrupts	false	true	true
TIM3 global interrupt	false	true	true
TIM7 global interrupt	false	true	true
DMA2 channel3 global interrupt	false	true	true
DMA2 channel4 global interrupt	false	true	true
DMA2 channel5 global interrupt	false	true	true
USB low priority interrupt remap	false	true	true

\* User modified value

## 4. System Views

### 4.1. Category view

#### 4.1.1. Current

##### Middleware

FATFS 

USB\_DEVICE 

##### System Core

##### Analog

##### Timers

##### Connectivity

##### Multimedia

##### Computing

DMA 

ADC1 

TIM1 

SPI3 

GPIO 

ADC2 

TIM2 

USART2 

IVIC 

ADC3 

TIM3 

USB 

RCC 

ADC4 

TIM7 

SYS 

DAC1 

TIM8 

## 5. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32f3_bsdل.zip">https://www.st.com/resource/en/bsdl_model/stm32f3_bsdل.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32f3-svd.zip">https://www.st.com/resource/en/svd/stm32f3-svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/brstm32f3.pdf">https://www.st.com/resource/en/brochure/brstm32f3.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf">https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstmcsuite.pdf">https://www.st.com/resource/en/flyer/flstmcsuite.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flpowerstbd.pdf">https://www.st.com/resource/en/flyer/flpowerstbd.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/fldpstpfcl1120.pdf">https://www.st.com/resource/en/flyer/fldpstpfcl1120.pdf</a>
Product Certifications	<a href="https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf">https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf</a>
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- Application Notes [https://www.st.com/resource/en/application\\_note/an4908-stm32-usart-automatic-baud-rate-detection-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4908-stm32-usart-automatic-baud-rate-detection-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf)
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- Application Notes [https://www.st.com/resource/en/application\\_note/an5036-thermal-management-guidelines-for-stm32-applications-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an5036-thermal-management-guidelines-for-stm32-applications-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an5105-getting-started-with-touch-sensing-control-on-stm32-microcontrollers-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an5105-getting-started-with-touch-sensing-control-on-stm32-microcontrollers-stmicroelectronics.pdf)
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