Simulink Design Verifier Report

example_02

16-Jan-2016 16:50:38

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Chapter 1. Summary

Analysis Information

Model: example_02
Mode: PropertyProving
Status: Stopped by user
Analysis Time: 40s

Objectives Status

Number of Objectives: **2**
Objectives Falsified with Counterexamples: 1
Objectives Undecided when the Analysis was Stopped: 1

Chapter 2. Analysis Information

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Model Information

File: example_02
Version: 1.20
Time Stamp: Sat Jan 16 16:40:05 2016

Analysis Options

Mode:	PropertyProving
Proving Strategy:	Prove
Proof Assumptions:	UseLocalSettings
Test Objectives:	UseLocalSettings
Assertions:	UseLocalSettings
Maximum Analysis Time:	3000s
Block Replacement:	off
Parameters Analysis:	off
Save Data:	on
Save Harness:	off
Save Report:	off

Approximations

Simulink Design Verifier performed the following approximations during analysis. These can impact the precision of the results generated by Simulink Design Verifier. Please see the product documentation for further details.

#	Type	Description
1	Rational approximation	The model includes floating-point arithmetic. Simulink Design Verifier approximates floating-point arithmetic with rational number arithmetic.

Chapter 3. Proof Objectives Status

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Objectives Falsified with Counterexamples

#	Type	Model Item	Description	Analysis Time (sec)	Counterexample
2	Proof objective	Verification Subsystem/Proof Objective1	Objective: T	19	1

Objectives Undecided when the Analysis was Stopped

Simulink Design Verifier was not able to process these objectives with the current options.

#	Type	Model Item	Description	Analysis Time (sec)	Counterexample
1	Proof	Verification Subsystem/Proof	Objective:	-1	n/a

#	Type	Model Item	Description	Analysis Time (sec)	Counterexample
	objective	[Objective](#)	T		

Chapter 4. Properties

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Verification Subsystem/Proof Objective

Summary

Model Item: [Verification Subsystem/Proof Objective](#)
Property: Objective: T
Status: Undecided

Verification Subsystem/Proof Objective1

Summary

Model Item: [Verification Subsystem/Proof Objective1](#)
Property: Objective: T
Status: Falsified

Counterexample

Time	0
Step	1
In1	0
In2	1
In3	1
In4	1
In5	1
In6	1
In7	1
In8	1
In9	1
In10	1
In11	1