Table 1: Additional swap gates and circuit depth, n = 5

benchmark	g	d	layout	s basic	s sabre	s look	swap (%)	d basic	d swap	d look	d (%)
ghz	7	7	full_10_2	0	0	0	nan	7	7	7	0
ghz	7	7	full_7_3	0	0	0	nan	7	7	7	0
ghz	7	7	ring_10_2	0	3	9	200	7	10	8	-20
ghz	7	7	ring_7_3	0	0	9	nan	7	7	8	14.29
ghz	7	7	grid_9_3	6	3	6	100	13	10	8	-20
ghz	7	7	grid_4_5	3	0	9	nan	10	7	8	14.29
ghz	7	7	line_5_4	0	9	18	100	7	13	9	-30.77
ghz	7	7	t_horizontal_5_4	9	3	6	100	16	10	9	-10
ghz	7	7	t_vertical_5_4	9	0	6	nan	16	7	9	28.57
ghz	7	7	ring_5_4	0	6	9	50	7	8	8	0
dj	36	11	full_10_2	0	0	0	nan	11	11	11	0
dj	36	11	full_7_3	0	0	0	nan	11	11	11	0
dj	36	11	ring_10_2	36	3	3	0	40	17	12	-29.41
dj	36	11	ring_7_3	24	3	3	0	30	14	12	-14.29
dj	36	11	grid_9_3	9	3	0	-100	21	17	11	-35.29
dj	36	11	grid_4_5	21	3	3	0	37	14	12	-14.29
dj	36	11	line_5_4	36	6	6	0	40	17	14	-17.65
dj	36	11	t_horizontal_5_4	24	3	3	0	37	16	12	-25
dj	36	11	t_vertical_5_4	24	3	3	0	37	17	12	-29.41
dj	36	11	ring_5_4	9	3	3	0	24	14	12	-14.29
graphstate	50	22	full_10_2	0	3	0	-100	22	22	22	0
graphstate	50	22	full_7_3	0	6	0	-100	22	25	22	-12
graphstate	50	22	ring_10_2	12	6	9	50	32	25	20	-20
graphstate	50	22	ring_7_3	18	6	12	100	38	25	21	-16
graphstate	50	22	grid_9_3	15	3	6	100	37	32	20	-37.5
graphstate	50	22	grid_4_5	18	3	9	200	41	25	20	-20
graphstate	50	22	line_5_4	12	9	12	33.33	32	25	21	-16
graphstate	50	22	t_horizontal_5_4	12	6	9	50	35	25	20	-20
graphstate	50	22	t_vertical_5_4	12	6	9	50	35	22	20	-9.09
graphstate	50	22	ring_5_4	12	6	12	100	33	25	25	0
qft	71	38	full_10_2	0	0	0	nan	38	38	38	0
qft	71	38	full_7_3	0	0	0	nan	38	38	38	0
qft	71	38	ring_10_2	72	15	24	60	92	60	42	-30
qft	71	38	ring_7_3	51	18	24	33.33	77	59	42	-28.81
qft	71	38	grid_9_3	39	12	21	75	74	53	41	-22.64
qft	71	38	grid_4_5	36	15	27	80	82	54	52	-3.7
qft	71	38	line_5_4	72	24	24	0	92	57	42	-26.32
qft	71	38	t_horizontal_5_4	48	15	24	60	82	60	42	-30
qft	71	38	t_vertical_5_4	48	15	24	60	82	60	42	-30
qft	71	38	ring_5_4	27	18	18	0	65	57	43	-24.56
wstate	73	45	full_10_2	0	0	0	nan	45	45	45	0
wstate	73	45	full_7_3	0	0	0	nan	45	45	45	0
wstate	73	45	ring_10_2	0	0	9	nan	45	45	40	-11.11
wstate	73	45	ring_7_3	0	0	9	nan	45	45	40	-11.11
wstate	73	45	grid_9_3	18	0	12	nan	54	45	41	-8.89
wstate	73	45	grid_4_5	12	0	9	nan	51	45	40	-11.11
wstate	73	45	line_5_4	0	0	15	nan	45	45	33	-26.67
wstate	73	45	t_horizontal_5_4	18	0	6	nan	58	45	39	-13.33
wstate	73	45	t_vertical_5_4	18	0	6	nan	58	45	39	-13.33
wstate	73	45	ring_5_4	nan	nan	9	nan	nan	nan	39	nan
qftentangled	78	42	full_10_2	0	0	0	nan	42	42	42	0
qftentangled	78	42	full_7_3	0	6	0	-100	42	63	42	-33.33
qftentangled	78	42	ring_10_2	72	21	30	42.86	96	75	49	-34.67
qftentangled	78	42	ring_7_3	51	21	30	42.86	81	75	49	-34.67
qftentangled	78	42	grid_9_3	45	21	27	28.57	87	76	45	-40.79
qftentangled	78	42	grid_4_5	36	18	15	-16.67	78	57	45	-21.05
qftentangled	78	42	line_5_4	72	24	36	50	96	73	50	-31.51
qftentangled	78	42	t_horizontal_5_4	60	24	33	37.5	90	73	48	-34.25
qftentangled	78	42	t_vertical_5_4	60	21	33	57.14	90	75	48	-36
qftentangled	78	42	ring_5_4	27	21	30	42.86	69	76	49	-35.53
vqe	83	21	full_10_2	0	0	0	nan	21	21	21	0

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Table 1: Additional swap gates and circuit depth, n = 5

benchmark	g	d	layout	s basic	s sabre	s look	swap (%)	d basic	d swap	d look	d (%)
vqe	83	21	full_7_3	0	0	0	nan	21	21	21	0
vqe	83	21	ring_10_2	0	0	15	nan	21	21	29	38.1
vqe	83	21	ring_7_3	0	0	15	nan	21	21	29	38.1
vqe	83	21	grid_9_3	15	0	12	nan	35	21	27	28.57
vqe	83	21	grid_4_5	18	0	15	nan	39	21	29	38.1
vqe	83	21	line_5_4	0	0	15	nan	21	21	24	14.29
vqe	83	21	t_horizontal_5_4	12	0	12	nan	33	21	25	19.05
vqe	83	21	t_vertical_5_4	12	0	12	nan	33	21	25	19.05
vqe	83	21	ring_5_4	0	0	15	nan	21	21	29	38.1
qaoa	95	31	full_10_2	0	3	0	-100	31	42	31	-26.19
qaoa	95	31	full_7_3	0	0	0	nan	31	31	31	0
qaoa	95	31	ring_10_2	48	12	27	125	106	47	45	-4.26
qaoa	95	31	ring_7_3	24	9	27	200	54	58	45	-22.41
qaoa	95	31	grid_9_3	9	9	21	133.33	37	48	48	0
qaoa	95	31	grid_4_5	18	6	27	350	59	50	45	-10
qaoa	95	31	line_5_4	48	12	18	50	106	42	39	-7.14
qaoa	95	31	t_horizontal_5_4	33	9	24	166.67	100	48	45	-6.25
qaoa	95	31	t_vertical_5_4	33	9	24	166.67	100	48	45	-6.25
qaoa	95	31	ring_5_4	18	9	27	200	53	39	48	23.08
realamprandom	130	37	full_10_2	0	0	0	nan	37	37	37	0
realamprandom	130	37	full_7_3	0	0	0	nan	37	37	37	0
realamprandom	130	37	ring_10_2	180	51	60	17.65	206	109	66	-39.45
realamprandom	130	37	ring_7_3	120	51	60	17.65	129	109	66	-39.45
realamprandom	130	37	grid_9_3	96	24	42	75	145	89	64	-28.09
realamprandom	130	37	grid_4_5	81	42	48	14.29	160	97	59	-39.18
realamprandom	130	37	line_5_4	180	72	93	29.17	206	128	59	-53.91
realamprandom	130	37	t_horizontal_5_4	117	51	60	17.65	185	106	66	-37.74
realamprandom	130	37	t_vertical_5_4	117	51	60	17.65	185	106	66	-37.74
twolocalrandom	130	37	full_10_2	0	0	0	nan	37	37	37	0
twolocalrandom	130	37	full_7_3	0	18	0	-100	37	81	37	-54.32
twolocalrandom	130	37	ring_10_2	180	51	60	17.65	206	109	66	-39.45
twolocalrandom	130	37	ring_7_3	120	51	60	17.65	129	112	66	-41.07
twolocalrandom	130	37	grid_9_3	96	36	42	16.67	145	93	64	-31.18
twolocalrandom	130	37	grid_4_5	81	42	48	14.29	160	101	59	-41.58
twolocalrandom	130	37	line_5_4	180	72	93	29.17	206	113	59	-47.79
twolocalrandom	130	37	t_horizontal_5_4	117	72	60	-16.67	185	126	66	-47.62
twolocalrandom	130	37	t_vertical_5_4	117	48	60	25	185	107	66	-38.32
su2random	150	41	full_10_2	0	15	0	-100	41	64	41	-35.94
su2random	150	41	full_7_3	0	0	0	nan	41	41	41	0
su2random	150	41	ring_10_2	180	48	60	25	219	110	70	-36.36
su2random	150	41	ring_7_3	120	48	60	25	138	115	70	-39.13
su2random	150	41	grid_9_3	96	24	42	75	155	96	68	-29.17
su2random	150	41	grid_4_5	81	42	48	14.29	174	106	63	-40.57
su2random	150	41	line_5_4	180	69	93	34.78	219	123	63	-48.78
su2random	150	41	t_horizontal_5_4	117	48	60	25	198	115	70	-39.13
su2random	150	41	t_vertical_5_4	117	48	60	25	198	110	70	-36.36
qnn	154	58	full_10_2	0	39	0	-100	58	133	58	-56.39
qnn	154	58	full_7_3	0	0	0	nan	58	58	58	0
qnn	154	58	ring_10_2	120	39	66	69.23	172	122	84	-31.15
qnn	154	58	ring_7_3	93	36	66	83.33	122	122	84	-31.15
qnn	154	58	grid_9_3	63	30	48	60	132	97	78	-19.59
qnn	154	58	grid_4_5	54	30	54	80	151	103	80	-22.33
qnn	154	58	line_5_4	120	48	84	75	172	127	80	-37.01
qnn	154	58	t_horizontal_5_4	81	48	66	37.5	172	127	84	-33.86
qnn	154	58	t_vertical_5_4	81	45	66	46.67	172	133	84	-36.84
qnn	154	58	ring_5_4	48	36	66	83.33	95	122	84	-31.15
portfolioqaoa	195	72	full_10_2	0	0	0	nan	72	72	72	0
portfolioqaoa	195	72	full_7_3	0	21	0	-100	72	135	72	-46.67
portfolioqaoa	195	72	ring_10_2	180	66	87	31.82	255	166	110	-33.73
portfolioqaoa	195	72	ring_7_3	120	51	87	70.59	157	164	110	-32.93
portfolioqaoa	195	72	grid_9_3	96	39	69	76.92	199	141	121	-14.18

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Table 1: Additional swap gates and circuit depth, n = 5

benchmark	g	d	layout	s basic	s sabre	s look	swap (%)	d basic	d swap	d look	d (%)
portfolioqaoa	195	72	grid_4_5	81	42	69	64.29	220	138	104	-24.64
portfolioqaoa	195	72	line_5_4	180	66	93	40.91	255	166	90	-45.78
portfolioqaoa	195	72	t_horizontal_5_4	117	60	87	45	252	179	110	-38.55
portfolioqaoa	195	72	t_vertical_5_4	117	66	87	31.82	252	166	110	-33.73
random	223	97	full_10_2	0	12	0	-100	97	126	97	-23.02
random	223	97	full_7_3	0	12	0	-100	97	123	97	-21.14
random	223	97	ring_10_2	63	12	66	450	160	106	121	14.15
random	223	97	ring_7_3	60	12	66	450	157	106	121	14.15
random	223	97	grid_9_3	30	12	27	125	114	106	111	4.72
random	223	97	grid_4_5	39	12	27	125	169	106	111	4.72
random	223	97	line_5_4	63	12	30	150	160	106	99	-6.6
random	223	97	t_horizontal_5_4	36	12	66	450	151	106	121	14.15
random	223	97	t_vertical_5_4	36	12	66	450	151	106	121	14.15
random	223	97	ring_5_4	24	12	66	450	120	106	121	14.15
portfoliovqe	310	107	full_10_2	0	0	0	nan	107	107	107	0
portfoliovqe	310	107	full_7_3	0	21	0	-100	107	161	107	-33.54
portfoliovqe	310	107	ring_10_2	180	51	93	82.35	242	204	125	-38.73
portfoliovqe	310	107	ring_7_3	120	48	93	93.75	179	193	125	-35.23
portfoliovqe	310	107	grid_9_3	96	42	57	35.71	209	181	111	-38.67
portfoliovqe	310	107	grid_4_5	81	39	48	23.08	239	175	115	-34.29
portfoliovqe	310	107	line_5_4	180	69	90	30.43	242	187	126	-32.62
portfoliovqe	310	107	t_horizontal_5_4	117	48	93	93.75	239	193	125	-35.23
portfoliovqe	310	107	t_vertical_5_4	117	57	93	63.16	239	205	125	-39.02

Table 2: Additional swap gates and circuit depth, n = 10

benchmark	g	d	layout	s basic	s sabre	s look	swap (%)	d basic	d swap	d look	d (%)
ghz	12	12	full_10_2	0	6	0	-100	12	15	12	-20
ghz	12	12	full_7_3	0	9	0	-100	12	21	12	-42.86
ghz	12	12	ring_10_2	0	9	36	300	12	21	17	-19.05
ghz	12	12	ring_7_3	0	15	51	240	12	24	25	4.17
ghz	12	12	grid_9_3	12	9	24	166.67	24	21	16	-23.81
ghz	12	12	grid_4_5	6	6	24	300	18	18	16	-11.11
ghz	12	12	line_5_4	0	9	27	200	12	21	15	-28.57
ghz	12	12	t_horizontal_5_4	18	0	21	nan	30	12	17	41.67
ghz	12	12	t_vertical_5_4	27	9	30	233.33	39	18	19	5.56
ghz	12	12	ring_5_4	nan	nan	45	nan	nan	nan	21	nan
dj	79	17	full_10_2	0	3	0	-100	17	20	17	-15
dj	79	17	full_7_3	48	9	9	0	70	26	22	-15.38
dj	79	17	ring_10_2	78	21	24	14.29	64	43	21	-51.16
dj	79	17	ring_7_3	126	15	24	60	79	35	19	-45.71
dj	79	17	grid_9_3	90	21	12	-42.86	82	46	22	-52.17
dj	79	17	grid_4_5	144	21	18	-14.29	88	44	24	-45.45
dj	79	17	line_5_4	216	21	21	0	94	54	30	-44.44
dj	79	17	t_horizontal_5_4	150	21	15	-28.57	88	51	26	-49.02
dj	79	17	t_vertical_5_4	135	30	15	-50	85	49	25	-48.98
dj	79	17	ring_5_4	nan	nan	12	nan	nan	nan	23	nan
graphstate	100	26	full_10_2	0	6	0	-100	23	30	23	-23.33
graphstate	100	26	full_7_3	18	3	12	300	53	24	23	-4.17
graphstate	100	26	ring_10_2	30	12	39	225	45	28	29	3.57
graphstate	100	26	ring_7_3	48	18	39	116.67	63	33	29	-12.12
graphstate	100	26	grid_9_3	42	15	48	220	57	33	26	-21.21
graphstate	100	26	grid_4_5	51	15	36	140	70	35	24	-31.43
graphstate	100	26	line_5_4	72	24	57	137.5	68	36	32	-11.11
graphstate	100	26	t_horizontal_5_4	60	21	36	71.43	66	38	23	-39.47
graphstate	100	26	t_vertical_5_4	63	21	39	85.71	76	34	24	-29.41
graphstate	100	26	ring_5_4	nan	nan	39	nan	nan	nan	30	nan
wstate	163	90	full_10_2	0	0	0	nan	90	90	90	0
wstate	163	90	full_7_3	0	0	0	nan	90	90	90	0
wstate	163	90	ring_10_2	0	12	48	300	90	96	62	-35.42
wstate	163	90	grid_9_3	21	0	27	nan	102	90	46	-48.89
wstate	163	90	grid_4_5	24	15	42	180	96	99	65	-34.34
wstate	163	90	line_5_4	0	0	27	nan	90	90	76	-15.56
wstate	163	90	t_horizontal_5_4	45	0	27	nan	116	90	72	-20
wstate	163	90	t_vertical_5_4	72	0	45	nan	137	90	66	-26.67
wstate	163	90	ring_5_4	0	12	45	275	90	96	55	-42.71
wstate	163	90	ring_7_3	0	6	66	1000	90	96	62	-35.42
vqe	168	26	full_10_2	0	0	0	nan	26	26	26	0
vqe	168	26	full_7_3	0	0	0	nan	26	26	26	0
vqe	168	26	ring_10_2	0	9	66	633.33	26	40	40	0
vqe	168	26	grid_9_3	9	6	54	800	31	35	43	22.86
vqe	168	26	grid_4_5	36	3	45	1400	61	35	33	-5.71
vqe	168	26	line_5_4	0	0	27	nan	26	26	33	26.92
vqe	168	26	t_horizontal_5_4	51	0	33	nan	71	26	37	42.31
vqe	168	26	t_vertical_5_4	66	3	51	1600	73	35	38	8.57
vqe	168	26	ring_5_4	0	15	57	280	26	38	35	-7.89
vqe	168	26	ring_7_3	0	0	84	nan	26	26	43	65.38
qaoa	190	34	grid_9_3	63	12	78	550	145	56	49	-12.5
qaoa	190	34	grid_4_5	105	21	33	57.14	174	59	38	-35.59
qaoa	190	34	line_5_4	168	30	75	150	228	53	44	-16.98
qaoa	190	34	t_horizontal_5_4	129	21	78	271.43	206	50	50	0
qaoa	190	34	t_vertical_5_4	114	27	81	200	196	82	56	-31.71
qaoa	190	34	full_10_2	0	6	0	-100	34	47	34	-27.66
qaoa	190	34	full_7_3	48	9	15	66.67	138	48	42	-12.5
qaoa	190	34	ring_10_2	120	24	60	150	154	42	48	14.29
qaoa	190	34	ring_7_3	81	18	75	316.67	158	64	52	-18.75
qaoa	190	34	ring_5_4	117	12	72	500	191	56	56	0
qft	270	78	full_10_2	0	18	0	-100	78	133	78	-41.35

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Table 2: Additional swap gates and circuit depth, n = 10

benchmark	g	d	layout	s basic	s sabre	s look	swap (%)	d basic	d swap	d look	d (%)
qft	270	78	full_7_3	168	75	150	100	236	181	140	-22.65
qft	270	78	ring_10_2	330	141	165	17.02	233	205	103	-49.76
qft	270	78	ring_7_3	540	120	159	32.5	319	204	116	-43.14
qft	270	78	grid_9_3	279	96	180	87.5	288	211	120	-43.13
qft	270	78	grid_4_5	507	108	195	80.56	335	176	130	-26.14
qft	270	78	line_5_4	780	168	195	16.07	342	181	106	-41.44
qft	270	78	t_horizontal_5_4	486	162	195	20.37	331	198	106	-46.46
qft	270	78	t_vertical_5_4	498	144	195	35.42	273	187	106	-43.32
qftentangled	282	82	full_10_2	0	18	0	-100	82	156	82	-47.44
qftentangled	282	82	full_7_3	168	45	150	233.33	240	176	144	-18.18
qftentangled	282	82	ring_10_2	330	147	165	12.24	237	239	107	-55.23
qftentangled	282	82	ring_7_3	540	129	150	16.28	323	244	115	-52.87
qftentangled	282	82	grid_9_3	282	99	198	100	288	177	135	-23.73
qftentangled	282	82	grid_4_5	414	108	180	66.67	285	213	122	-42.72
qftentangled	282	82	line_5_4	780	195	195	0	346	217	110	-49.31
qftentangled	282	82	t_horizontal_5_4	510	156	195	25	313	225	110	-51.11
qftentangled	282	82	t_vertical_5_4	510	153	195	27.45	309	228	110	-51.75
qftentangled	282	82	ring_5_4	336	153	195	27.45	262	256	137	-46.48
realamprandom	335	57	full_10_2	0	105	0	-100	57	213	57	-73.24
realamprandom	335	57	full_7_3	471	99	141	42.42	632	223	130	-41.7
realamprandom	335	57	ring_10_2	885	399	516	29.32	522	351	215	-38.75
realamprandom	335	57	grid_9_3	690	231	321	38.96	591	248	151	-39.11
realamprandom	335	57	grid_4_5	1323	258	375	45.35	786	246	138	-43.9
realamprandom	335	57	line_5_4	2160	369	396	7.32	876	278	112	-59.71
realamprandom	335	57	t_horizontal_5_4	1614	363	414	14.05	840	263	143	-45.63
realamprandom	335	57	t_vertical_5_4	1515	378	447	18.25	835	243	154	-36.63
realamprandom	335	57	ring_7_3	1299	339	465	37.17	799	323	171	-47.06
twolocalrandom	335	57	full_10_2	0	81	0	-100	57	196	57	-70.92
twolocalrandom	335	57	full_7_3	471	162	141	-12.96	632	235	130	-44.68
twolocalrandom	335	57	ring_10_2	885	405	516	27.41	522	402	215	-46.52
twolocalrandom	335	57	grid_9_3	690	273	321	17.58	591	299	151	-49.5
twolocalrandom	335	57	grid_4_5	1323	258	375	45.35	786	254	138	-45.67
twolocalrandom	335	57	line_5_4	2160	360	396	10	876	268	112	-58.21
twolocalrandom	335	57	t_horizontal_5_4	1614	366	414	13.11	840	265	143	-46.04
twolocalrandom	335	57	t_vertical_5_4	1515	423	447	5.67	835	304	154	-49.34
twolocalrandom	335	57	ring_7_3	1299	417	465	11.51	799	370	171	-53.78
su2random	375	61	full_10_2	0	99	0	-100	61	236	61	-74.15
su2random	375	61	full_7_3	471	174	141	-18.97	657	292	135	-53.77
su2random	375	61	ring_10_2	885	402	537	33.58	543	381	224	-41.21
su2random	375	61	grid_9_3	690	273	321	17.58	619	310	157	-49.35
su2random	375	61	grid_4_5	1323	261	375	43.68	815	267	142	-46.82
su2random	375	61	line_5_4	2160	360	396	10	904	291	116	-60.14
su2random	375	61	t_horizontal_5_4	1614	372	414	11.29	868	292	147	-49.66
su2random	375	61	t_vertical_5_4	1515	384	447	16.41	863	310	160	-48.39
qnn	459	108	full_10_2	0	90	0	-100	108	310	108	-65.16
qnn	459	108	full_7_3	294	180	249	38.33	531	338	214	-36.69
qnn	459	108	ring_10_2	663	288	432	50	440	360	232	-35.56
qnn	459	108	grid_9_3	456	180	240	33.33	537	275	174	-36.73
qnn	459	108	grid_4_5	876	186	390	109.68	636	291	220	-24.4
qnn	459	108	line_5_4	1440	249	327	31.33	657	258	155	-39.92
qnn	459	108	t_horizontal_5_4	1056	249	402	61.45	662	258	194	-24.81
qnn	459	108	t_vertical_5_4	1002	258	423	63.95	662	304	204	-32.89
portfolioqaoa	615	132	full_10_2	0	111	0	-100	132	426	132	-69.01
portfolioqaoa	615	132	full_7_3	471	156	231	48.08	845	478	239	-50
portfolioqaoa	615	132	ring_10_2	885	387	594	53.49	606	496	292	-41.13
portfolioqaoa	615	132	grid_9_3	690	249	384	54.22	803	384	248	-35.42
portfolioqaoa	615	132	grid_4_5	1323	261	450	72.41	956	356	262	-26.4
portfolioqaoa	615	132	line_5_4	2160	360	408	13.33	985	380	176	-53.68
portfolioqaoa	615	132	t_horizontal_5_4	1614	366	489	33.61	979	367	238	-35.15
portfolioqaoa	615	132	t_vertical_5_4	1515	396	504	27.27	976	462	255	-44.81
random	646	155	full_10_2	0	93	0	-100	155	320	155	-51.56

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Table 2: Additional swap gates and circuit depth, n = 10

benchmark	g	d	layout	s basic	s sabre	s look	swap (%)	d basic	d swap	d look	d (%)
random	646	155	full_7_3	159	111	132	18.92	419	348	179	-48.56
random	646	155	ring_10_2	402	237	381	60.76	493	375	244	-34.93
random	646	155	grid_9_3	285	171	225	31.58	455	312	185	-40.71
random	646	155	grid_4_5	477	186	375	101.61	643	325	222	-31.69
random	646	155	line_5_4	582	312	435	39.42	708	342	225	-34.21
random	646	155	t_horizontal_5_4	522	273	402	47.25	660	419	231	-44.87
random	646	155	t_vertical_5_4	525	246	381	54.88	710	351	228	-35.04
portfoliovqe	1145	217	grid_9_3	690	222	387	74.32	951	479	284	-40.71
portfoliovqe	1145	217	grid_4_5	1323	261	342	31.03	994	465	265	-43.01
portfoliovqe	1145	217	line_5_4	2160	360	408	13.33	1007	402	255	-36.57
portfoliovqe	1145	217	t_horizontal_5_4	1614	366	441	20.49	1001	444	276	-37.84
portfoliovqe	1145	217	t_vertical_5_4	1515	396	507	28.03	997	536	282	-47.39
portfoliovqe	1145	217	full_10_2	0	15	0	-100	217	288	217	-24.65
portfoliovqe	1145	217	full_7_3	471	105	255	142.86	878	450	308	-31.56
portfoliovqe	1145	217	ring_10_2	885	411	636	54.74	636	588	298	-49.32

Table 3: Additional swap gates and circuit depth, n = 15

benchmark	g	d	layout	s basic	s sabre	s look	swap (%)	d basic	d swap	d look	d (%)
ghz	17	17	full_10_2	0	6	0	-100	17	20	17	-15
ghz	17	17	full_7_3	0	6	0	-100	17	20	17	-15
ghz	17	17	ring_10_2	0	21	111	428.57	17	26	40	53.85
ghz	17	17	grid_9_3	18	9	42	366.67	35	20	25	25
ghz	17	17	grid_4_5	12	18	33	83.33	29	32	25	-21.88
ghz	17	17	line_5_4	0	12	42	250	17	23	20	-13.04
ghz	17	17	t_horizontal_5_4	27	39	39	0	44	53	28	-47.17
ghz	17	17	t_vertical_5_4	45	51	54	5.88	62	59	29	-50.85
ghz	17	17	ring_5_4	0	27	51	88.89	17	41	30	-26.83
ghz	17	17	ring_7_3	0	18	84	366.67	17	32	28	-12.5
dj	118	22	full_10_2	66	9	9	0	95	33	29	-12.12
dj	118	22	full_7_3	96	9	15	66.67	116	36	30	-16.67
dj	118	22	ring_10_2	336	33	60	81.82	122	71	28	-60.56
dj	118	22	grid_9_3	234	48	24	-50	122	67	34	-49.25
dj	118	22	grid_4_5	324	45	27	-40	128	75	38	-49.33
dj	118	22	line_5_4	546	66	36	-45.45	146	102	45	-55.88
dj	118	22	t_horizontal_5_4	384	42	27	-35.71	137	65	40	-38.46
dj	118	22	t_vertical_5_4	318	48	27	-43.75	131	69	38	-44.93
dj	118	22	ring_5_4	153	36	27	-25	113	71	33	-53.52
dj	118	22	ring_7_3	168	39	42	7.69	116	66	29	-56.06
graphstate	150	29	full_10_2	30	6	24	300	51	40	34	-15
graphstate	150	29	full_7_3	36	9	27	200	67	35	32	-8.57
graphstate	150	29	ring_10_2	111	27	108	300	84	32	31	-3.12
graphstate	150	29	grid_9_3	108	30	87	190	86	38	33	-13.16
graphstate	150	29	grid_4_5	147	24	111	362.5	94	31	38	22.58
graphstate	150	29	line_5_4	186	36	138	283.33	95	33	49	48.48
graphstate	150	29	t_horizontal_5_4	147	42	147	250	96	37	45	21.62
graphstate	150	29	t_vertical_5_4	150	30	138	360	107	35	41	17.14
graphstate	150	29	ring_5_4	78	18	102	466.67	72	38	32	-15.79
graphstate	150	29	ring_7_3	84	24	96	300	85	43	35	-18.6
vqe	253	31	full_10_2	0	6	0	-100	31	41	31	-24.39
vqe	253	31	ring_10_2	0	33	192	481.82	31	63	59	-6.35
vqe	253	31	grid_9_3	48	9	66	633.33	60	45	47	4.44
vqe	253	31	grid_4_5	48	12	78	550	75	60	49	-18.33
vqe	253	31	line_5_4	0	69	42	-39.13	31	83	43	-48.19
vqe	253	31	t_horizontal_5_4	63	6	54	800	79	34	47	38.24
vqe	253	31	t_vertical_5_4	150	12	99	725	94	54	48	-11.11
vqe	253	31	ring_7_3	0	24	138	475	31	63	53	-15.87
vqe	253	31	full_7_3	0	12	0	-100	31	56	31	-44.64
vqe	253	31	ring_5_4	0	39	63	61.54	31	76	44	-42.11
wstate	253	135	full_10_2	0	12	0	-100	135	141	135	-4.26
wstate	253	135	ring_10_2	0	15	177	1080	135	138	78	-43.48
wstate	253	135	grid_9_3	57	18	72	300	156	147	107	-27.21
wstate	253	135	grid_4_5	39	3	57	1800	147	138	102	-26.09
wstate	253	135	line_5_4	0	0	42	nan	135	135	121	-10.37
wstate	253	135	t_horizontal_5_4	63	21	45	114.29	166	141	111	-21.28
wstate	253	135	t_vertical_5_4	126	45	84	86.67	200	153	97	-36.6
wstate	253	135	ring_7_3	0	15	108	620	135	144	81	-43.75
wstate	253	135	full_7_3	0	12	0	-100	135	141	135	-4.26
wstate	253	135	ring_5_4	0	48	72	50	135	150	79	-47.33
qaoa	285	34	full_10_2	63	6	69	1050	164	50	65	30
qaoa	285	34	ring_10_2	291	36	141	291.67	303	54	60	11.11
qaoa	285	34	grid_9_3	198	36	243	575	247	51	71	39.22
qaoa	285	34	grid_4_5	357	39	141	261.54	369	58	70	20.69
qaoa	285	34	line_5_4	438	75	210	180	391	56	71	26.79
qaoa	285	34	t_horizontal_5_4	348	54	234	333.33	337	56	67	19.64
qaoa	285	34	t_vertical_5_4	336	63	234	271.43	351	62	89	43.55
qaoa	285	34	ring_5_4	171	51	93	82.35	250	83	43	-48.19
qaoa	285	34	ring_7_3	228	51	177	247.06	267	76	71	-6.58
qaoa	285	34	full_7_3	108	15	51	240	223	50	53	6
qft	591	118	full_10_2	378	48	321	568.75	485	307	241	-21.5

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Table 3: Additional swap gates and circuit depth, n = 15

benchmark	g	d	layout	s basic	s sabre	s look	swap (%)	d basic	d swap	d look	d (%)
qft	591	118	ring_10_2	2034	384	504	31.25	707	389	186	-52.19
qft	591	118	grid_9_3	1164	270	450	66.67	680	292	203	-30.48
qft	591	118	grid_4_5	1698	312	525	68.27	734	324	214	-33.95
qft	591	118	line_5_4	2877	426	519	21.83	742	316	170	-46.2
qft	591	118	t_horizontal_5_4	1842	381	519	36.22	729	309	170	-44.98
qft	591	118	t_vertical_5_4	1680	396	615	55.3	642	352	222	-36.93
qft	591	118	full_7_3	501	117	300	156.41	588	295	213	-27.8
qftentangled	608	122	full_10_2	378	72	321	345.83	489	329	245	-25.53
qftentangled	608	122	ring_10_2	2034	360	624	73.33	711	344	216	-37.21
qftentangled	608	122	grid_9_3	1128	279	357	27.96	650	327	192	-41.28
qftentangled	608	122	grid_4_5	1575	300	561	87	687	315	223	-29.21
qftentangled	608	122	line_5_4	2877	414	543	31.16	746	311	177	-43.09
qftentangled	608	122	t_horizontal_5_4	1788	390	543	39.23	698	320	177	-44.69
qftentangled	608	122	t_vertical_5_4	1764	411	621	51.09	653	393	234	-40.46
qftentangled	608	122	full_7_3	501	150	300	100	592	399	217	-45.61
realamprandom	615	77	full_10_2	1146	177	315	77.97	1399	372	210	-43.55
realamprandom	615	77	ring_10_2	5427	1155	1332	15.32	1879	565	302	-46.55
realamprandom	615	77	grid_9_3	3018	666	834	25.23	1603	439	240	-45.33
realamprandom	615	77	grid_4_5	5277	645	759	17.67	1840	412	198	-51.94
realamprandom	615	77	line_5_4	8190	888	936	5.41	1996	418	162	-61.24
realamprandom	615	77	t_horizontal_5_4	5859	885	1020	15.25	1927	446	234	-47.53
realamprandom	615	77	t_vertical_5_4	5304	1047	1098	4.87	1919	564	261	-53.72
realamprandom	615	77	ring_7_3	2679	999	1224	22.52	1444	740	319	-56.89
twolocalrandom	615	77	full_10_2	1146	138	315	128.26	1399	327	210	-35.78
twolocalrandom	615	77	ring_10_2	5427	1131	1332	17.77	1879	601	302	-49.75
twolocalrandom	615	77	grid_9_3	3018	672	834	24.11	1603	453	240	-47.02
twolocalrandom	615	77	grid_4_5	5277	696	759	9.05	1840	446	198	-55.61
twolocalrandom	615	77	line_5_4	8190	876	936	6.85	1996	416	162	-61.06
twolocalrandom	615	77	t_horizontal_5_4	5859	876	1020	16.44	1927	424	234	-44.81
twolocalrandom	615	77	t_vertical_5_4	5304	1011	1098	8.61	1919	593	261	-55.99
twolocalrandom	615	77	ring_7_3	2679	882	1224	38.78	1444	595	319	-46.39
su2random	675	81	full_10_2	1146	189	315	66.67	1433	452	215	-52.43
su2random	675	81	ring_10_2	5427	1155	1338	15.84	1922	661	305	-53.86
su2random	675	81	grid_9_3	3018	672	831	23.66	1641	489	242	-50.51
su2random	675	81	grid_4_5	5277	672	759	12.95	1881	422	202	-52.13
su2random	675	81	line_5_4	8190	897	936	4.35	2039	461	165	-64.21
su2random	675	81	t_horizontal_5_4	5859	993	1020	2.72	1970	538	237	-55.95
su2random	675	81	t_vertical_5_4	5304	1086	1098	1.1	1962	658	265	-59.73
qnn	914	158	full_10_2	720	90	369	310	1103	527	302	-42.69
qnn	914	158	ring_10_2	3576	708	1116	57.63	1356	558	349	-37.46
qnn	914	158	grid_9_3	2061	444	771	73.65	1277	456	343	-24.78
qnn	914	158	grid_4_5	3384	447	858	91.95	1386	414	355	-14.25
qnn	914	158	line_5_4	5460	591	732	23.86	1442	431	234	-45.71
qnn	914	158	t_horizontal_5_4	4041	606	1065	75.74	1458	481	355	-26.2
qnn	914	158	t_vertical_5_4	3669	600	1077	79.5	1449	509	344	-32.42
portfolioqaoa	1260	192	full_10_2	1146	141	393	178.72	1766	777	351	-54.83
portfolioqaoa	1260	192	ring_10_2	5427	1065	1701	59.72	2060	793	534	-32.66
portfolioqaoa	1260	192	grid_9_3	3018	663	1074	61.99	1843	655	412	-37.1
portfolioqaoa	1260	192	grid_4_5	5277	663	1170	76.47	2077	585	418	-28.55
portfolioqaoa	1260	192	line_5_4	8190	888	948	6.76	2165	531	260	-51.04
portfolioqaoa	1260	192	t_horizontal_5_4	5859	822	1359	65.33	2156	636	420	-33.96
portfolioqaoa	1260	192	t_vertical_5_4	5304	879	1440	63.82	2150	641	430	-32.92
random	1992	412	full_10_2	534	246	597	142.68	1200	957	529	-44.72
random	1992	412	ring_10_2	2127	1050	1407	34	2042	1129	580	-48.63
random	1992	412	grid_9_3	1647	783	1140	45.59	1913	1177	576	-51.06
random	1992	412	grid_4_5	2250	1041	1533	47.26	2103	1056	629	-40.44
random	1992	412	line_5_4	3348	1623	1926	18.67	2915	1128	656	-41.84
random	1992	412	t_horizontal_5_4	2613	1407	1815	29	2408	1130	644	-43.01
random	1992	412	t_vertical_5_4	2475	1203	1800	49.63	2366	1214	658	-45.8
portfoliovqe	2505	327	full_10_2	1146	189	534	182.54	1903	984	504	-48.78
portfoliovqe	2505	327	ring_10_2	5427	1098	1590	44.81	2195	1030	520	-49.51

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Table 3: Additional swap gates and circuit depth, n = 15

benchmark	g	d	layout	s basic	s sabre	s look	swap (%)	d basic	d swap	d look	d (%)
portfoliovqe	2505	327	grid_9_3	3018	636	1107	74.06	2112	835	471	-43.59
portfoliovqe	2505	327	grid_4_5	5277	648	768	18.52	2244	756	412	-45.5
portfoliovqe	2505	327	line_5_4	8190	891	948	6.4	2297	695	378	-45.61
portfoliovqe	2505	327	t_horizontal_5_4	5859	975	1047	7.38	2288	893	431	-51.74
portfoliovqe	2505	327	t_vertical_5_4	5304	942	1251	32.8	2280	834	456	-45.32