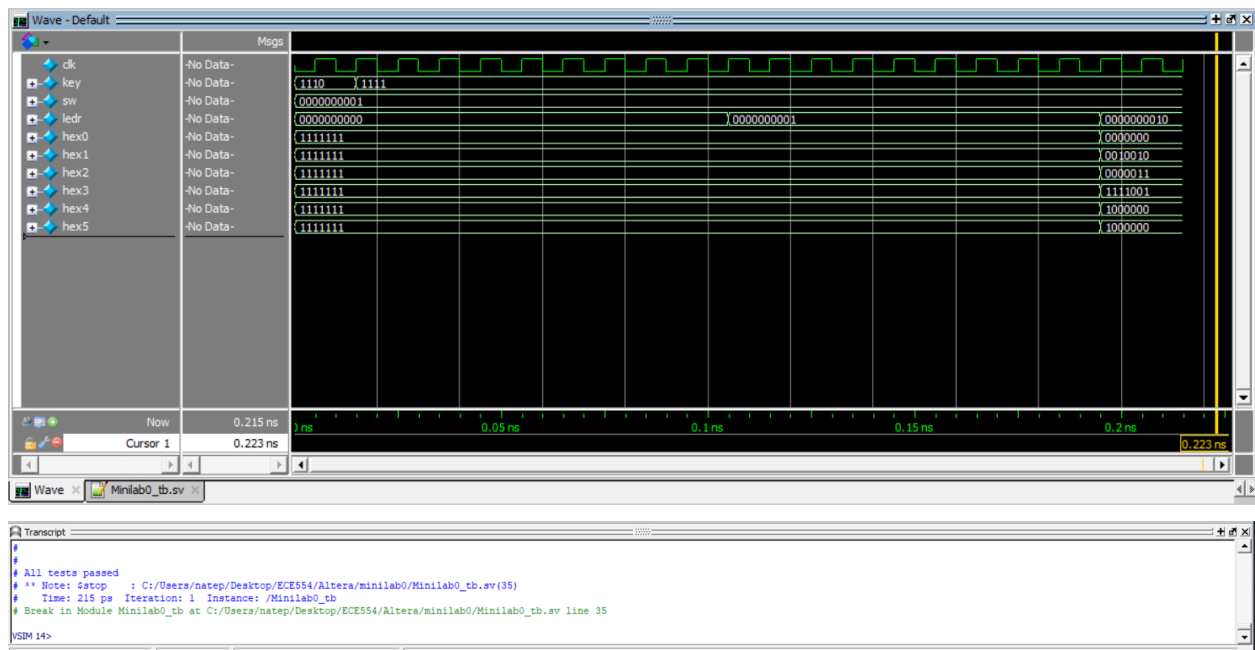


MiniLab 1a Report

Nathan Parmley

Simulation:

The top-level DUT instantiates two FIFOs and one MAC and fills the FIFOs with [0,5,10,15,20,25,30,35] and [0,10,20,30,40,50,60,70], which should result in a final MAC result of 7000. This value is 0x001B58 in hex, so I wrote a testbench that will wait until we have reached the DONE state and check if the hex 7-segment registers have the correct values that correspond to this hex value. The waveform below shows that the hex registers have the expected values and the simulation log shows that all tests passed.



Resource Utilization:

- My Design:

```
+-----+
; Analysis & Synthesis Resource Usage Summary
+-----+
; Resource ; Usage
+-----+
; Estimate of Logic utilization (ALMs needed) ; 128
;
; Combinational ALUT usage for logic ; 138
; -- 7 input functions ; 0
; -- 6 input functions ; 15
; -- 5 input functions ; 0
; -- 4 input functions ; 84
; -- <=3 input functions ; 39
;
; Dedicated logic registers ; 170
;
; I/O pins ; 70
;
; Total DSP Blocks ; 1
;
; Maximum fan-out node ; CLOCK_50~input
; Maximum fan-out ; 170
; Total fan-out ; 1516
; Average fan-out ; 3.38
+-----+
```

- IP Design:

```
+-----+
; Analysis & Synthesis Resource Usage Summary
+-----+
; Resource ; Usage
+-----+
; Estimate of Logic utilization (ALMs needed) ; 99
;
; Combinational ALUT usage for logic ; 174
; -- 7 input functions ; 0
; -- 6 input functions ; 10
; -- 5 input functions ; 11
; -- 4 input functions ; 91
; -- <=3 input functions ; 62
;
; Dedicated logic registers ; 116
;
; I/O pins ; 70
; Total MLAB memory bits ; 0
; Total block memory bits ; 128
;
; Total DSP Blocks ; 1
;
; Maximum fan-out node ; CLOCK_50~input
; Maximum fan-out ; 132
; Total fan-out ; 1233
; Average fan-out ; 2.76
+-----+
```

My design uses more logic registers and ALMs, but uses less ALUTs than the design using IPs. My design also has a larger average fan-out than the IP design.