Panchip Microelectronics Co., Ltd.

PAN2025

User's Manual

2.4GHz RF Transceiver SOC

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Shanghai Panchip Microelectronics Co., Ltd.

Addr: Room 302 of Building D, No. 666 Shengxia Road
Zhangjiang Hi-Tech Park, Shanghai
People's Republic of China

Tel: 021-50802371

Web: http://www.panchip.com

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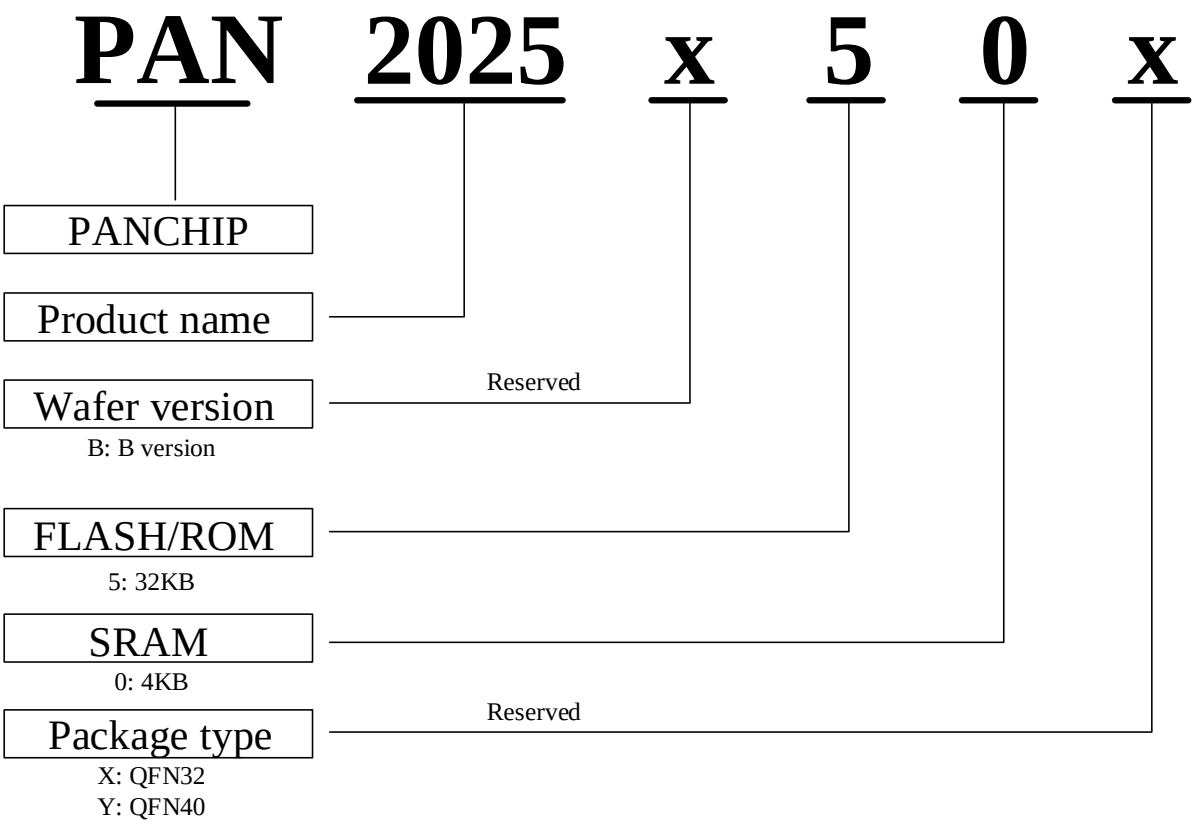
1.0	Nov.2019	Initial, A version.	-
1.1	Feb.2020	Refresh to B version. ● The value of voltage to 2.2~3.6V ● Part of the register description	-
1.2	Aug.2020	Refresh the voltage range of ADC. Refresh RF's contents.	-
1.3	Jan.2021	Refresh: ● The application reference diagram	-
1.4	Nov.2021	Refresh: ● The parameter of Low Power in chapter "Key Features"	-

Naming Rules



Product Series

Product series	Wafer version	MCU	Flash	SRAM	Package	Timer	PWM	ADC	I/O	Connectivity		
										UART	I2C	SPI
PAN2025B50X	B	72 MHz	32 KB	4 KB	QFN32	2×32bits	8	7ch 12bits	21	4	1	1
PAN2025B50Y	B	72 MHz	32 KB	4 KB	QFN40	2×32bits	8	8ch 12bits	24	4	1	1

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Abbreviation

A	
APB	Advanced Peripheral Bus
ANA	Analog Control
APROM	Application ROM
B	
BOD	Brown-out Detector
BOM	Bill of Materials
BUFERRINT	Buffer Error Interrupt
C	
CRC	Cyclic Redundancy Check
D	
DSSS	Direct Sequence Spread Spectrum
E	
EEPROM	Electrically Erasable Programmable read only memory
ESD	Electro-Static discharge
F	
FIFO	First Input First Output
FMC	Flash Memory Controller
G	
GC	General Call
GFSK	Gauss frequency Shift Keying
GPIO	General-purpose I/O
H	
HXT	16 MHz external high speed crystal oscillator
I	
I2C	Inter-Integrated Circuit
IAP	In-Application-Programming
ICP	In-Circuit Programming
ISM	Industrial Scientific Medical
ISP	In-System Programming
L	
LDO	Low dropout regulator
LDROM	Loader ROM
LNA	Low Noise Amplifier
LSB	Least significant bit
LVR	Low Voltage Reset
M	
MISO	Master input slave output
MOSI	Master output slave input
MSB	Most Significant Bit
N	
NACK	Not Acknowledge
NRESET	Pin reset
P	
DPLL	Digital PhaseLockedLoop
POR	Power-on Reset
PWM	Pulse Width Modulation
R	
RCC	Reset and clock controller
RCH	16 MHz internal high speed RC oscillator
RCL	32 KHz internal low speed RC oscillator
RDAINT	Receiver threshold level reached interrupt
RF	Radio frequency
RLSINT	Line status interrupt
RTOS	Real Time Operating System
RXTOINT	Receiver buffer time-out interrupt
S	
SCL	Serial clock
SDA	Serial data
SLA	Slave address
SPI	Serial Peripheral Interface
SRAM	Static random access memory
SWD	Serial Wire Debug
T	
TFL	Transmit FIFO Level
TFR	Transmit FIFO Read
THR	Transmit Holding Register
THREINT	Transmitter FIFO empty interrupt
TMR	Timer Controller
U	
UART	Universal Asynchronous Receiver/Transmitters
W	
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

1 General Description

The PAN2025 is a system-on-chip (SOC), embedded with 2.4GHz radio frequency(RF) transceiver and 32-bit microcontroller unit(MCU). The 2.4GHz transceiver is designed to operate in the world-wide ISM frequency band at 2.400~2.483GHz. It integrates radio RF transceiver, frequency synthesizer, crystal oscillator, baseband GFSK and DSSS modem, and other related modules. The PAN2025 supports both one-to-one and one-to-multiple communication with ACK. TX power, frequency channel, and data rates are configurable. Matching network and other external components are integrated into the chip to reduce the system cost.

The 32-bit MCU supports a wide range of applications from low-end, price-sensitive designs to computing-intensive system.

The PAN2025 can run up to 72 MHz and operate at a wide voltage range of 2.2V ~ 3.6V and temperature range of -40℃~ +85℃. The embedded program flash size is up to 32K bytes and SRAM size is up to 4K bytes. It also offers configurable flash size for the ISP.

The PAN2025 has many high-performance peripherals, such as 16 MHz internal RC oscillator (±1% accuracy after calibration), I/O port with up to 24 pins, three 32-bit timers, four UARTs, one SPI interface, one I2C interface, one 16-bit PWM generator providing eight channels, one 8-channel 12-bit ADC, Watchdog Timer, Window Watchdog Timer and one Brown-out Detector. All these peripherals have been integrated into the PAN2025 to reduce the number of components, board area and system cost.

Additionally, the PAN2025 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end products. PAN2025 also supports IAP (In-Application-Programming) function, users can switch the code execution without resetting the chip after the embedded flash is updated. There are two kinds of packages, QFN32 and QFN40, which are compatible with Panchip's PAN163 and PAN159 products respectively.

1.1 Key Features

- RF
  - Radio
    - Frequency band: 2.400~2.483GHz
    - Data rate: 1Mbps, 250Kbps
    - DSSS and GFSK modulation
    - RF communication mode: PAN2025B is recommended to communicate in RX mode.
  - Receiver
    - -100dBm sensitivity at 1Mbps@DSSS
    - -91dBm sensitivity at 1Mbps@GFSK
    - -94dBm sensitivity at 250Kbps@GFSK
  - Transmitter
    - Programmable output power: 12, 10, 8, 7, 6, 5, 4, 3, 2, 1, 0 or -4dBm
    - 25mA at 0dBm output power
    - 55mA at 10dBm output power

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- Core
  - 32-bit MCU running up to 72 MHz
  - One 24-bit system timer
  - Supports three level low power mode
  - One single-cycle 32-bit hardware multiplier
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Built-in LDO for wide operating voltage: 2.2V to 3.6V
- Memory
  - Up to 29 KB internal flash memory for program memory (APROM)
  - Configurable flash memory for data memory (Data Flash)
  - 2 KB internal flash memory for loader (LDROM)
  - Up to 4 KB internal SRAM
- Low Power
  - Active mode RX:40mA
  - Active mode TX at 0dBm:50mA
  - Active mode TX at 10dBm:68mA
  - Standby mode (external interrupts, CPU Power Down):0.2uA
  - Standby mode (external interrupts, CPU Power Down, SRAM retention): 1uA
  - Standby mode (sleep timer running, CPU Power Down):2.5uA
  - Standby mode (sleep timer running, CPU Sleep, SRAM retention): 3.3uA
- Clock Control
  - Programmable system clock sources
  - 16 MHz external crystal oscillator
  - Built-in 16 MHz internal high speed RC oscillator
  - Built-in 32 KHz internal low speed RC oscillator
  - Internal DPLL allowing CPU frequency up to maximum 72 MHz
- I/O Port
  - Up to 24 general-purpose I/O (GPIO) pins
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Schmitt trigger input
- Timer
  - Provides three 32-bit timers: each timer includes one 8-bit pre-scaler counter and one 24-bit up-counter
    - Supports Event Counter mode
    - Supports Toggle Output mode
    - Supports external trigger in Pulse Width Measurement mode
    - Supports external trigger in Pulse Width Capture mode
- WDT
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out

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- WWDT
  - Flexible WWDT time-out window period with 6-bit down-counter value and 6-bit compare value
  - Supports 4-bit value to program the prescale counter's period of WWDT counter, the prescale counter is up to 11 bits
- PWM
  - Up to four built-in 16-bit PWM generators, providing eight PWM outputs or four complementary pairs of PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-time generator for each PWM generator
- UART
  - Four UART devices
  - Buffered receiver and transmitter, each with 8-byte FIFO
  - Programmable baud-rate generator, baud rate up to 1 system clock
- SPI
  - One SPI device
  - Master frequency up to 24 MHz, and Slave frequency up to 10 MHz
  - Supports Master/Slave mode
  - Full-duplex synchronous serial data transfer
- I2C
  - One I2C devices
  - Supports Master/Slave mode
  - Bidirectional data transfer between Master and Slave
- ADC
  - Analog input voltage range: 0~2V or 0~VDD for PAN2025BX and PAN2025BY
  - Guaranteed 12-bit resolution and 10-bit accuracy
  - Up to eight single-end analog input channels, one bandgap input channel, one RSSI input channel, one GND check channel and one voltage input channel.
- ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application-Programming) update
- BOD
  - With 4 programmable threshold levels: 3.0V/2.7V/2.4V/2.2V
  - Supports Brown-out interrupt and reset option
- 32-bit unique ID
- LVR
  - Threshold voltage level: 2.0±0.1V
- Operating Temperature: -40℃ ~85℃
- Operating Voltage: 2.2V ~ 3.6V
- Reliability:
  - ESD HBM pass ±5KV
  - ESD CDM pass ±2KV
  - ESD MM pass ±300V
- Packages:
  - QFN32 (5×5)
  - QFN40 (5×5)

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1.2 Typical Applications

- Small flying saucer with four-axises rotor
- Remote control toys
- Smart home
- TV and set-top box remote control

2 Block Diagram

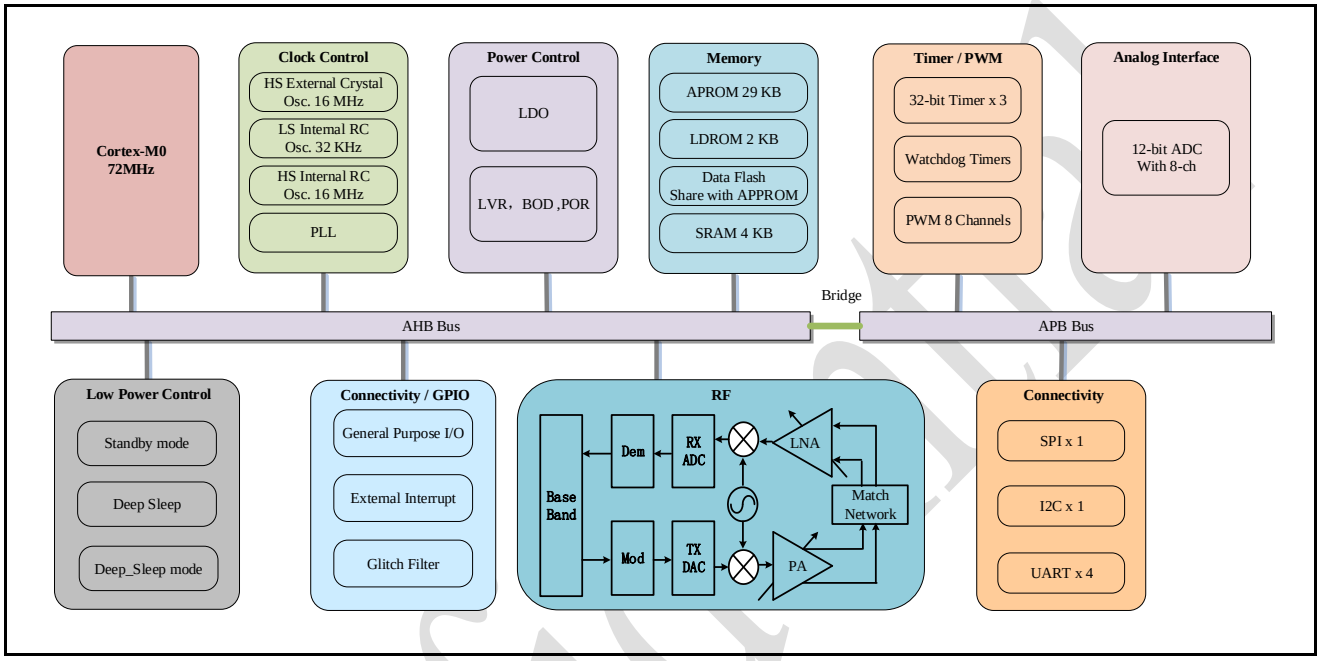

Figure 2-1 PAN2025 Block Diagram

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3 Pin Information

3.1 QFN32-PIN

3.1.1 QFN32-Pin Diagram

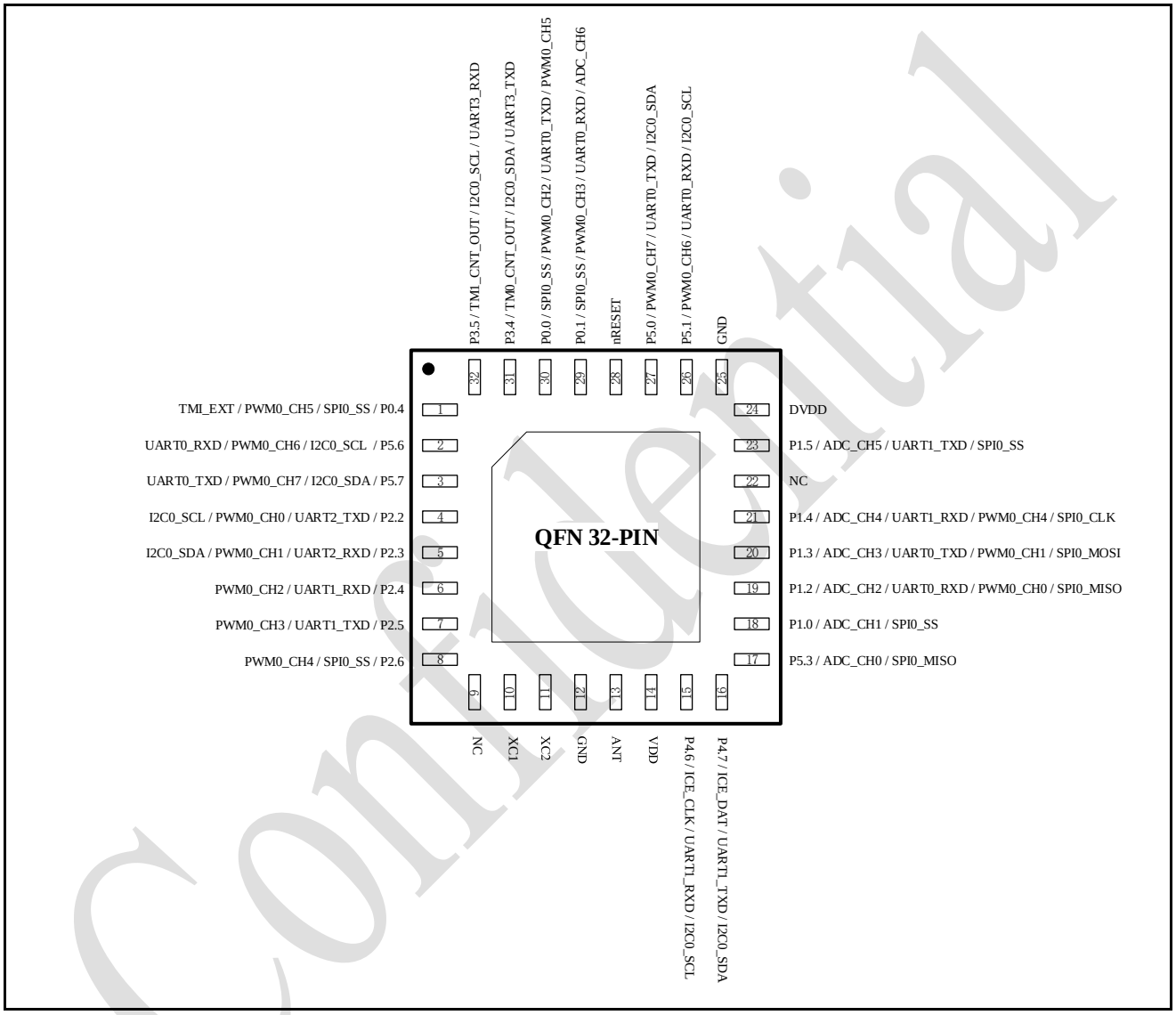

Figure 3-1 PAN2025 QFN 32-PIN Diagram

3.1.2 QFN32-Pin Description

Detail pin descriptions see Table 3-1.

Table 3-1 PAN2025 QFN32 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	P0.4	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin

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	PWM0_CH5	O	PWM0 Channel5 Output Pin
	TM1_EXT	I	Timer1 External Input Pin
2	P5.6	I/O	General Purpose Digital I/O Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
	PWM0_CH6	O	PWM0 Channel6 Output Pin
	UART0_RXD	I	UART0 RX Pin
3	P5.7	I/O	General Purpose Digital I/O Pin
	I2C0_SDA	I/O	I2C0 Data Pin
	PWM0_CH7	O	PWM0 Channel7 Output Pin
	UART0_TXD	O	UART0 TX Pin
4	P2.2	I/O	General Purpose Digital I/O Pin
	UART2_TXD	O	UART2 TX Pin
	PWM0_CH0	O	PWM0 Channel0 Output Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
5	P2.3	I/O	General Purpose Digital I/O Pin
	UART2_RXD	I	UART2 RX Pin
	PWM0_CH1	O	PWM0 Channel1 Output Pin
	I2C0_SDA	I/O	I2C0 Data Pin
6	P2.4	I/O	General Purpose Digital I/O Pin
	UART1_RXD	I	UART1 RX Pin
	PWM0_CH2	O	PWM0 Channel2 Output Pin
7	P2.5	I/O	General Purpose Digital I/O Pin
	UART1_TXD	O	UART1 TX Pin
	PWM0_CH3	O	PWM0 Channel3 Output Pin
8	P2.6	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH4	O	PWM0 Channel4 Output Pin
9	-	-	-
10	XC1	AI	Crystal Pin1
11	XC2	AO	Crystal Pin2
12	GND	P	Ground Pin
13	ANT	AIO	Antenna Pin
14	VDD	P	SoC Power Supply VDD Pin
15	P4.6	I/O	General Purpose Digital I/O Pin
	ICE_CLK	I	ICE Clk Input Pin
	UART1_RXD	O	UART1 RX Pin
	I2C0_SCL	I/O	I2C0 CLK Pin

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16	P4.7	I/O	General Purpose Digital I/O Pin
	ICE_DAT	I	Debug and Program Data Pin
	UART1_TXD	O	UART1 TX Pin
	I2C0_SDA	I/O	I2C0 Data Pin
17	P5.3	I/O	General Purpose Digital I/O Pin
	ADC_CH0	AI	ADC Channel0 Analog Input Pin
	SPI0_MISO	I	SPI0 MISO Pin
18	P1.0	I/O	General Purpose Digital I/O Pin
	ADC_CH1	AI	ADC Channel1 Analog Input Pin
	SPI0_SS	O	SPI0 SS Pin
19	P1.2	I/O	General Purpose Digital I/O Pin
	ADC_CH2	AI	ADC Channel2 Analog Input Pin
	UART0_RXD	I	UART0 RX Pin
	PWM0_CH0	O	PWM0 Channel0 Output Pin
	SPI0_MISO	I	SPI0 MISO Pin
20	P1.3	I/O	General Purpose Digital I/O Pin
	ADC_CH3	AI	ADC Channel3 Analog Input Pin
	UART0_TXD	O	UART0 TX Pin
	PWM0_CH1	O	PWM0 Channel1 Output Pin
	SPI0_MOSI	I	SPI0 MOSI Pin
21	P1.4	I/O	General Purpose Digital I/O Pin
	ADC_CH4	AI	ADC Channel4 Analog Input Pin
	UART1_RXD	I	UART1 RX Pin
	PWM0_CH4	O	PWM0 Channel4 Output Pin
	SPI0_CLK	O	SPI0 CLK Pin
22	-	-	-
23	P1.5	I/O	General Purpose Digital I/O Pin
	ADC_CH5	AI	ADC Channel5 Analog Input Pin
	UART1_TXD	O	UART1 TX Pin
	SPI0_SS	O	SPI0 SS Pin
24	DVDD	P	Core Power Supply, Generated by Internal LDO
25	GND	P	Ground Pin
26	P5.1	I/O	General Purpose Digital I/O Pin
	PWM0_CH6	O	PWM0 Channel6 Output Pin
	UART0_RXD	I	UART0 RX Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
27	P5.0	I/O	General Purpose Digital I/O Pin

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	PWM0_CH7	O	PWM0 Channel7 Output Pin
	UART0_TXD	O	UART0 TX Pin
	I2C0_SDA	I/O	I2C0 Data Pin
28	nRESET	I	Reset Pin
29	P0.1	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH3	O	PWM0 Channel3 Output Pin
	UART0_RXD	I	UART0 RX Pin
	ADC_CH6	AI	ADC Channel6 Analog Input Pin
30	P0.0	I/O	General Purpose Digital I/O Pin
	PWM0_CH2	O	PWM0 Channel2 Output Pin
	UART0_TXD	O	UART0 TX Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH5	O	PWM0 Channel5 Output Pin
31	P3.4	I/O	General Purpose Digital I/O Pin
	TM0_CNT_OUT	O	TM0_CNT Output Pin
	I2C0_SDA	I/O	I2C0 Data Pin
	UART3_TXD	O	UART3 TX Pin
32	P3.5	I/O	General Purpose Digital I/O Pin
	TM1_CNT_OUT	O	TM1_CNT Output Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
	UART3_RXD	I	UART3 RX Pin
33	GND	P	Ground Pin

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3.2 QFN40-PIN

3.2.1 QFN40-Pin Diagram

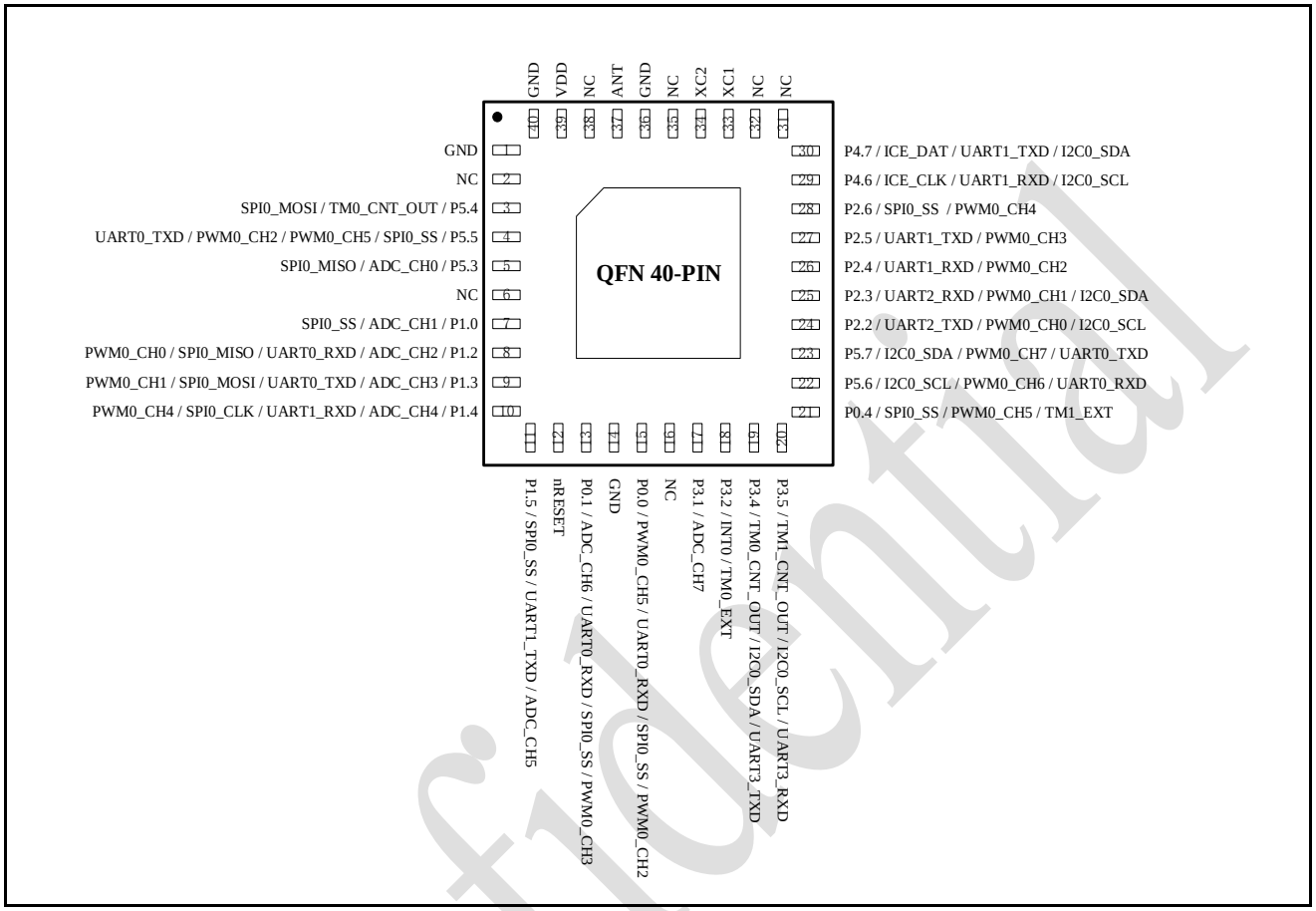

Figure 3-2 PAN2025 QFN 40-PIN Diagram

3.2.2 QFN40-Pin Description

Detail pin descriptions see Table 3-2.

Table 3-2 PAN2025 QFN40 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	GND	P	Ground Pin
2	-	-	-
3	P5.4	I/O	General Purpose Digital I/O Pin
	TM0_CNT_OUT	O	TM0_CNT Output Pin
	SPI0_MOSI	I	SPI0 MOSI Pin
4	P5.5	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH5	O	PWM0 Channel5 Output Pin

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	PWM0_CH2	O	PWM0 Channel2 Output Pin
	UART0_TXD	O	UART0 TX Pin
5	P5.3	I/O	General Purpose Digital I/O Pin
	ADC_CH0	AI	ADC Channel0 Analog Input Pin
	SPI0_MISO	I	SPI0 MISO Pin
6	-	-	-
7	P1.0	I/O	General Purpose Digital I/O Pin
	ADC_CH1	AI	ADC Channel1 Analog Input Pin
	SPI0_SS	O	SPI0 SS Pin
8	P1.2	I/O	General Purpose Digital I/O Pin
	ADC_CH2	AI	ADC Channel2 Analog Input Pin
	UART0_RXD	I	UART0 RX Pin
	SPI0_MISO	O	SPI0 SS Pin
	PWM0_CH0	O	PWM0 Channel0 Output Pin
9	P1.3	I/O	General Purpose Digital I/O Pin
	ADC_CH3	AI	ADC Channel3 Analog Input Pin
	UART0_TXD	O	UART0 TX Pin
	SPI0_MOSI	I	SPI0 MOSI Pin
	PWM0_CH1	O	PWM0 Channel1 Output Pin
10	P1.4	I/O	General Purpose Digital I/O Pin
	ADC_CH4	AI	ADC Channel4 Analog Input Pin
	UART1_RXD	I	UART1 RX Pin
	SPI0_CLK	O	SPI0 CLK Pin
	PWM0_CH4	O	PWM0 Channel4 Output Pin
11	P1.5	I/O	General Purpose Digital I/O Pin
	ADC_CH5	AI	ADC Channel5 Analog Input Pin
	UART1_TXD	O	UART1 TX Pin
	SPI0_SS	O	SPI0 SS Pin
12	nRESET	I	Reset Pin
13	P0.1	I/O	General Purpose Digital I/O Pin
	ADC_CH6	AI	ADC Channel6 Analog Input Pin
	UART0_RXD	I	UART0 RX Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH3	O	PWM0 Channel3 Output Pin
14	GND	P	Ground Pin
15	P0.0	I/O	General Purpose Digital I/O Pin
	PWM0_CH5	O	PWM0 Channel5 Output Pin

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	UART0_TXD	O	UART0 TX Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH2	O	PWM0 Channel2 Output Pin
16	-	-	-
17	P3.1	I/O	General Purpose Digital I/O Pin
	ADC_CH7	AI	ADC Channel7 Analog Input Pin
18	P3.2	I/O	General Purpose Digital I/O Pin
	INT0	I	External Interrupt0 Input Pin
	TM0_EXT	I	Timer0 External Input Pin
19	P3.4	I/O	General Purpose Digital I/O Pin
	TM0_CNT_OUT	O	TM0_CNT Output Pin
	I2C0_SDA	I/O	I2C0 Data Pin
	UART3_TXD	O	UART3 TX Pin
20	P3.5	I/O	General Purpose Digital I/O Pin
	TM1_CNT_OUT	O	TM1_CNT Output Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
	UART3_RXD	I	UART3 RX Pin
21	P0.4	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH5	O	PWM0 Channel5 Output Pin
	TM1_EXT	I	Timer1 External Input Pin
22	P5.6	I/O	General Purpose Digital I/O Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
	PWM0_CH6	O	PWM0 Channel6 Output Pin
	UART0_RXD	I	UART0 RX Pin
23	P5.7	I/O	General Purpose Digital I/O Pin
	I2C0_SDA	I/O	I2C0 Data Pin
	PWM0_CH7	O	PWM0 Channel7 Output Pin
	UART0_TXD	O	UART0 TX Pin
24	P2.2	I/O	General Purpose Digital I/O Pin
	UART2_TXD	O	UART2 TX Pin
	PWM0_CH0	O	PWM0 Channel0 Output Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
25	P2.3	I/O	General Purpose Digital I/O Pin
	UART2_RXD	I	UART2 RX Pin
	PWM0_CH1	O	PWM0 Channel1 Output Pin
	I2C0_SDA	I/O	I2C0 Data Pin
26	P2.4	I/O	General Purpose Digital I/O Pin

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	UART1_RXD	I	UART1 RX Pin
	PWM0_CH2	O	PWM0 Channel2 Output Pin
27	P2.5	I/O	General Purpose Digital I/O Pin
	UART1_TXD	O	UART1 TX Pin
	PWM0_CH3	O	PWM0 Channel3 Output Pin
28	P2.6	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH4	O	PWM0 Channel4 Output Pin
29	P4.6	I/O	General Purpose Digital I/O Pin
	ICE_CLK	I	ICE Clk Input Pin
	UART1_RXD	I	UART1 RX Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
30	P4.7	I/O	General Purpose Digital I/O Pin
	ICE_DAT	I	Debug and Program Data Pin
	UART1_TXD	O	UART1 TX Pin
	I2C0_SDA	I/O	I2C0 Data Pin
31	-	-	-
32	-	-	-
33	XC1	AI	Crystal Pin1
34	XC2	AO	Crystal Pin2
35	-	-	-
36	GND	P	Ground Pin
37	ANT	AIO	Antenna Pin
38	-	-	-
39	VDD	P	Soc Power Supply VDD Pin
40	GND	P	Ground Pin
41	GND	P	Ground Pin

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4 Function Description

4.1 System Manager

4.1.1 Overview

System management includes the following sections:

- System Power Architecture
- System Memory Map
- Chip reset, on-chip controllers reset, and multi-functional pin control
- System Control Block Registers

4.1.2 System Power Architecture

In this chip, the power distribution is divided into three segments.

- Analog power from VDD and GND, providing the power for analog module.
- Digital power from DVDD and DVSS, supplying 1.5V power for digital modules.
- Built-in capacitor for internal voltage regulator

The output of internal voltage regulator, DVDD, requires an external capacitor which is located close to the corresponding pin. Figure 4-1 shows the power distribution of the PAN2025 for PAN163. Figure 4-2 shows the power distribution of the PAN2025 for PAN159.

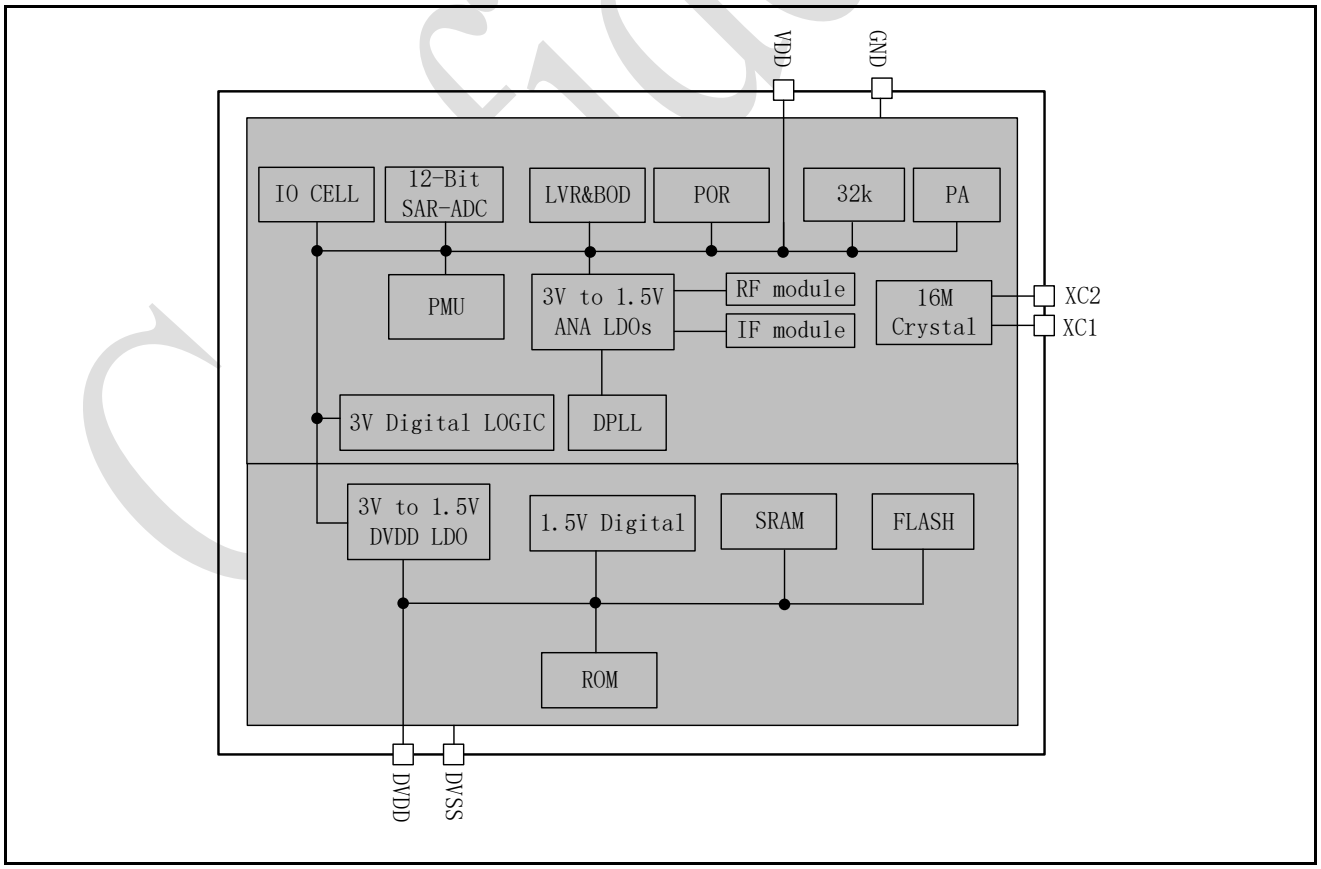

Figure 4-1 PAN2025 Power Architecture Diagram for PAN163

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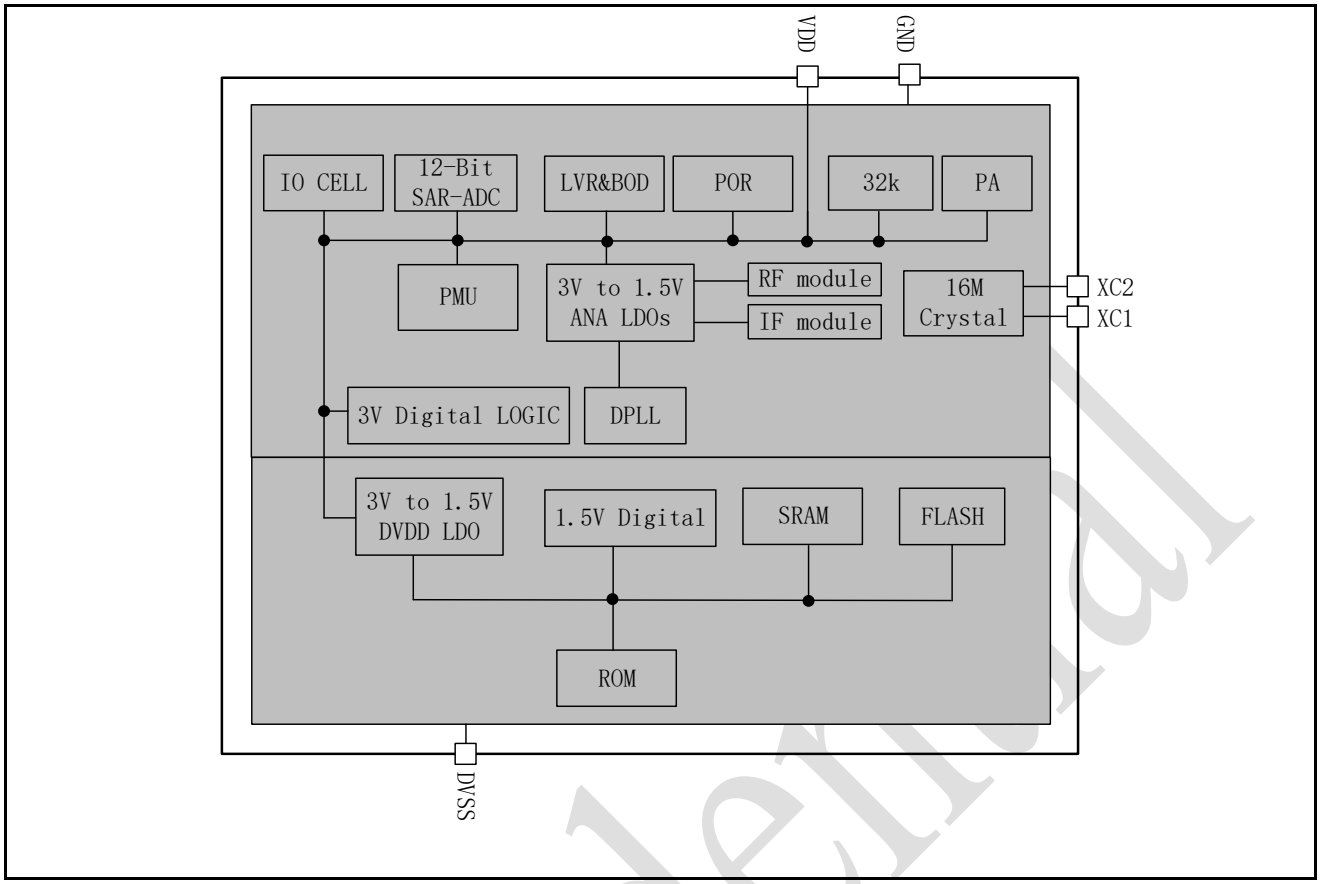

Figure 4-2 PAN2025 Power Architecture Diagram for PAN159

4.1.3 System Memory Mapping

Table 4-1 Memory Mapping Table

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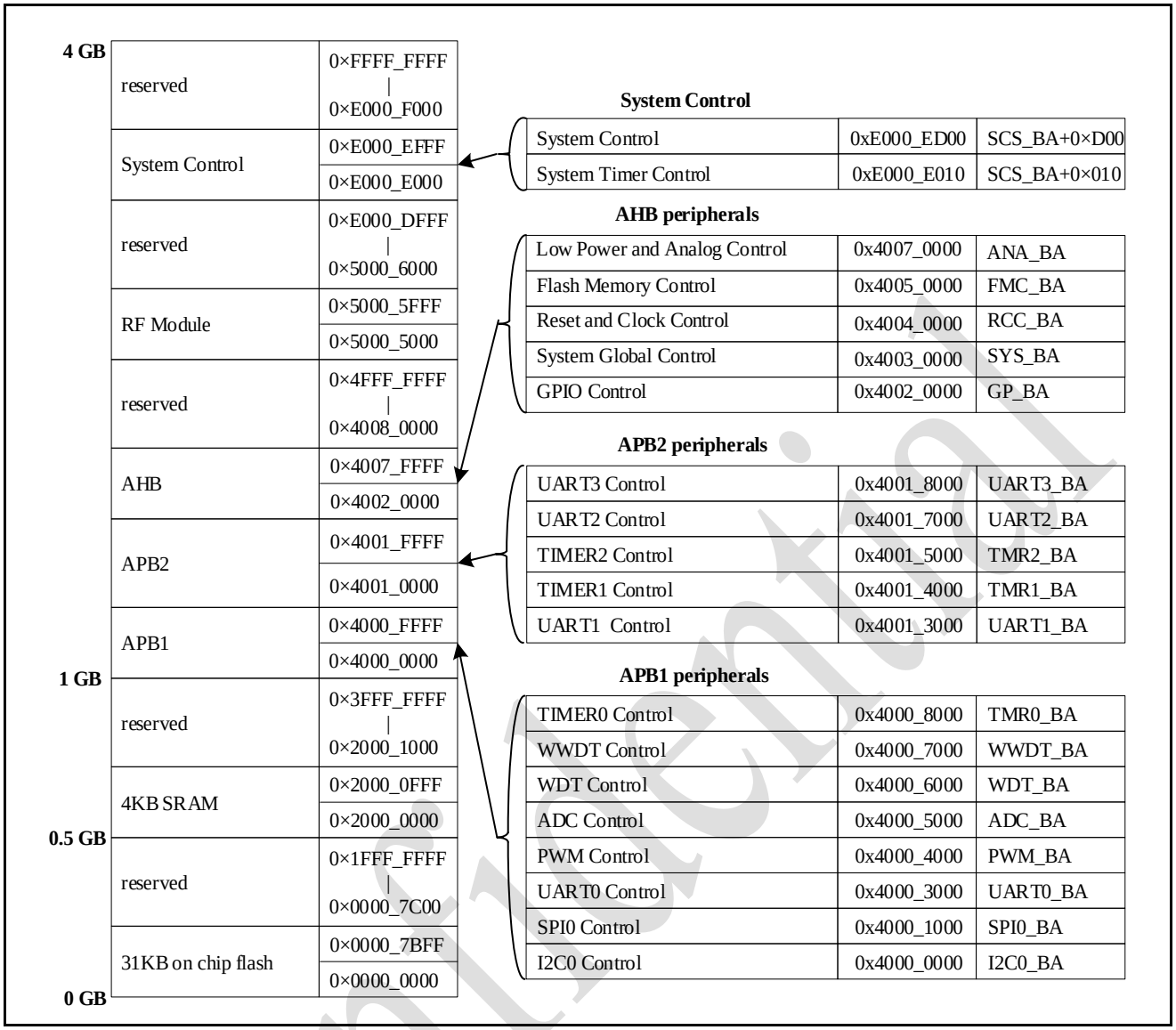

4.1.4 Memory Organization

4.1.4.1 Overview

The PAN2025 provides 4G-byte addressing space. The addressing space assigned to on-chip controllers is shown in the Table 4-2. The detailed register definition, addressing space and programming details will be described in the following sections for each on-chip peripheral.

4.1.4.2 System Memory Map

The memory locations assigned to on-chip controllers are shown in the Table 4-2.

Table 4-2 Address Space Assignments for On-Chip Modules

Addressing Space	Token	Modules
System Control Space (0×E000_E000 – 0×E000_EFFF)		
0×E000_ED00 – 0×E000_ED8F	SCS_BA+ 0×D00	System Control Block Registers
0×E000_E010 – 0×E000_E0FF	SCS_BA+ 0×010	System Timer Control Registers

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RF Module Space (0×5001_0000 – 0×5001_FFFF)		
0x5000_5000-0x5000_5FFF	RF_BA	RF Module Registers
AHB Modules Space (0×4002_0000 – 0×4007_FFFF)		
0x4007_0000-0x4007_FFFF	ANA_BA	Analog Low Power Controller Registers
0x4005_0000-0x4005_FFFF	FMC_BA	FMC Control Registers
0x4004_0000-0x4004_FFFF	RCC_BA	Reset and Clock Control Registers
0x4003_0000-0x4003_FFFF	SYS_BA	System Global Control Registers
0x4002_0000-0x4002_FFFF	GP_BA	GPIO (P0~P5) Control Registers
APB2 Modules Space (0×4001_0000 – 0×4001_FFFF)		
0x4001_8000-0x4001_8FFF	UART3_BA	UART3 Control Registers
0x4001_7000-0x4001_7FFF	UART2_BA	UART2 Control Registers
0x4001_5000-0x4001_5FFF	TMR2_BA	TIMER2 Control Registers
0x4001_4000-0x4001_4FFF	TMR1_BA	TIMER1 Control Registers
0x4001_3000-0x4001_3FFF	UART1_BA	UART1 Control Registers
APB1 Modules Space (0×4000_0000 – 0×4000_FFFF)		
0x4000_8000-0x4000_8FFF	TMR0_BA	TIMER0 Control Registers
0x4000_7000-0x4000_7FFF	WWDT_BA	WWDT Control Registers
0x4000_6000-0x4000_6FFF	WDT_BA	WDT Control Registers
0x4000_5000-0x4000_5FFF	ADC_BA	ADC Control Registers
0x4000_4000-0x4000_4FFF	PWM0_BA	PWM0 Control Registers
0x4000_3000-0x4000_3FFF	UART0_BA	UART0 Control Registers
0x4000_1000-0x4000_1FFF	SPI0_BA	SPI0 Control Registers
0x4000_0000-0x4000_0FFF	I2C0_BA	I2C0 Interface Control Registers
Flash and SRAM Memory Space		
0×2000_0000 – 0×2000_0FFF	SRAM_BA	SRAM Memory Space (4 KB)
0×0000_0000 – 0×0000_7BFF	FLASH_BA	Flash Memory Space (31 KB)

4.1.5 Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
SYS Base Address: **SYS_BA = 0x4003_0000**				
SYS_P0_MFP	SYS_BA+0x00	R/W	P0 Multiple Function and Input Type Control Register	0x0000_0000
SYS_P1_MFP	SYS_BA+0x04	R/W	P1 Multiple Function and Input Type Control Register	0x0000_0000
SYS_P2_MFP	SYS_BA+0x08	R/W	P2 Multiple Function and Input Type Control Register	0x0000_0000
SYS_P3_MFP	SYS_BA+0x0C	R/W	P3 Multiple Function and Input Type Control Register	0x0000_0000
SYS_P4_MFP	SYS_BA+0x10	R/W	P4 Multiple Function and Input Type Control Register	0x0000_00C0
SYS_P5_MFP	SYS_BA+0x14	R/W	P5 Multiple Function and Input Type Control Register	0x0000_0000
SYS_REGLCTL	SYS_BA+0x40	R/W	Register Write-Protection Control Register	0x0000_0000
SYS_STATUS	SYS_BA+0x44	RO	Register to reflect the status of ROM Mode	0x0000_0000

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4.1.6 Register Description

4.1.6.1 Multiple Function Port0 Control Register (SYS_P0_MFP)

Register	Offset	R/W	Description	Reset Value
SYS_P0_MFP	SYS_BA+0x00	R/W	P0 Multiple Function and Input Type Control Register	0x0000_0000

Bits	Description	
[31:24]	Reserved	Reserved.
[23:16]	EXT[7:0]	P0 Extend Function Select Bit The pin function of P0 depends on MFP and ALT and EXT. Refer to ALT Description for details.
[15]	ALT[7]	P0.7 Alternate Function Select Bit Bits EXT[7] (SYS_P0_MFP[23]), ALT[7] (SYS_P0_MFP[15]), and MFP[7] (SYS_P0_MFP[7]) determine the P0.7 function. (0, 0, 0) = GPIO function is selected. (0, 1, 0) = SPI0_CLK function is selected. (0, 1, 1) = PWM0_CH0 function is selected. Others: GPIO function is selected.
[14]	ALT[6]	P0.6 Alternate Function Select Bit Bits EXT[6] (SYS_P0_MFP[22]), ALT[6] (SYS_P0_MFP[14]), and MFP[6] (SYS_P0_MFP[6]) determine the P0.6 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = UART3_RXD function is selected. (0, 1, 0) = SPI0_MISO function is selected. (0, 1, 1) = PWM0_CH1 function is selected. Others: GPIO function is selected.
[13]	ALT[5]	P0.5 Alternate Function Select Bit Bits EXT[5] (SYS_P0_MFP[21]), ALT[5] (SYS_P0_MFP[13]), and MFP[5] (SYS_P0_MFP[5]) determine the P0.5 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = UART3_TXD function is selected. (0, 1, 0) = SPI0_MOSI function is selected. (0, 1, 1) = PWM0_CH4 function is selected. Others: GPIO function is selected.
[12]	ALT[4]	P0.4 Alternate Function Select Bit Bits EXT[4] (SYS_P0_MFP[20]), ALT[4] (SYS_P0_MFP[12]), and MFP[4] (SYS_P0_MFP[4]) determine the P0.4 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = TADC_DATH function is selected. (0, 1, 0) = SPI0_SS function is selected. (0, 1, 1) = PWM0_CH5 function is selected. (1, 0, 1) = TM1_EXT function is selected.

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		Others: GPIO function is selected.
[11]	ALT[3]	P0.3 Alternate Function Select Bit Bits EXT[3] (SYS_P0_MFP[19]), ALT[3] (SYS_P0_MFP[11]), and MFP[3] (SYS_P0_MFP[3]) determine the P0.3 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = SPI1_SS function is selected. Others: GPIO function is selected.
[10]	ALT[2]	P0.2 Alternate Function Select Bit Bits EXT[2] (SYS_P0_MFP[18]), ALT[2] (SYS_P0_MFP[10]), and MFP[2] (SYS_P0_MFP[2]) determine the P0.2 function. (0, 0, 0) = GPIO function is selected. Others: GPIO function is selected.
[9]	ALT[1]	P0.1 Alternate Function Select Bit Bits EXT[1] (SYS_P0_MFP[17]), ALT[1] (SYS_P0_MFP[9]), and MFP[1] (SYS_P0_MFP[1]) determine the P0.1 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = SPI0_SS function is selected. (0, 1, 0) = PWM0_CH3 function is selected. (0, 1, 1) = UART0_RXD function is selected. (1, 0, 1) = ADC_CH6 function is selected. Others: GPIO function is selected.
[8]	ALT[0]	P0.0 Alternate Function Select Bit Bits EXT[0] (SYS_P0_MFP[16]), ALT[0] (SYS_P0_MFP[8]), and MFP[0] (SYS_P0_MFP[0]) determine the P0.0 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = TADC_CLK function is selected. (0, 1, 0) = PWM0_CH2 function is selected. (0, 1, 1) = UART0_TXD function is selected. (1, 1, 0) = SPI0_SS function is selected. (1, 1, 1) = PWM0_CH5 function is selected. Others: GPIO function is selected.
[7:0]	MFP[7:0]	P0 Multiple Function Select Bit The pin function of P0 depends on MFP and ALT and EXT. Refer to ALT Description for details.

4.1.6.2 Multiple Function Port1 Control Register (SYS_P1_MFP)

Register	Offset	R/W	Description	Reset Value
SYS_P1_MFP	SYS_BA+0x04	R/W	P1 Multiple Function and Input Type Control Register	0x0000_0000

Bits	Description	
[31:24]	Reserved	Reserved.
[23:16]	EXT[7:0]	P1 Extend Function Select Bit The pin function of P0 depends on MFP and ALT and EXT.

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		Refer to ALT Description for details.
[15]	ALT[7]	P1.7 Alternate Function Select Bit Bits EXT[7] (SYS_P1_MFP[23]), ALT[7] (SYS_P1_MFP[15]), and MFP[7] (SYS_P1_MFP[7]) determine the P1.7 function. (0, 0, 0) = GPIO function is selected. Others: GPIO function is selected.
[14]	ALT[6]	P1.6 Alternate Function Select Bit Bits EXT[6] (SYS_P1_MFP[22]), ALT[6] (SYS_P1_MFP[14]), and MFP[6] (SYS_P1_MFP[6]) determine the P1.6 function. (0, 0, 0) = GPIO function is selected. (0, 1, 0) = UART2_RXD function is selected. Others: GPIO function is selected.
[13]	ALT[5]	P1.5 Alternate Function Select Bit Bits EXT[5] (SYS_P1_MFP[21]), ALT[5] (SYS_P1_MFP[13]), and MFP[5] (SYS_P1_MFP[5]) determine the P1.5 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = ADC_CH5 function is selected. (0, 1, 0) = UART1_TXD function is selected. (0, 1, 1) = RCL function is selected. (1, 0, 1) = SPI0_SS function is selected. Others: GPIO function is selected.
[12]	ALT[4]	P1.4 Alternate Function Select Bit Bits EXT[4] (SYS_P1_MFP[20]), ALT[4] (SYS_P1_MFP[12]), and MFP[4] (SYS_P1_MFP[4]) determine the P1.4 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = ADC_CH4 function is selected. (0, 1, 0) = UART1_RXD function is selected. (0, 1, 1) = PWM0_CH4 function is selected. (1, 0, 1) = SPI0_CLK function is selected. Others: GPIO function is selected.
[11]	ALT[3]	P1.3 Alternate Function Select Bit Bits EXT[3] (SYS_P1_MFP[19]), ALT[3] (SYS_P1_MFP[11]), and MFP[3] (SYS_P1_MFP[3]) determine the P1.3 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = ADC_CH3 function is selected. (0, 1, 0) = UART0_TXD function is selected. (0, 1, 1) = PWM0_CH1 function is selected. (1, 0, 1) = SPI0_MOSI function is selected. Others: GPIO function is selected.
[10]	ALT[2]	P1.2 Alternate Function Select Bit Bits EXT[2] (SYS_P1_MFP[18]), ALT[2] (SYS_P1_MFP[10]), and MFP[2] (SYS_P1_MFP[2]) determine the P1.2 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = ADC_CH2 function is selected.

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		(0, 1, 0) = UART0_RXD function is selected. (0, 1, 1) = PWM0_CH0 function is selected. (1, 0, 1) = SPI0_MISO function is selected. Others: GPIO function is selected.
[9]	ALT[1]	P1.1 Alternate Function Select Bit Bits EXT[1] (SYS_P1_MFP[17]), ALT[1] (SYS_P1_MFP[9]), and MFP[1] (SYS_P1_MFP[1]) determine the P1.1 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = SPI1_CLK function is selected. (0, 1, 0) = UART2_TXD function is selected. Others: GPIO function is selected.
[8]	ALT[0]	P1.0 Alternate Function Select Bit Bits EXT[0] (SYS_P1_MFP[16]), ALT[0] (SYS_P1_MFP[8]), and MFP[0] (SYS_P1_MFP[0]) determine the P1.0 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = ADC_CH1 function is selected. (0, 1, 1) = SPI0 function is selected. Others: GPIO function is selected.
[7:0]	MFP[7:0]	P1 Multiple Function Select Bit The pin function of P1 depends on MFP and ALT. Refer to ALT Description for details.

4.1.6.3 Multiple Function Port2 Control Register (SYS_P2_MFP)

Register	Offset	R/W	Description	Reset Value
SYS_P2_MFP	SYS_BA+0x08	R/W	P2 Multiple Function and Input Type Control Register	0x0000_0000

Bits	Description	
[31:24]	Reserved	Reserved.
[23:16]	EXT[7:0]	P2 Extend Function Select Bit The pin function of P0 depends on MFP and ALT and EXT. Refer to ALT Description for details.
[15]	ALT[7]	P2.7 Alternate Function Select Bit Bits EXT[7] (SYS_P2_MFP[23]), ALT[7] (SYS_P2_MFP[15]), and MFP[7] (SYS_P2_MFP[7]) determine the P2.7 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = ADC_CH8 function is selected. (0, 1, 0) = TM2_EXT or TM2 function is selected. (0, 1, 1) = TADC_VLD function is selected. Others: GPIO function is selected.
[14]	ALT[6]	P2.6 Alternate Function Select Bit Bits EXT[6] (SYS_P2_MFP[22]), ALT[6] (SYS_P2_MFP[14]), and MFP[6] (SYS_P2_MFP[6]) determine the P2.6 function. (0, 0, 0) = GPIO function is selected.

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		(0, 0, 1) = SPI0_SS function is selected. (0, 1, 0) = PWM0_CH4 function is selected. Others: GPIO function is selected.
[13]	ALT[5]	P2.5 Alternate Function Select Bit Bits EXT[5] (SYS_P2_MFP[21]), ALT[5] (SYS_P2_MFP[13]), and MFP[5] (SYS_P2_MFP[5]) determine the P2.5 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = UART1_TXD function is selected. (0, 1, 0) = PWM0_CH3 function is selected. (1, 0, 1) = LIMT_Q function is selected. Others: GPIO function is selected.
[12]	ALT[4]	P2.4 Alternate Function Select Bit Bits EXT[4] (SYS_P2_MFP[20]), ALT[4] (SYS_P2_MFP[12]), and MFP[4] (SYS_P2_MFP[4]) determine the P2.4 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = UART1_RXD function is selected. (0, 1, 0) = PWM0_CH2 function is selected. (1, 0, 1) = LIMT_I function is selected. Others: GPIO function is selected.
[11]	ALT[3]	P2.3 Alternate Function Select Bit Bits EXT[3] (SYS_P2_MFP[19]), ALT[3] (SYS_P2_MFP[11]), and MFP[3] (SYS_P2_MFP[3]) determine the P2.3 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = UART2_RXD function is selected. (0, 1, 0) = PWM0_CH1 function is selected. (1, 0, 1) = I2C0_SDA function is selected. Others: GPIO function is selected.
[10]	ALT[2]	P2.2 Alternate Function Select Bit Bits EXT[2] (SYS_P2_MFP[18]), ALT[2] (SYS_P2_MFP[10]), and MFP[2] (SYS_P2_MFP[2]) determine the P2.2 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = UART2_TXD function is selected. (0, 1, 0) = PWM0_CH0 function is selected. (1, 0, 1) = I2C0_SCL function is selected. Others: GPIO function is selected.
[9]	ALT[1]	P2.1 Alternate Function Select Bit Bits EXT[1] (SYS_P2_MFP[17]), ALT[1] (SYS_P2_MFP[9]), and MFP[1] (SYS_P2_MFP[1]) determine the P2.1 function. (0, 0, 0) = GPIO function is selected. Others: GPIO function is selected.
[8]	ALT[0]	P2.0 Alternate Function Select Bit Bits EXT[0] (SYS_P2_MFP[16]), ALT[0] (SYS_P2_MFP[8]), and MFP[0] (SYS_P2_MFP[0]) determine the P2.0 function. (0, 0, 0) = GPIO function is selected.

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		(0, 1, 0) = INT2 function is selected. Others: GPIO function is selected.
[7:0]	MFP[7:0]	P2 Multiple Function Select Bit The pin function of P2 depends on MFP and ALT. Refer to ALT Description for details.

4.1.6.4 Multiple Function Port3 Control Register (SYS_P3_MFP)

Register	Offset	R/W	Description	Reset Value
SYS_P3_MFP	SYS_BA+0x0C	R/W	P3 Multiple Function and Input Type Control Register	0x0000_0000

Bits	Description	
[31:16]	Reserved	Reserved.
[23:16]	EXT[7:0]	P3 Extend Function Select Bit The pin function of P0 depends on MFP and ALT and EXT. Refer to ALT Description for details.
[15]	Reserved	Reserved.
[14]	ALT[6]	P3.6 Alternate Function Select Bit Bits EXT[6] (SYS_P3_MFP[22]), ALT[6] (SYS_P3_MFP[14]), and MFP[6] (SYS_P3_MFP[6]) determine the P3.6 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = TM1_EXT or TM1 function is selected. Others: GPIO function is selected.
[13]	ALT[5]	P3.5 Alternate Function Select Bit Bits EXT[5] (SYS_P3_MFP[21]), ALT[5] (SYS_P3_MFP[13]), and MFP[5] (SYS_P3_MFP[5]) determine the P3.5 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = TM1_CNT_OUTfunction is selected. (0, 1, 0) = I2C0_SCL function is selected. (0, 1, 1) = UART3_RXD function is selected. (1, 0, 1) = flash_strobe function is selected. Others: GPIO function is selected.
[12]	ALT[4]	P3.4 Alternate Function Select Bit Bits EXT[4] (SYS_P3_MFP[20]), ALT[4] (SYS_P3_MFP[12]), and MFP[4] (SYS_P3_MFP[4]) determine the P3.4 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = TM0_CNT_OUT function is selected. (0, 1, 0) = I2C0_SDA function is selected. (0, 1, 1) = UART3_TXD function is selected. Others: GPIO function is selected.
[11]	Reserved	Reserved.
[10]	ALT[2]	P3.2 Alternate Function Select Bit Bits EXT[2] (SYS_P3_MFP[18]), ALT[2] (SYS_P3_MFP[10]), and MFP[2] (SYS_P3_MFP[2])

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		determine the P3.2 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = INT0 function is selected. (0, 1, 0) = TM0_EXT or TM0 function is selected (0, 1, 1) = STADC function is selected. Others: GPIO function is selected.
[9]	ALT[1]	P3.1 Alternate Function Select Bit The pin function of P3.1 depends on P3_MFP[1] and P3_ALT[1]. Bits EXT[1] (SYS_P3_MFP[17]), ALT[1] (SYS_P3_MFP[9]), and MFP[1] (SYS_P3_MFP[1]) determine the P3.1 function. (0, 0, 0) = GPIO function is selected. (0, 1, 1) = ADC_CH7 function is selected. Others: GPIO function is selected.
[8]	ALT[0]	P3.0 Alternate Function Select Bit Bits EXT[0] (SYS_P3_MFP[16]), ALT[0] (SYS_P3_MFP[8]), and MFP[0] (SYS_P3_MFP[0]) determine the P3.0 function. (0, 0, 0) = GPIO function is selected. (0, 1, 1) = ADC_CH6 function is selected. Others: GPIO function is selected.
[7:0]	MFP[7:0]	P3 Multiple Function Select Bits The pin function of P3 depends on MFP and ALT. Refer to ALT Description for details.

4.1.6.5 Multiple Function Port4 Control Register (SYS_P4_MFP)

Register	Offset	R/W	Description	Reset Value
SYS_P4_MFP	SYS_BA+0x10	R/W	P4 Multiple Function and Input Type Control Register	0x0000_00C0

Bits	Description	
[31:24]	Reserved	Reserved.
[23:16]	EXT[7:0]	P4 Extend Function Select Bit The pin function of P0 depends on MFP and ALT and EXT. Refer to ALT Description for details.
[15]	ALT[7]	P4.7 Alternate Function Select Bit Bits EXT[7] (SYS_P4_MFP[23]), ALT[7] (SYS_P4_MFP[15]), and MFP[7] (SYS_P4_MFP[7]) determine the P4.7 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = ICE_DAT function is selected. (0, 1, 0) = UART1_TXD function is selected. (0, 1, 1) = I2C0_SDA function is selected. (1, 0, 1) = flash_clk function is selected. Others: GPIO function is selected.
[14]	ALT[6]	P4.6 Alternate Function Select Bit Bits EXT[6] (SYS_P4_MFP[22]), ALT[6] (SYS_P4_MFP[14]), and MFP[6] (SYS_P4_MFP[6])

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		determine the P4.6 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = ICE_CLK function is selected. (0, 1, 0) = UART1_RXD function is selected. (0, 1, 1) = I2C0_SCL function is selected. (1, 0, 1) = flash_dat function is selected. Others: GPIO function is selected.
[13:8]	Reserved	Reserved.
[7:0]	MFP[7:0]	P4 Multiple Function Select Bits The pin function of P4 depends on MFP and ALT. Refer to ALT Description for details.

4.1.6.6 Multiple Function Port5 Control Register (SYS_P5_MFP)

Register	Offset	R/W	Description	Reset Value
SYS_P5_MFP	SYS_BA+0x14	R/W	P5 Multiple Function and Input Type Control Register	0x0000_0000

Bits	Description	
[31:24]	Reserved	Reserved.
[23:16]	EXT[7:0]	P5 Extend Function Select Bit The pin function of P0 depends on MFP and ALT and EXT. Refer to ALT Description for details.
[15]	ALT[7]	P5.7 Alternate Function Select Bit Bits EXT[7] (SYS_P5_MFP[23]), ALT[7] (SYS_P5_MFP[15]), and MFP[7] (SYS_P5_MFP[7]) determine the P5.7 function. (0, 0, 0) = GPIO function is selected. (0, 1, 0) = I2C0_SDA function is selected. (0, 1, 1) = PWM0_CH7 function is selected. (1, 1, 1) = UART0_TXD is selected. Others: GPIO function is selected.
[14]	ALT[6]	P5.6 Alternate Function Select Bit Bits EXT[6] (SYS_P5_MFP[22]), ALT[6] (SYS_P5_MFP[14]), and MFP[6] (SYS_P5_MFP[6]) determine the P5.6 function. (0, 0, 0) = GPIO function is selected. (0, 1, 0) = I2C0_SCL function is selected. (0, 1, 1) = PWM0_CH6 function is selected. (1, 1, 1) = UART0_RXD is selected. Others: GPIO function is selected.
[13]	ALT[5]	P5.5 Alternate Function Select Bit Bits EXT[5] (SYS_P5_MFP[21]), ALT[5] (SYS_P5_MFP[13]), and MFP[5] (SYS_P5_MFP[5]) determine the P5.5 function. (0, 0, 0) = GPIO function is selected. (0, 1, 0) = SPI0_SS function is selected. (0, 1, 1) = PWM0_CH5 function is selected.

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		(1, 0, 1) = TADC_CLK function is selected. (1, 1, 0) = PWM0_CH2 function is selected. (1, 1, 1) = UART0_TXD function is selected. Others: GPIO function is selected.
[12]	ALT[4]	P5.4 Alternate Function Select Bit Bits EXT[4](SYS_P5_MFP[20]), ALT[4](SYS_P5_MFP[12]), and MFP[4](SYS_P5_MFP[4]) determine the P5.4 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = TM0_CNT_OUT function is selected. (0, 1, 0) = TADC_DATL function is selected. (0, 1, 1) = SPI0_MOSI function is selected. Others: GPIO function is selected.
[11]	ALT[3]	P5.3 Alternate Function Select Bit Bits EXT[3] (SYS_P5_MFP[19]), ALT[3] (SYS_P5_MFP[11]), and MFP[3] (SYS_P5_MFP[3]) determine the P5.3 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = ADC_CH0 function is selected. (0, 1, 1) = SPI0_MISO function is selected. Others: GPIO function is selected.
[10]	ALT[2]	P5.2 Alternate Function Select Bit Bits EXT[2] (SYS_P5_MFP[18]), ALT[2] (SYS_P5_MFP[10]), and MFP[2] (SYS_P5_MFP[2]) determine the P5.2 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = INT1 function is selected. Others: GPIO function is selected.
[9]	ALT[1]	P5.1 Alternate Function Select Bit Bits EXT[1] (SYS_P5_MFP[17]), ALT[1] (SYS_P5_MFP[9]), and MFP[1] (SYS_P5_MFP[1]) determine the P5.1 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = PWM0_CH6 function is selected. (0, 1, 1) = UART0_RXD function is selected. (1, 0, 1) = I2C0_SCL function is selected. Others: GPIO function is selected.
[8]	ALT[0]	P5.0 Alternate Function Select Bit Bits EXT[0] (SYS_P5_MFP[16]), ALT[0] (SYS_P5_MFP[8]), and MFP[0] (SYS_P5_MFP[0]) determine the P5.0 function. (0, 0, 0) = GPIO function is selected. (0, 0, 1) = PWM0_CH7 function is selected. (0, 1, 1) = UART0_TXD function is selected. (1, 0, 1) = I2C0_SDA function is selected. Others: GPIO function is selected.
[7:0]	MFP[7:0]	P5 Multiple Function Select Bits The pin function of P5 depends on MFP and ALT. Refer to ALT Description for details.

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4.1.6.7 Register-Write-Protection Control Register (SYS_REGLCTL)

Some of the system control registers need to be protected to avoid inadvertent write which disturbs the chip operation. These system control registers will be protected after power on reset until the register protection is disabled by the user. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data 0x59, 0x16, 0x88 to the register SYS_REGLCTL address at 0x5000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

After the protection is disabled, the user can check the protection disable bit at address 0x4004_0040 bit 0 (1 is protection disable, 0 is protection enable). User can update the target protected register value and then write any data to the address 0x4004_0040 to enable the register protection.

The REGLCTL status can be get by writing this register to disable/enable register protection, and reading it

Register	Offset	R/W	Description	Reset Value
SYS_REGLCTL	SYS_BA+0x40	R/W	Register-Write-Protection Control Register	0x0000_0000

Bits	Description	
[31:8]	Reserved	Reserved.
[7:0]	REGLCTL	Register Write-protection Code (Write Only) Some registers have write-protection function. To write these registers, these registers should be disabled by writing the sequence value 0x59, 0x16, 0x88 to this field. After this sequence is completed, the REGLCTL bit will be set to 1 and write-protection registers can be normally written. Register Write-protection Disable Index (Read Only) 0 = Write-protection is enabled for write-protected registers. Any writing to the protected register is ignored. 1 = Write-protection is disabled for write-protected registers. Protected registers are listed below:

Register	Address	Note
WDT_CTL	0x4000_6000	Watchdog Timer Control
WDT_ALTCTL	0x4000_6004	Watchdog Timer Alternative Control
RCC_IPRST0	0x4004_0004	Peripheral Reset Control Register 0
CLK_AHB_SEL	0x4004_0050	AHB Clock Source Select Control
CLK_APB_SEL	0x4004_0054	Bit0,bit1 wdtsel wwdtsel

Note: The bits which are write-protected will be noted as" (Write Protect)" beside the description.

4.1.6.8 Register to reflect the status of ROM Mode (SYS_STATUS)

Register	Offset	R/W	Description	Reset Value
SYS_ STATUS	SYS_BA+0x44	R/W	Register to reflect the status of ROM Mode	0x0000_0000

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Bits	Description	
[31:9]	Reserved	Reserved.
[8]	Flash_test_en	Flash CP test enable bit. 1 = Flash CP test enabled 0 = Flash CP test disabled
[7:0]	STATUS	Register to reflect the status of ROM Mode(Read Only) 0xA5,0xA6,0xA7,0xA8,0xA9: ROM Mode Others: Flash Mode Note: the value of this register reflects the command that Host has issued, when PAD_NRST is active low, host transmits command by P4.6 and P4.7.

4.1.7 System Timer (SysTick)

The PAN2025MCU includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock edge, and then decrement on subsequent clocks. When the counter transforms to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN after reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer to count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained as zero after reloaded. This mechanism can be used to disable the feature independently from the timer enable bit.

4.1.7.1 System Timer Control Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
SCS Base Address: **SCS_BA = 0xE000_E000**				
SYST_CTRL	SCS_BA+0x10	R/W	SysTick Control and Status Register	0x0000_0000
SYST_LOAD	SCS_BA+0x14	R/W	SysTick Reload Value Register	0x00XX_XXXX
SYST_VAL	SCS_BA+0x18	R/W	SysTick Current Value Register	0x00XX_XXXX

4.1.7.2 System Timer Control Register

4.1.7.2.1. SysTick Control and Status Register (SYST_CTRL)

Register	Offset	R/W	Description	Reset Value
SYST_CTRL	SCS_BA+0x10	R/W	SysTick Control and Status Register	0x0000_0000

Bits	Description

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[31:17]	Reserved	Reserved.
[16]	COUNTFLAG	System Tick Counter Flag Returns 1 if timer counted to 0 since last time this register was read. COUNTFLAG is set by a count transition from 1 to 0. COUNTFLAG is cleared on read or by a write to the Current Value register.
[15:3]	Reserved	Reserved.
[2]	CLKSRC	System Tick Clock Source Select Bit 0 = Clock source is optional, refer to STCLKSEL. 1 = Core clock used for SysTick timer.
[1]	TICKINT	System Tick Interrupt Enable Bit 0 = Counting down to 0 does not cause the SysTick exception to be pended. Software can use COUNTFLAG to determine if a count to 0 has occurred. 1 = Counting down to 0 will cause the SysTick exception to be pended. Clearing the SysTick Current Value register written by a register in software will not cause SysTick to be pended.
[0]	ENABLE	System Tick Counter Enable Bit 0 = Counter disabled. 1 = Counter enabled and will operate in a multi-shot manner.

4.1.7.2.2. SysTick Reload Value Register (SYST_LOAD)

Register	Offset	R/W	Description	Reset Value
SYST_LOAD	SCS_BA+0x14	R/W	SysTick Reload Value Register	0x00XX_XXXX

Bits	Description	
[31:24]	Reserved	Reserved.
[23:0]	RELOAD	System Tick Reload Value Value to be load into the Current Value register when the counter is 0.

4.1.7.2.3. SysTick Current Value Register (SYST_VAL)

Register	Offset	R/W	Description	Reset Value
SYST_VAL	SCS_BA+0x18	R/W	SysTick Current Value Register	0x00XX_XXXX

Bits	Description	
[31:24]	Reserved	Reserved.
[23:0]	CURRENT	System Tick Current Value Current counter value. This is the value of the counter at the time it is sampled. The counter does not provide read-modify-write protection. The register is write-clear. A software write of any value will clear the register to 0. Unsupported bits RAZ (see SysTick Reload Value Register). Any value written by a software will clear the register. RAZ are unsupported bits. (Refer to SysTick Reload Value Register).

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4.1.8 System Control Block Registers (SCB)

The PAN2025MCU status and operating mode control are managed by System Control Block Registers. Including CPUID, PAN2025MCU interrupt priority and PAN2025MCU power management can be controlled by these system control registers.

4.1.8.1 System Control Block Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
SCS Base Address: **SCS_BA = 0xE000_E000**				
SCS_CPUID	SCS_BA+0xD00	R	CPUID Base Register	0x410C_C200
SCS_ICSR	SCS_BA+0xD04	R/W	Interrupt Control State Register	0x0000_0000
SCS_AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000
SCS_SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000
SCS_SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000
SCS_SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

4.1.8.2 System Control Block Register Description

4.1.8.2.1. CPUID Base Register (SCS_CPUID)

Register	Offset	R/W	Description	Reset Value
SCS_CPUID	SCS_BA+0xD00	R	CPUID Base Register	0x410C_C200

Bits	Description	
[31:24]	IMPLEMENTER	Implementer Code Implementer code assigned by M0_core.
[23:20]	Reserved	Reserved.
[19:16]	PART	Architecture of the Processor Read as 0xC for M0_core parts.
[15:4]	PARTNO	Part Number of the Processor Read as 0xC20.
[3:0]	REVISION	Revision Number Read as 0x0.

4.1.8.2.2. Interrupt Control State Register (SCS_ICSR)

Register	Offset	R/W	Description	Reset Value
SCS_ICSR	SCS_BA+0xD04	R/W	Interrupt Control State Register	0x0000_0000

Bits	Description

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[31]	NMIPENDSET	NMI Set-pending Bit Write Operation: 0 = No effect. 1 = Change NMI exception state to pending. Read Operation: 0 = NMI exception is not pending. 1 = NMI exception is pending. **Note**: Because NMI is the highest-priority exception, normally the processor enters the NMI exception handler as soon as it detects a writing of 1 to this bit. Enter the handler then clear this bit to 0. This means a read of this bit by the NMI exception handler returns 1 only if the NMI signal is reasserted while the processor is executing that handler.
[30:29]	Reserved	Reserved.
[28]	PENDSVSET	PendSV Set-pending Bit Write Operation: 0 = No effect. 1 = Change PendSV exception state to pending. Read Operation: 0 = PendSV exception is not pending. 1 = PendSV exception is pending. **Note**: Writing 1 to this bit is the only way to set the PendSV exception state to pending.
[27]	PENDSVCLR	PendSV Clear-pending Bit Write Operation: 0 = No effect. 1 = Remove the pending state from the PendSV exception. **Note**: This bit is write-only. To clear the PENDSV bit, you must “write 0 to PENDSVSET and write 1 to PENDSVCLR” at the same time.
[26]	PENDSTSET	SysTick Exception Set-pending Bit Write Operation: 0 = No effect. 1 = Changes SysTick exception state to pending. Read Operation: 0 = SysTick exception is not pending. 1 = SysTick exception is pending.
[25]	PENDSTCLR	SysTick Exception Clear-pending Bit Write Operation: 0 = No effect. 1 = Remove the pending state from the SysTick exception. **Note**: This bit is write-only. To clear PENDST bit, “write 0 to PENDSTSET “ and “write 1 to PENDSTCLR” at the same time.
[24]	Reserved	Reserved.
[23]	ISRPREEMPT	Interrupt Preemption Bit (Read-only) If set, a pending exception will be served on exit from the debug halt state.

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[22]	ISRPENDING	Interrupt Pending Flag, excluding NMI and Faults (Read-only) 0 = Interrupt not pending. 1 = Interrupt pending.
[21]	Reserved	Reserved.
[20:12]	VECTPENDING	Exception Number of the Highest Priority Pending Enabled Exception (Read-only) 0 = No pending exceptions. Non-zero = Exception number of the highest priority pending enabled exception.
[11:9]	Reserved	Reserved.
[8:0]	VECTACTIVE	Contains the Active Exception Number (Read-only) 0 = Thread mode. Non-zero = Exception number of the currently active exception.

4.1.8.2.3. Application Interrupt and Reset Control Register (SCS_AIRCR)

Register	Offset	R/W	Description	Reset Value
SCS_AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000

Bits	Description	
[31:16]	VECTORKEY	Register Access Key Write Operation: When writing to this register, the VECTORKEY field needs to be set to 0x05FA, otherwise the write operation would be ignored. The VECTORKEY filed is used to prevent accidental writing to this register from resetting the system or clearing of the exception status. Read Operation: Read as 0xFA05.
[15:3]	Reserved	Reserved.
[2]	SYSRESETREQ	System Reset Request Writing 1 to this bit will cause a reset signal to be asserted to the chip to indicate a reset is requested. The bit is a write-only bit and is self-cleared as part of the reset sequence.
[1]	VECTCLRACTIVE	Exception Active Status Clear Bit Reserved for debug. When writing to the register, the user must write 0 to this bit, otherwise the following behavior is unpredictable.
[0]	Reserved	Reserved.

4.1.8.2.4. System Control Register (SCS_SCR)

Register	Offset	R/W	Description	Reset Value
SCS_SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000

Bits	Description	
[31:5]	Reserved	Reserved.

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[4]	SEVONPEND	Send Event on Pending Bit 0 = Only enabled interrupts or events can wake-up the processor, disabled interrupts are excluded. 1 = Enabled events and all interrupts, including disabled interrupts, can wake-up the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects next WFE. The processor also wakes up on execution of an SEV instruction or an external event.
[3]	Reserved	Reserved.
[2]	SLEEPDEEP	Processor Deep Sleep and Sleep Mode Selection Controls the processor to select sleep or deep sleep in low power mode: 0 = Sleep mode. 1 = Deep Sleep mode.
[1]	SLEEPONEXIT	Sleep-on-exit Enable This bit indicates sleep-on-exit when returning from Handler mode to Thread mode: 0 = Do not sleep when returning to Thread mode. 1 = Enter sleep, or deep_sleep, when returning from ISR to Thread mode. Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.
[0]	Reserved	Reserved.

4.1.8.2.5. System Handler Priority Register 2 (SCS_SHPR2)

Register	Offset	R/W	Description	Reset Value
SCS_SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000

Bits	Description	
[31:30]	PRSH_11	Priority of System Handler 11 – SVCall 0 denotes the highest priority and 3 denotes the lowest priority.
[29:0]	Reserved	Reserved.

4.1.8.2.6. System Handler Priority Register 3 (SCS_SHPR3)

Register	Offset	R/W	Description	Reset Value
SCS_SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

Bits	Description	
[31:30]	PRSH_15	Priority of System Handler 15 – SysTick 0 denotes the highest priority and 3 denotes the lowest priority.
[29:24]	Reserved	Reserved.
[23:22]	PRSH_14	Priority of System Handler 14 – PendSV 0 denotes the highest priority and 3 denotes the lowest priority.
[21:0]	Reserved	Reserved.

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4.2 Reset and Clock Controller(RCC)

4.2.1 Overview

The RCC module can implement reset function and generate clocks for the whole chip, including system clocks and all peripheral clocks. In regard to the reset function, chip waits for wake-up interrupt source to exit Power-down mode. In Power-down mode, the clock controller turns off the 16MHz external high speed crystal (HXT) to reduce the overall system power consumption.

4.2.2 Reset

PAN2025 reset source includes:

1. Power-on reset (POR)
2. Pin reset (nRESET)
3. Low voltage reset (LVR, BOD)
4. CPU requset reset
5. WDT and WWDT Time-out Reset (WDT/WWDT Reset)
6. MCU reset
7. Each module reset

Number 1 and 2 can reset the whole digital system including the low power mode module. Number 3~5 can reset the system except the low power mode module. Number 6 and 7 can reset each single module.

4.2.2.1 Power-On Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PINRF (SYS_RSTSTS[1]) will be set to 1 to indicate there is a POR reset event. The PINRF (SYS_RSTSTS[1]) bit can be cleared by writing 1 to it. Figure 4-3 shows the waveform of Power-On reset.

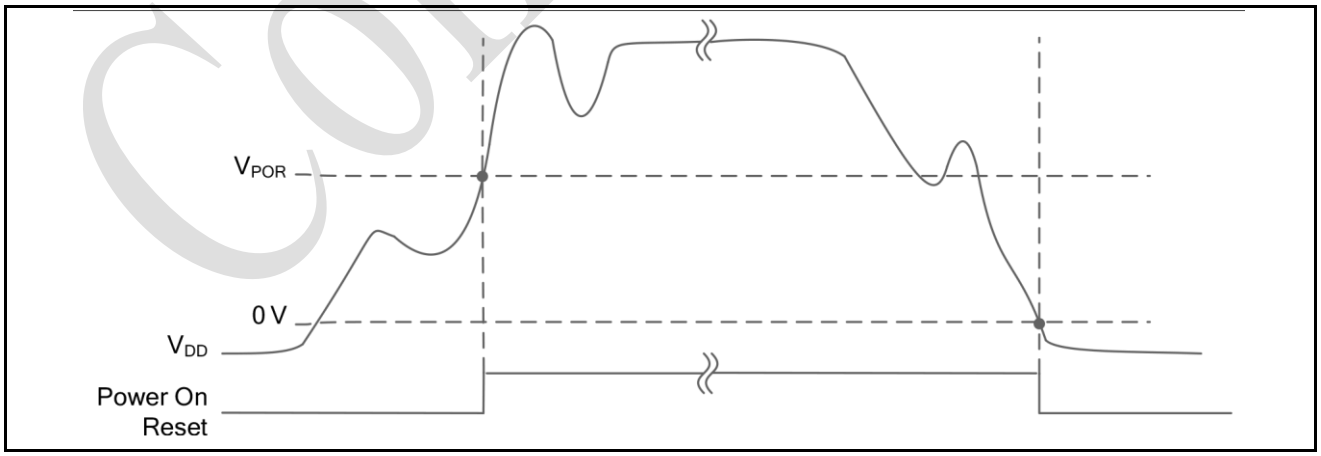

Figure 4-3 Power-on Reset (POR) Waveform

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4.2.2.2 Low Voltage Reset (LVR)

Low Voltage Reset detects AVDD during system operation. When the AVDD voltage is lower than VLVR and the state keeps longer than De-glitch time (see SYS_BLDBCTL register), chip will be reset. The LVR reset will control the chip in reset state until the AVDD voltage rises above VLVR and the state keeps longer than De-glitch time. The PINRF (SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 4-4 shows the Low Voltage Reset waveform.

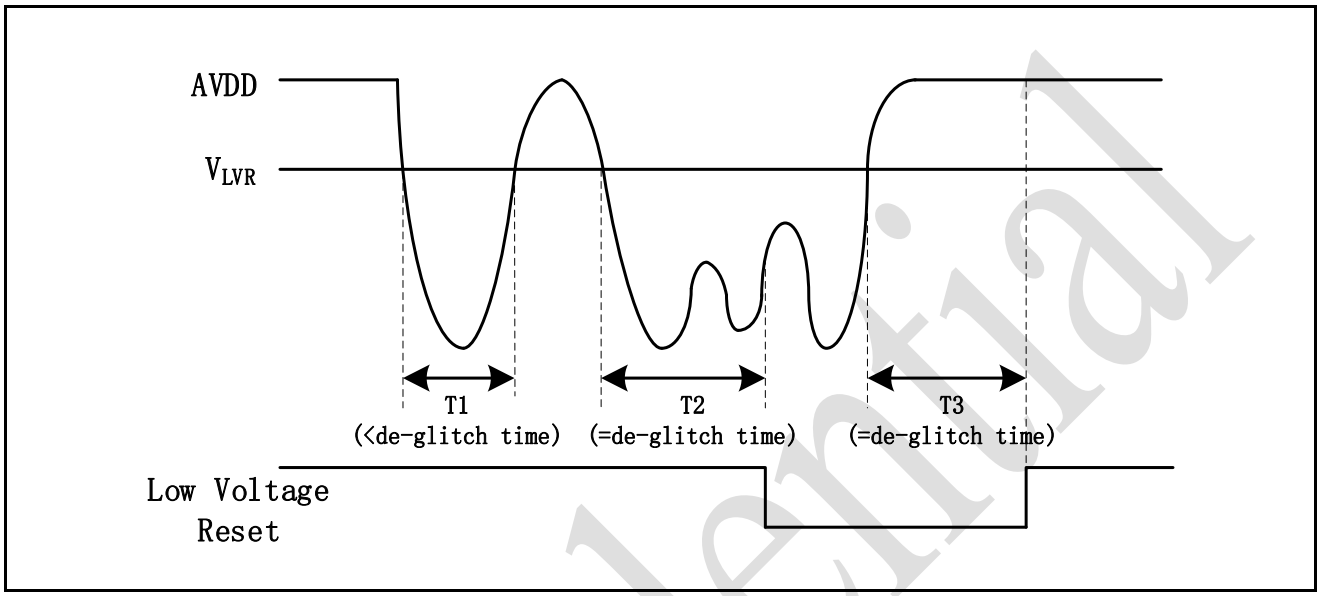

Figure 4-4 Low Voltage Reset (LVR) Waveform

4.2.2.3 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (ANAC_RCCCTL [24]), Brown-Out Detector function will detect AVDD during system operation. When the AVDD voltage is lower than VBOD which is decided by BODEN (ANAC_RCCCTL [24]) and BODVL (ANAC_RCCCTL [26:25]) and the state keeps longer than De-glitch time (see SYS_BLDBCTL register), chip will be reset. The BOD reset will control the chip in reset state until the AVDD voltage rises above VBOD and the state keeps longer than De-glitch time. The default value of BODEN, BODVL and BODRSTEN is set by flash controller user configuration register CBOVEXT (CONFIG0[23]), CBOV (CONFIG0[22:21]) and CBORST (CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 4-5 shows the Brown-Out Detector waveform.

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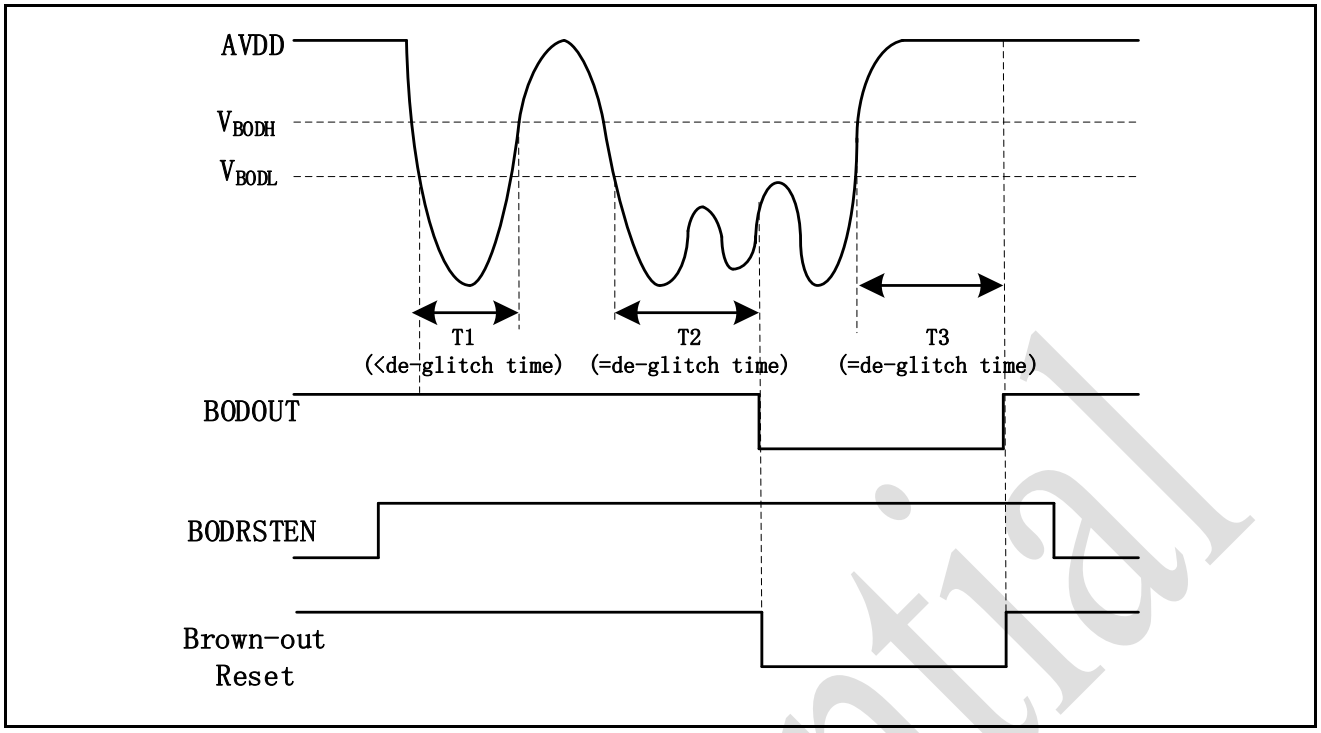

Figure 4-5 Brown-out Detector (BOD) Waveform

4.2.3 Clock Controller

The analog clock generator consists of 6 clocks as listed below:

- 16MHz external crystal oscillator (HXT)
- 32KHz internal low speed RC oscillator (RCL) (Used in low power mode or 1.5V digital region)
- 16 MHz internal high speed RC oscillator (RCH)
- Clock for internal AHB (CPU) (MCU_DPLL)
- Clock for MODEM (RF_DPLL)
- SWD clock (default as GPIO P46)

All clocks of the system are divided into two categories:

- Providing clocks to the CPU and the corresponding AHB/APB bus;
  - 16MHz external crystal oscillator (HXT)
  - 16MHz internal high speed RC oscillator (RCH)
  - Clock for internal AHB (CPU) (MCU_DPLL)
- Providing clocks for specific IPs
  - 32KHz internal low speed RC oscillator (RCL)
  - 16MHz internal high speed RC oscillator (RCH)
  - 16MHz external crystal oscillator (HXT)
  - Clock for MODEM (RF_DPLL)

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4.2.4 Clock Block Diagram

As shown in Figure 4-6, digital system clock source includes RCH, HXT, RF_DPLL, MCU_DPLL and RCL. The digital clock source is composed of RCH, HXT and MCU_DPLL. RCH is configured as the default clock once powered on.

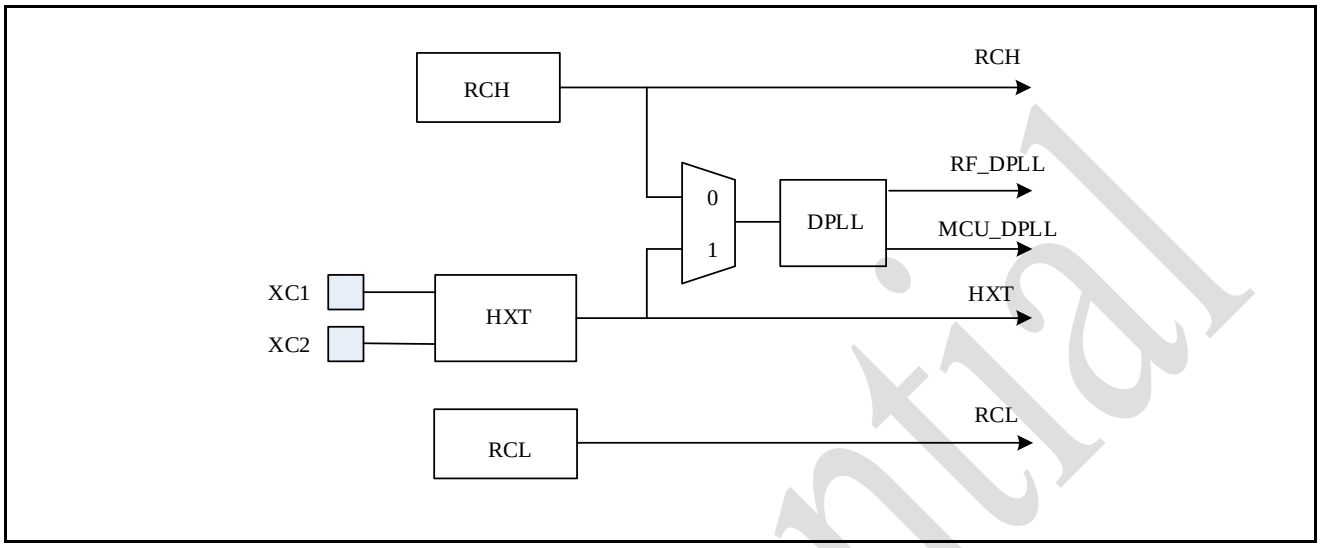

Figure 4-6 Clock Generator Block Diagram

4.2.5 System Clock

The system clock(SYS_CLK) has 3 clock sources which were generated by clock generator block. The clock source switch depends on the register AHB_CLK_SEL (CLK_AHB_SEL0[1:0]). ST_CLK, APB1_CLK, APB2_CLK and AHB_CLK are generated based on SYS_CLK.

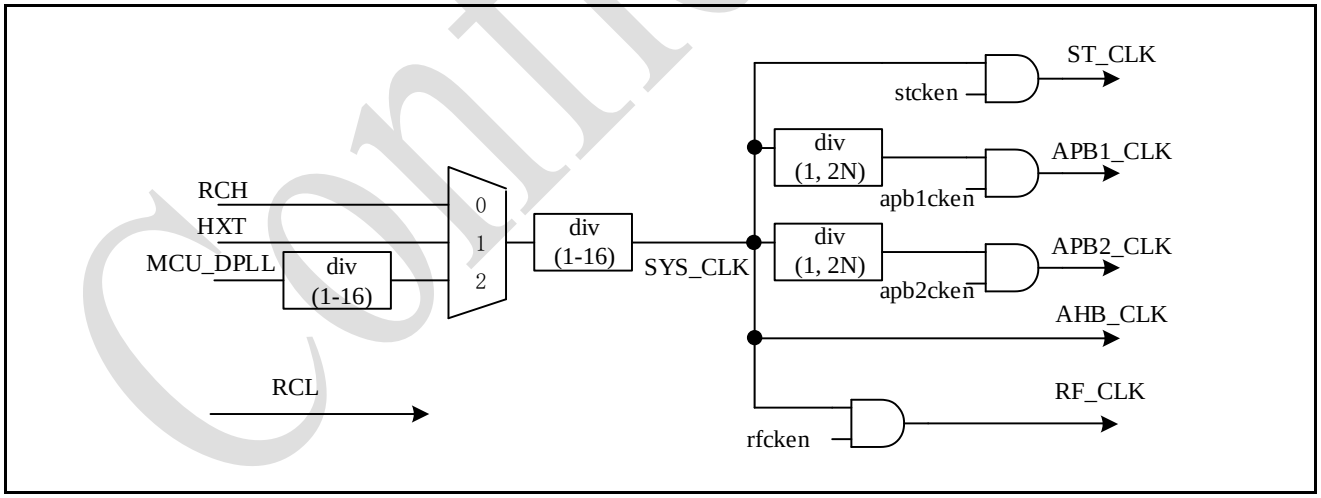

Figure 4-7 System Clock and SysTick Block Diagram

4.2.6 Peripherals Clock Source Selection

The peripheral clock has different clock source and the switch settings depends on different peripherals. Please to note that, while switching clock source from one to another, the user must wait until both clock sources are running stably.

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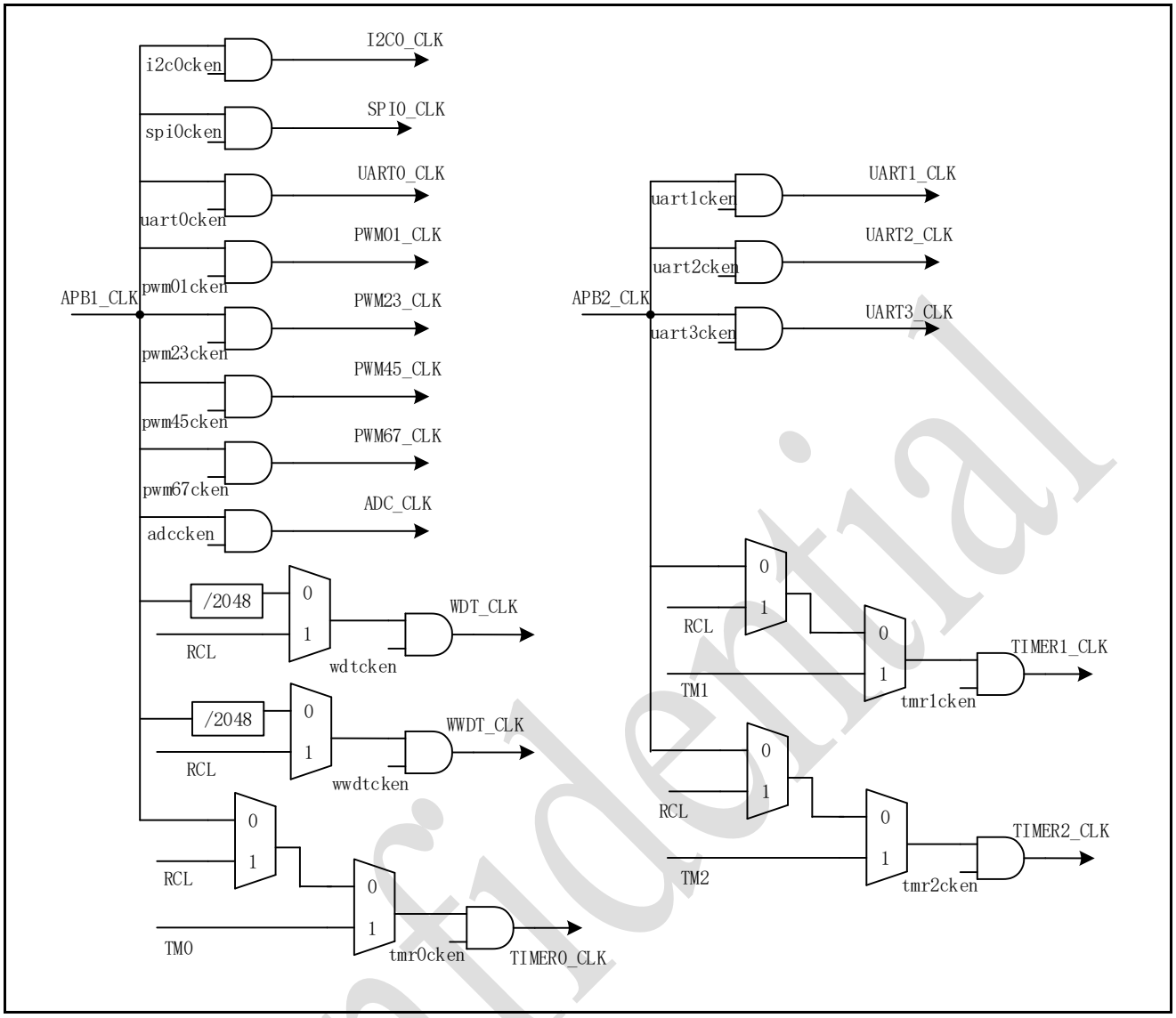

Figure 4-8 APB Peripheral Clock

4.2.7 APB Clock Domain Peripherals

In PAN2025, there are two groups of APB, APB1_CLK and APB2_CLK. The basic clock is AHB_CLK.

The peripheral clock has different clock sources and the switch settings depend on different peripherals. Please refer to APB1 Devices Clock Enable Control Register (CLK_APB1_EN) and APB2 Devices Clock Enable Control Register (CLK_APB2_EN) in section 5.2.7. Please to note that, while switching clock source from one to another, user must wait until both clock sources are running stably.

Table 4-3 Peripheral Clock Source Selection Table

	APB1_CLK / 2048	RCL	APB1_CLK	APB2_CLK
WDT	Yes	Yes	-	-
WWDT	Yes	Yes	-	-
TMR0	-	Yes	Yes	No

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TMR1	-	Yes	Yes	No
TMR2	-	Yes	Yes	No
I2C0	-	-	Yes	No
SPI0	-	-	Yes	No
UART0	-	-	Yes	No
UART1	-	-	No	Yes
UART2	-	-	No	Yes
UART3	-	-	No	Yes
PWM01	-	-	Yes	No
PWM23	-	-	Yes	No
PWM45	-	-	Yes	No
PWM67	-	-	Yes	No
ADC	-	-	Yes	No

4.2.8 Clock Control Process

4.2.8.1 AHB/CPU clock

There are three clock sources for the CPU: RCH, HXT, and MCU_DPLL. RCH is used when the system is powerd on, MCU_DPLL is used when the chip is in normal operation. The reference clock of MCU_DPLL can be RCH or HXT. The clock switching process is listed as follow:

1. Enable Crystal oscillator
   reg_sync_3v (LP_REG_SYNC[0]) is set,
   Waiting for synchronization to complete,
   After the oscillator works stable, Hxt16_stb (CLK_STB_STATUS[2]) is set 1.
2. Switch the DPLL's reference clock to a crystal oscillator
   DPLL_CLK_SEL(LP_MISC[0]) is set
   reg_sync_3v (LP_REG_SYNC[0]) is set
   Waiting for synchronization to complete.
3. Enable MCU_DPLL
   EN_DPLL (LP_FL_CTRL1[6]) is set
   reg_sync_3v (LP_REG_SYNC[0]) is set
   Waiting for synchronization to complete,
   After the oscillator works stable, mcu_dpll_stb (CLK_STB_STATUS[3]) is set 1.
4. Switch AHB/APB clock to a MCU_DPLL
   AHB_CLK_SEL (CLK_AHB_SEL [1:0]) is set to 10
5. Close RCH: RCH need to be closed when RF is transmitting/receiving data
   RC_16M_CTRL (LP_MISC[1]) is set to 0
   EN_RC_16M (LP_FL_CTRL1[5]) is set to 0
   Waiting for synchronization to complete.

4.2.8.2 RF clock

The RF module has three clocks: the AHB bus clock RF_CLK, the transceiver module HXT and RF_DPLL. RF_DPLL and MCU_DPLL are two different outputs of the same DPLL, so the start process of RF_DPLL is the same as MCU_DPLL. rfcken(CLK_AHB_EN[16]) is the enable signal

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for both RF_DPLL and RCH. HXT is the source of RCH.

4.2.8.3 APB1/APB2 and peripheral clock

APB1_CLK and APB2_CLK are the 2N frequency division of AHB_CLK. apb1cken (CLK_APB1_EN[12]) and apb2cken(CLK_APB2_EN[11]) are respectively the enable signal for APB1 and APB2. When apb2cken(CLK_APB2_EN[11]) is set to 0, all the peripheral clocks of APB2 are off. Othewise, the peripherals are controlled by the respective enable control bits. APB1_CLK is the same as APB2_CLK.

4.2.9 RCC Register Map

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
RCC Base Address: **RCC_BA = 0x4004_0000**				
RSTSTS	RCC_BA+0x00	R/W	System Reset Status Register	0x0000_0002
IPRST0	RCC_BA+0x04	R/W	Peripheral Reset Control Register 0	0x0000_0000
IPRST1	RCC_BA+0x08	R/W	Peripheral Reset Control Register 1	0x0000_0000
BODCTL	RCC_BA+0x0C	R/W	Brown-out Detector Control Register	0x0000_0040
BLDBCTL	RCC_BA+0x10	R/W	BOD LVR De-Bounce Control Register	0x0000_2020
CLK_WKUP_0	RCC_BA+0x40	R/W	Clock Wake Up Stable Timing Control Register0	0x0840_0840
CLK_WKUP_1	RCC_BA+0x44	R/W	Clock Wake Up Stable Timing Control Register1	0x0040_4040
CLK_DIV_0	RCC_BA+0x48	R/W	Clock Divider Control register0	0x0001_0000
CLK_DIV_1	RCC_BA+0x4C	R/W	Clock Divider Control register1	0x0000_0000
CLK_AHB_SEL	RCC_BA+0x50	R	AHB Clock Source Select Control	0x0000_0000
CLK_APB_SEL	RCC_BA+0x54	R/W	APB Peripherals Clock Source Select Control	0x0000_0000
CLK_AHB_EN	RCC_BA+0x58	R/W	AHB Clock Enable Control	0x0002_0002
CLK_APB1_EN	RCC_BA+0x5C	R/W	APB1 Clock Enable Control	0x0000_0000
CLK_APB2_EN	RCC_BA+0x60	R/W	APB2 Clock Enable Control	0x0000_0000
CLK_STB_STATUS	RCC_BA+0x64	R	Clock Stable Signal	0x0000_0003

4.2.10 RCC Register Description

4.2.10.1 System Reset Status Register (RSTSTS)

Register	Offset	R/W	Description	Reset Value
RSTSTS	RCC_BA+0x00	R/W	System Reset Status Register	0x0000_0002

Bits	Description	
[31:8]	Reserved	Reserved.
[7]	CPURF	CPU Reset Flag The CPU reset flag is set by hardware if software writes 1 to CPURST (IPRST0[1]) to reset MCU and Flash Memory Controller (FMC). 0 = No reset from CPU.

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		1 = The MCU and FMC are reset by software setting CPURST to 1. Note: Software can write 1 to clear this bit.
[6]	Reserved	Reserved.
[5]	SYSRF	System Reset Flag The system reset flag is set by the “Reset Signal” from the MCU to indicate the previous reset source. 0 = No reset from MCU 1 = The MCU had issued the reset signal to reset the system by writing 1 to the bit SYSRESETREQ (SCS_AIRCR[2]), Application Interrupt and Reset Control Register, address = 0xE000ED0C) in system control registers of MCU. Note: Software can write 1 to clear this bit.
[4]	BODRF	BOD Reset Flag The BOD reset flag is set by the “Reset Signal” from the Brown-out Detector to indicate the previous reset source. 0 = No reset from BOD. 1 = The BOD had issued the reset signal to reset the system. Note: Software can write 1 to clear this bit.
[3]	LVRRF	LVR Reset Flag The LVR reset flag is set by the “Reset Signal” from the Low-Voltage-Reset (LVR) to indicate the previous reset source. 0 = No reset from LVR. 1 = LVR had issued the reset signal to reset the system. Note: Software can write 1 to clear this bit.
[2]	WDTRF	WDT/WWDT Reset Flag The WDT reset flag is set by the “Reset Signal” from the Watchdog Timer or Window Watchdog Timer to indicate the previous reset source. 0 = No reset from watchdog timer or window watchdog timer. 1 = The watchdog timer or window watchdog timer had issued the reset signal to reset the system. Note: Software can write 1 to clear this bit.
[1]	PINRF	NRESET Pin/POR Reset Flag The nRESET pin reset flag is set by the “Reset Signal” from the nRESET pin or Power-on Reset (POR) Controller to indicate the previous reset source. 0 = No reset from nRESET pin, POR. 1 = Pin nRESET, POR had issued the reset signal to reset the system. Note: Software can write 1 to clear this bit.
[0]	CHIPRF	CHIP Reset Flag The CHIP reset flag is set by the “Reset Signal” from the CHIPRST (IPRST0[0]) to indicate the previous reset source. 0 = No reset from CHIPRST. 1 = CHIPRST had issued the reset signal to reset the system. Note: Software can write 1 to clear this bit.

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4.2.10.2 Peripheral Reset Control Register 0(IPRST0)

Register	Offset	R/W	Description	Reset Value
IPRST0	RCC_BA+0x04	R/W	Peripheral Reset Control Register 0	0x0000_0000

Bits	Description	
[31:2]	Reserved	Reserved.
[1]	CPURST	Processor Core One-shot Reset (Write Protected) Setting this bit will only reset the processor core and Flash Memory Controller (FMC), and this bit will automatically return to 0. 0 = Processor core operates normally. 1 = Processor core one-shot is reset. Note: This bit is write-protected. Refer to the SYS_REGLCTL register.
[0]	CHIPRST	CHIP One-shot Reset (Write Protected) Setting this bit will reset the whole chip, including Processor core and all peripherals, and this bit will automatically return to 0. The CHIPRST is the same as the POR reset, all the chip controllers is reset and the chip settings from flash are also reload. 0 = Chip normal operates normally. 1 = CHIP one-shot is reset. Note: This bit is write-protected. Refer to the SYS_REGLCTL register.

4.2.10.3 Peripheral Reset Control Register 1(IPRST1)

Register	Offset	R/W	Description	Reset Value
IPRST1	RCC_BA+0x08	R/W	Peripheral Reset Control Register 1	0x0000_0000

Bits	Description	
[31:21]	Reserved	Reserved.
[20]	RFRST	RF Controller Reset 0 = RF controller operates normally. 1 = RF controller is reset.
[19:18]	Reserved	Reserved
[17]	UART3RST	UART3 Controller Reset 0 = UART3 controller operates normally. 1 = UART3 controller is reset.
[16]	UART2RST	UART2 Controller Reset 0 = UART2 controller operates normally. 1 = UART2 controller is reset.
[15]	GPIORST	GPIO (P0~P5) Controller Reset 0 = GPIO controller operates normally. 1 = GPIO controller is reset.
[14]	TMR2RST	Timer2 Controller Reset

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		0 = Timer2 controller operates normally. 1 = Timer2 controller is reset.
[13]	TMR1RST	Timer1 Controller Reset 0 = Timer1 controller operates normally. 1 = Timer1 controller is reset.
[12]	TMR0RST	Timer0 Controller Reset 0 = Timer0 controller operates normally. 1 = Timer0 controller is reset.
[11]	WWDTRST	WWDT Controller Reset 0 = WWDT controller operates normally. 1 = WWDT controller is reset.
[10]	WDTRST	WDT Controller Reset 0 = WDT controller operates normally. 1 = WDT controller is reset.
[9]	ADCRST	ADC Controller Reset 0 = ADC controller operates normally. 1 = ADC controller is reset.
[8]	PWMRST	PWM0 Controller Reset 0 = PWM0 controller operates normally. 1 = PWM0 controller is reset.
[7]	UART1RST	UART1 Controller Reset 0 = UART1 controller operates normally. 1 = UART1 controller is reset.
[6]	UART0RST	UART0 Controller Reset 0 = UART0 controller operates normally. 1 = UART0 controller is reset.
[5:3]	Reserved	Reserved
[2]	SPI0RST	SPI0 Controller Reset 0 = SPI0 controller operates normally. 1 = SPI0 controller is reset.
[1]	Reserved	Reserved
[0]	I2C0RST	I2C0 Controller Reset 0 = I2C0 controller operates normally. 1 = I2C0 controller is reset.

4.2.10.4 Brown-out Detector Control Register (BODCTL)

Register	Offset	R/W	Description	Reset Value
BODCTL	RCC_BA+0x0C	R/W	Brown-out Detector Control Register	0x0000_0040

Bits	Description	
[31:7]	Reserved	Reserved.
[6]	BODOUT	Brown-out Detector Output Status

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		1 = Brown-out Detector status output is 0, when the detected voltage is higher than BODVL setting. 0 = Brown-out Detector status output is 1, when the detected voltage is lower than BODVL setting.
[5]	Reserved	Reserved.
[4]	BODIF	Brown-out Detector Interrupt Flag 0 = Brown-out Detector does not detect any voltage draft when VDD is down through or up through the voltage of BODVL setting. 1 = If Brown-out Detector detects the VDD is dropped through the voltage of BODVL setting or the VDD is raised up through the voltage of BODVL setting, this bit is set to 1 and the Brown-out interrupt is requested if Brown-out interrupt is enabled.
[3]	BODRSTEN	Brown-out Reset Enable Bit (Write Protect) 0 = Brown-out "INTERRUPT" function enabled; when the Brown-out Detector function is enable and the detected voltage is lower than the threshold, assert a signal to interrupt the MCU 1 = Brown-out "RESET" function enabled; when the Brown-out Detector function is enabled and the detected voltage is lower than the threshold, then assert a signal to reset the chip. Note: When the EN_BOD is enabled and the interrupt is asserted, the interrupt will be kept till the EN_BOD is set to 0. The interrupt for CPU can be blocked by disabling the NVIC in CPU for BOD interrupt. Or the interrupt source can be disabled by disabling the EN_BOD and then re-enabling the EN_BOD function if the BOD function is required. Default value: 0
[2:0]	Reserved	Reserved.

4.2.10.5 BOD LVR De-Bounce Control Register (BLDBCTL)

Register	Offset	R/W	Description	Reset Value
BLDBCTL	RCC_BA+0x10	R/W	BOD LVR De-Bounce Control Register	0x0000_2020

Bits	Description	
[31:14]	Reserved	Reserved.
[13:8]	LVRDBSEL	LVR De-Bounce (glitch) time Control register [0]=1: about 2^4 SYS clock [1]=1: about 2^7 SYS clock [2]=1: about 2^9 SYS clock [3]=1: about 2^11 SYS clock [4]=1: about 2^13 SYS clock [5]=1: about 2^15 SYS clock(default) Note: If software enables more than one bit, the bit with the smallest number will be selected and the other enabled channels will be ignored.
[7:6]	Reserved	Reserved.
[5:0]	BODDBSEL	BOD De-Bounce (glitch) time Control register [0]=1: about 2^4 SYS clock [1]=1: about 2^7 SYS clock [2]=1: about 2^9 SYS clock

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		[3]=1: about 2^11 SYS clock [4]=1: about 2^13 SYS clock [5]=1: about 2^15 SYS clock (default) Note: If software enables more than one bit, the bit with the smallest number will be selected and other enabled channels will be ignored.

4.2.10.6 Clock Wake Up Stable Timing Control Register0 (CLK_WKUP_0)

Register	Offset	R/W	Description	Reset Value
CLK_WKUP_0	RCC_BA+0x40	R/W	Clock Wake Up Stable Timing Control Register0	0x0840_0840

Bits	Description	
[31:24]	Reserved	Reserved
[23:16]	HXT_16M_WUSEL	16MHz HXT Stable Timing Select (62.5ns) [0]=1: about 2^1 HXT clock [1]=1: about 2^3 HXT clock [2]=1: about 2^5 HXT clock [3]=1: about 2^7 HXT clock [4]=1: about 2^9 HXT clock [5]=1: about 2^11 HXT clock [6]=1: about 2^13 HXT clock(default)512us [7]=1: about 2^15 HXT clock
[15:8]	RCO_32K_WUSEL	RCL Stable Timing Select (31.25us) (need to update to LP) [0]=1: about 2^0 RCL clock [1]=1: about 2^1 RCL clock [2]=1: about 2^2 RCL clock [3]=1: about 2^3 RCL clock(default) 250us [4]=1: about 2^4 RCL clock [5]=1: about 2^5 RCL clock
[7:0]	RCO_16M_WUSEL	16MHz RC Stable Timing Select (62.5ns) [0]=1: about 2^1 RCH clock [1]=1: about 2^3 RCH clock [2]=1: about 2^5 RCH clock [3]=1: about 2^7 RCH clock [4]=1: about 2^9 RCH clock [5]=1: about 2^1 RCH clock [6]=1: about 2^13 RCH clock(default)512us [7]=1: about 2^15 RCH clock

4.2.10.7 Clock Wake Up Stable Timing Control Register1 (CLK_WKUP_1)

Register	Offset	R/W	Description	Reset Value
CLK_WKUP_1	RCC_BA+0x44	R/W	Clock Wake Up Stable Timing Control Register1	0x0040_4040

Bits	Description

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[31:8]	Reserved	Reserved
[7:0]	MCU_DPLLWUSEL	MCU DPLL Stable Time Selection [0]=1: about 2^1 MCU DPLL clock [1]=1: about 2^3 MCU DPLL clock [2]=1: about 2^5 MCU DPLL clock [3]=1: about 2^7 MCU DPLL clock [4]=1: about 2^9 MCU DPLL clock [5]=1: about 2^11 MCU DPLL clock [6]=1: about 2^13 MCU DPLL clock(default) [7]=1: about 2^15 MCU DPLL clock

4.2.10.8 Clock Divider Control register0 (CLK_DIV_0)

Register	Offset	R/W	Description	Reset Value
CLK_DIV_0	RCC_BA+0x48	R/W	Clock Divider Control register0	0x0001_0000

Bits	Description	
[31:12]	Reserved	Reserved.
[11:8]	AHB_DIV	AHB Clock Divider Select [3:0]=0: clock does not divide [3:0]=N: clock is divided, clock = 1/(N+1), (0<N<16)
[7:4]	Reserved	Reserved
[3:0]	MCU_DIV	MCU DPLL Divider Select [3:0]=0: clock does not divide [3:0]=N: clock is divided, clock = 1/(N+1), (0<N<16)

4.2.10.9 Clock Divider Control register1 (CLK_DIV_1)

Register	Offset	R/W	Description	Reset Value
CLK_DIV_1	RCC_BA+0x4C	R/W	Clock Divider Control register1	0x0000_0000

Bits	Description	
[31:12]	Reserved	Reserved
[11:8]	APB2_DIV	APB2 Clock Divider Select [3:0]=0: clock does not divide [3:0]=N: clock is divided, clock = 1/(2*N), (0<N<16)
[7:4]	Reserved	Reserved
[3:0]	APB1_DIV	APB1 Clock Divider Select [3:0]=0: clock does not divide [3:0]=N: clock is divided, clock = 1/(2*N), (0<N<16)

4.2.10.10 AHB Clock Source Select Control（CLK_AHB_SEL）

Register	Offset	R/W	Description	Reset Value
CLK_AHB_SEL	RCC_BA+0x50	R	AHB Clock Source Select Control	0x0000_0000

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Bits	Description	
[31:4]	Reserved	Reserved.
[3:2]	DIG_CLK_SEL	DPLL Clock Choice(Write Protected) 00 = 48M 01 = 57.6M 10/11 = 72M
[1:0]	AHB_CLK_SEL	AHB Clock Select(Write Protected) 00 = RCH 01 = HXT 10 = MCU_DPLL

4.2.10.11 APB Peripherals Clock Source Select Control (CLK_APB_SEL)

Register	Offset	R/W	Description	Reset Value
CLK_APB_SEL	RCC_BA+0x54	R/W	APB Peripherals Clock Source Select Control	0x0000_0000

Bits	Description	
[31:20]	Reserved	Reserved.
[19:18]	tmr2sel	00 = APB1_CLK 01 = RCL 1x = TM2_I
[17:16]	tmr1sel	00 = APB1_CLK 01 = RCL 1x = TM1_I
[15:4]	Reserved	Reserved.
[3:2]	tmr0sel	00 = APB1_CLK 01 = RCL 1x = TM0_I
[1]	wwdtsel	WWDT Selection(Write Protected) 0 = APB1_CLK / 2048 1 = RCL
[0]	wdtsel	WDT Selection(Write Protected) 0 = APB1_CLK / 2048 1 = RCL

4.2.10.12 AHB Clock Enable Register（CLK_AHB_EN）

Register	Offset	R/W	Description	Reset Value
CLK_AHB_EN	RCC_BA+0x58	R/W	AHB Clock Enable Register	0x0002_0002

Bits	Description	
[31:17]	Reserved	Reserved.
[16]	rfcken	RF (RF_DPLL and RF) Clock Enable 0 = Clock disabled

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		1 = Clock enabled
[15:2]	Reserved	Reserved.
[1]	stcken	System Tick Clock Enable 0 = Clock disabled 1 = Clock enabled
[0]	Reserved	Reserved.

4.2.10.13 APB1 Clock Enable Register（CLK_APB1_EN）

Register	Offset	R/W	Description	Reset Value
CLK_APB1_EN	RCC_BA+0x5C	R/W	APB1 Clock Enable Register	0x0000_0000

Bits	Description	
[31:13]	Reserved	Reserved.
[12]	apb1cken	APB1 Clock Enable 0 = Clock disabled 1 = Clock enabled
[11]	tmr0cken	Timer0 Clock Enable 0 = Clock disabled 1 = Clock enabled
[10]	wwdtcken	WWDT Clock Enable 0 = Clock disabled 1 = Clock enabled
[9]	wdtcken	WDT Clock Enable 0 = Clock disabled 1 = Clock enabled
[8]	adccken	ADC Clock Enable 0 = Clock disabled 1 = Clock enabled
[7]	pwm67cken	PWM67 Clock Enable 0 = Clock disabled 1 = Clock enabled
[6]	pwm45cken	PWM45 Clock Enable 0 = Clock disabled 1 = Clock enabled
[5]	pwm23cken	PWM23 Clock Enable 0 = Clock disabled 1 = Clock enabled
[4]	pwm01cken	PWM01 Clock Enable 0 = Clock disabled 1 = Clock enabled
[3]	uart0cken	UART0 Clock Enable 0 = Clock disabled 1 = Clock enabled

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[2]	Reserved	Reserved
[1]	spi0cken	SPI0 Clock Enable 0 = Clock disabled 1 = Clock enabled
[0]	i2c0cken	I2C0 Clock Enable 0 = Clock disabled 1 = Clock enabled

4.2.10.14 APB2 Clock Enable Register（CLK_APB2_EN）

Register	Offset	R/W	Description	Reset Value
CLK_APB2_EN	RCC_BA+0x60	R/W	APB2 Clock Enable Register	0x0000_0000

Bits	Description	
[31:12]	Reserved	Reserved.
[11]	apb2cken	APB2 Clock Enable 0 = Clock disabled 1 = Clock enabled
[10:9]	Reserved	Reserved
[8]	uart3cken	UART3 Clock Enable 0 = Clock disabled 1 = Clock enabled
[7]	uart2cken	UART2 Clock Enable 0 = Clock disabled 1 = Clock enabled
[6]	Reserved	Reserved
[5]	tmr2cken	Timer2 Clock Enable 0 = Clock disabled 1 = Clock enabled
[4]	tmr1cken	Timer1 Clock Enable 0 = Clock disabled 1 = Clock enabled
[3]	uart1cken	UART1 Clock Enable 0 = Clock disabled 1 = Clock enabled
[2:0]	Reserved	Reserved

4.2.10.15 Clock Stable Status Register (CLK_STB_STATUS)

Register	Offset	R/W	Description	Reset Value
CLK_STB_STATUS	RCC_BA+0x64	RO	Clock Stable Status Register	0x0000_0003

Bits	Description	
[31:5]	Reserved	Reserved.

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[4]	Rf_dpll_stb	RF_DPLL Stable Flag. 0 = RF_DPLL unstable, can not be used. 1 = RF_DPLL satable.
[3]	Mcu_dpll_stb	MCU_DPLL Stable Flag. 0 = MCU_DPLL unstable, can not be used. 1 = MCU_DPLL satable.
[2]	Hxt16_stb	HXT Stable Flag. 0 = HXT unstable, can not be used. 1 = HXT satable.
[1]	Rc16m_stb	RCH Stable Flag. 0 = RCH unstable, can not be used. 1 = RCH satable.
[0]	Rc32k_stb	RCL Stable Flag. 0 = RCL unstable, can not be used. 1 = RCL satable.

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4.3 Analog Low Power Controller(ANA)

4.3.1 Overview

The ANA module decides whether the chip operates in low power mode. Moreover, this module can execute the wake up function. The wake-up logic is in the 3V domain and the working logic is in the 1.5V domain.

4.3.2 Features

- Three levels of low power mode
  - Standby mode
  - Sleep mode
  - Deep_Sleep mode

4.3.3 Functional Description

4.3.3.1 Work State

The PAN2025 uses a low-power design with multiple voltage domains. The wake-up logic is in the 3V domain and the working logic is in the 1.5V domain.There are three levels of low power mode. In different applications, the user can choose different mode to get the lowest power consumption and the highest performance.Table 4-4 lists the related descriptions of each power mode.

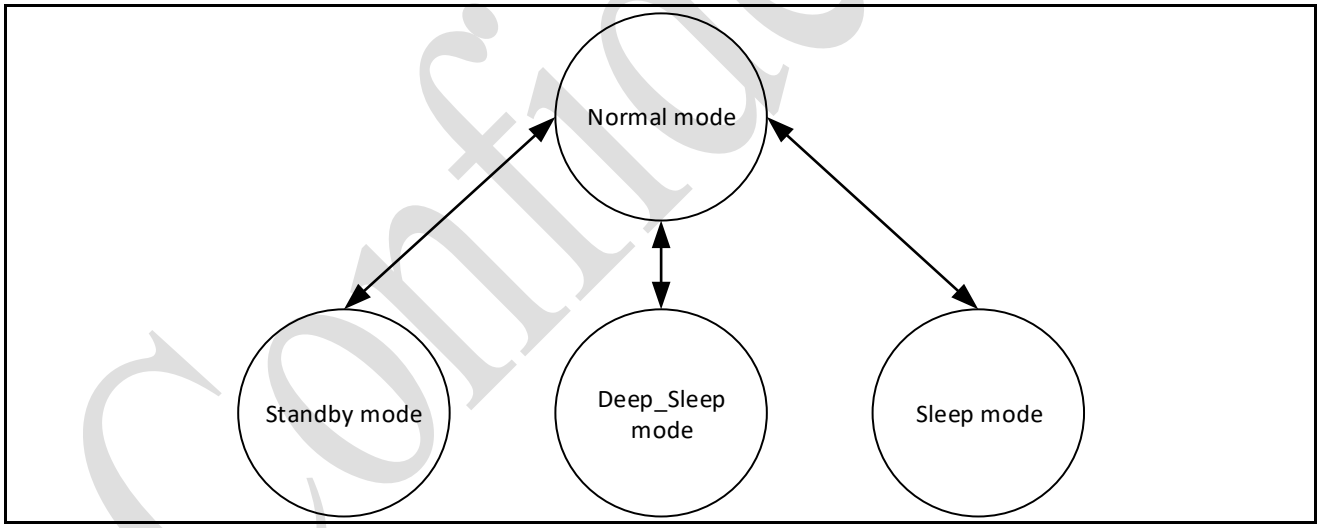

Figure 4-9 Work States

Table 4-4 Power Mode Difference Table

States	Descriptions	Wake up sources	Wake up time	Power consumption
Deep_Sleep mode	3V digital region works. 1.5V(main region) LDO works in low power mode. No clocks.	All GPIO;	Just as long as chip power up.	The lowest power consumption which is near 0.

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	3V digital region works. 1.5V(main region) LDO works in low power mode. RCL clock is on.	All GPIO; Timer WDT		
Sleep mode	3V digital region works. 1.5V(main region) LDO works in normal mode. RCL and RCH clocks are on, but CPU clock is off.	All GPIO; Timer Any interrupts	Just as long as chip power up.	Lower power consumption.
Standby mode	Only 3V region supplies. No clocks.	GPIO (P5.6);	Depend on wake_up source activity.	Low power consumption.
	Only 3V region supplies. RCL clocks is on..	GPIO (P5.6); Timer		
Normal mode	All regions are in right voltages.	-	-	Working power consumption.

The low power mode is mainly implemented by the control signal which is from software to analog part. Table 4-5 illustrates the control signals and the corresponding relationship.

Table 4-5 Relationship Between Control Signal and States

States / Control signal	Normal	Deep_Sleep	Sleep	Standby
PWR_UP	1	1	1	1
EN_PMU	1	1	1	1
CE_INT	1	1	1	1
EN_LDO (for RF region)	1	1	1	0
EN_DVDD_LP (small LDO)	0	1	1	1
EN_RC_32K_LP	1	x	1	x
EN_DPLL	1	0	0	x
EN_RC_16M	x	0	1	0

4.3.3.2 Low Power Process

4.3.3.2.1. Enter and Exit Deep_Sleep Mode

In Deep_Sleep mode, the difference between QFN32 and QFN40 packages depends on whether the capacitor can be hung outside the DVDD.

Entering Deep_Sleep mode from normal mode:

1. Set P5.6 to input mode without pulling up; (If not woken up by P5.6, this step can be omitted)
2. Enable Timer in 3V region, enable sleep_cnt_en (LP_FL_CTRL0[1]), and set the value of timer;

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(If not woken up by Timer, this step can be omitted)
3. Disable 1.5V region reset, and set reset_en (LP_1P5V_RST[8]) to 0.
4. LDO works in low power mode
5. Enable NVIC. Sleep_int_en (LP_INT_CTRL[1]) and sleep_en (LP_FL_CTRL0[17]) are both set to 1.
6. Close the extra RCH enable bit, and set RC_16M_CTRL (LP_MISC[1]) to 0.
7. Disable LDO in 1.5V region. (Bandgap, LDO_DPLL, DPLL, XTAL and RCH are all closed, LDO works in low power mode)
8. Request to enter standby mode.

Entering normal mode from Deep_Sleep mode:

1. Pull P5.6 high and sustain above 500us. Or
2. LP_TMR timer scale in 3V region is 31.25us, so 32000 is equivalent to 1 second. Or
3. Other GPIOs.

4.3.3.2.2. Enter and Exit Sleep Mode

Entering Sleep mode from normal mode:

To enter Sleep mode from normal mode, there are two circumstances:

- Woken up by P5.6 and 32K timer
- Woken up by other peripherals

If It is woken up by P5.6 and 32K timer, please adhere to the following software operation process:

1. Set P5.6 to input mode, without pulling up; (If not woken up by P5.6, this step can be omitted)
2. Enable Timer in 3V region, enable sleep_cnt_en (LP_FL_CTRL0[1]), and set the value of timer; (If not woken up by Timer, this step can be omitted)
3. Disable 1.5V region reset, and set reset_en (LP_1P5V_RST[8]) to 0.
4. Enable NVIC. And set Sleep_int_en (LP_INT_CTRL[1]) and sleep_en (LP_FL_CTRL0[17]) to 1.
5. Enable low power mode, and set sleep_en (LP_FL_CTRL0[17]) to 1.
6. Send WFI

If it is woken up by other peripherals, please adhere to the following software operation process:

1. Disable 1.5V region reset, and set reset_en (LP_1P5V_RST[8]) to 0.
2. Enable the wake up function of timer1
3. Enable low power mode, and set sleep_int_en (LP_FL_CTRL0[17]) to 1.
4. Send WFI

Entering normal mode from Sleep mode:

1. Pull P5.6 high and sustain above 500us. Or
2. LP_TMR timer scale in 3V region is 31.25us, so 32000 is equivalent to 1 second. Or
3. Other peripherals interrupts.

4.3.3.2.3. Enter and Exit Standby Mode

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Entering Standby mode from normal mode:

1. Set P5.6 to input mode without pulling up; (If not woken up by P5.6, this step can be omitted)
2. Enable Timer in 3V region, enable sleep_cnt_en (LP_FL_CTRL0[1]), and set the value of timer; (If not woken up by Timer, this step can be omitted)
3. Switch the system clock to RCH
4. Close XTAL, DPLL and analog LDO
5. Enable NVIC interrupt. And enable Standby_int_en (LP_INT_CTRL[1]) and sleep_en (LP_FL_CTRL0 [7]).
6. Enable 1.5V region reset(close bandgap and strong LDO).
7. If SRAM retention function is enabled, LDO_HP needs to be opened.
8. Request to enter standby mode.

Entering normal mode from Standby mode:

1. Pull P5.6 high and sustain above 500us. Or
2. Timer scale in 3V region is 31.25us, so 32000 is equivalent to 1 second.

4.3.4 ANA Register Map

Register	Offset	R/W	Description	Reset Value
ANA Base Address: **ANA_BA = 0x4007_0000**				
LP_REG_SYNC	ANA_BA+0x00	R/W	Low Power Synchronize Register	0x0000_0000
LP_FL_CTRL0	ANA_BA+0x04	R/W	Low Power Control Register	0x0000_0006
LP_FL_CTRL1	ANA_BA+0x08	R/W	Low Power Flow Control1	0x0000_0737
LP_SLT	ANA_BA+0x0C	R/W	Low Power Sleep Time Register	0xFFFF_FFFF
LP_1P5V_RST	ANA_BA+0x10	R/W	Digital 1.5V Region Reset Control Register	0x0000_0108
LP_INT_CTRL	ANA_BA+0x14	R/W	Low Power Interrupt Control Register	0x0000_0001
LP_ANA_CTRL0	ANA_BA+0x18	R/W	Low Power Analog Control0	0x0333_3336
LP_ANA_CTRL1	ANA_BA+0x1C	R/W	Low Power Analog Control1	0x0112_10C0
LP_ANA_CTRL2	ANA_BA+0x20	R/W	Low Power Analog Control2	0x0000_FF00
LP_MISC	ANA_BA+0x24	R/W	Low Power Miscellany Register	0x0000_0002
ANA_BOD_LVR_CTRL	ANA_BA+0x28	R/W	Analog BOD&LVR Control Register	0x0000_0010
ANA_RC_DPLL_CTRL	ANA_BA+0x2C	R/W	Analog RC&DPLL Control Register	0x0001_0080
ANA_ST	ANA_BA+0x30	RO	Analog Status Register	0x0000_0337
ANA_1P5V_RSV	ANA_BA+0x34	R/W	Analog 1.5V Reserved	0x0002_FF01

4.3.5 ANA Register Description

4.3.5.1 Low Power Synchronize Register (LP_REG_SYNC)

Register	Offset	R/W	Description	Reset Value
LP_REG_SYNC	ANA_BA+0x00	R/W	Low Power Synchronize Register	0x0000_0000

Bits	Description	
[31:2]	Reserved	Reserved.

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[1]	reg_sync_sts	Register Synchronization State (Read only) When bit[0] (reg_sync_3v) is set to 1, subsequent operation will be executed until this bit has been cleared to 0
[0]	reg_sync_3v	1 = The register's values are synchronized to high voltage (3V) region. 0 = The register's values are synchronized to low voltage (1.5V) region.

4.3.5.2 Low Power Flow Control0(LP_FL_CTRL0)

Register	Offset	R/W	Description	Reset Value
LP_FL_CTRL0	ANA_BA+0x04	R/W	Low Power Control Register	0x0000_0006

Bits	Description	
[31:29]	Reserved	Reserved.
[28]	en_ldo_dpll_sleep_en	Control the DPLL LDO when enter sleep mode. 0 = DPLL LDO will not be closed; 1 = DPLL LDO will be closed
[27]	en_ls_sleep_en	Control the Level Shift when enter sleep mode. 0 = Level Shift will not be closed; 1 = Level Shift will be closed.
[26]	en_dvdd_hp_sleep_en	Control the HP LDO when enter sleep mode. 0 = HP LDO will not be closed; 1 = HP LDO will be closed
[25]	Reserved	Reserved.
[24]	en_dpll_sleep_en	Control the DPLL when enter sleep mode. 0 = DPLL will not be closed; 1 = DPLL will be closed
[23]	rco16m_sleep_en	Control the RCH when enter sleep mode. 0 = RCH will not be closed; 1 = RCH will be closed
[22]	rco32k_sleep_en	Control the RCL when enter sleep mode. 0 = RCL will not be closed; 1 = RCL will be closed
[21]	lpldo_sleep_en	Control the LP LDO when enter sleep mode. 0 = LP LDO will not be closed; 1 = LP LDO will be closed
[20]	ce_int_sleep_en	Control the XTL buffer when enter sleep mode. 0 = XTL buffer will not be closed; 1 = XTL buffer will be closed
[19]	en_pm_sleep_en	Control the PMU when enter sleep mode. 0 = PUM will not be closed; 1 = PMU will be closed
[18]	pwr_up_sleep_en	Control the XTH when enter sleep mode. 0 = XTH will not be closed ; 1 = XTH will be closed.

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[17]	sleep_en	Control the sleep function of the chip, when this bit is set to 0, Standby and Deepsleep mode is disabled
[16]	extwkupdsb	External wake up disable bit. (P56) 0 = External wake up enabled 1 = External wake up disabled. Can not be woken up by P56. Default value: 0
[15:3]	Reserved	Reserved
[2]	extwkup_sel	Control the wakeup pole of P56. 0 = P56 woken up by low level 1 = P56 woken up by high level
[1]	sleep_cnt_en	Low Power counter enable bit. 0 = Low power counter disabled 1 = Low power counter enabled
[0]	sleep_req	Software set this bit to 1 when request to enter sleep mode.

4.3.5.3 Low Power Flow Control1 (LP_FL_CTRL1)

Register	Offset	R/W	Description	Reset Value
LP_FL_CTRL1	ANA_BA+0x08	R/W	Low Power Flow Control1	0x0000_0737

Bits	Description	
[31:12]	Reserved	Reserved.
[11]	EN_LDO_DPLL	LDO_DPLL enable bit 0 = LDO_DPLL enabled 1 = LDO_DPLL disabled
[10]	EN_DVDD_RAM	HP LDO for SRAM enable bit. 0 = HP DVDD LDO supply for SRAM. 1 = LP DVDD LDO supply for SRAM.
[9]	EN_LS	Level shift enable bit. 0 = Level shift disabled. 1 = Level shift enabled.
[8]	EN_DVDD_HP	High power DVDD LDO enable bit 0 = High power DVDD LDO disabled. 1 = High power DVDD LDO enabled.
[7]	Reserved	Reserved.
[6]	EN_DPLL	DPLL enable bit 0 = DPLL disabled. 1 = DPLL enabled.
[5]	EN_RC_16M	RCH clock enable bit 0 = RCH clock disabled. 1 = RCH clock enabled.
[4]	EN_RC_32K_LP	RCL clock enable bit 0 = RCL clock disabled. 1 = RCL clock enabled.

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[3]	EN_DVDD_LP	Low power LDO enable bit 0 = Low power LDO disabled. 1 = Low power LDO enabled. Default value: 0x1
[2]	CE_INT	0 = Xtal output disable 1 = Xtal output enable
[1]	EN_PMU	1 = Bandgap and digital LDO enable Note: This bit can not be set to 0.
[0]	PWR_UP	1 = Xtal startup 0 = Xtal not startup

4.3.5.4 Low Power Sleep Time(LP_SLT)

Register	Offset	R/W	Description	Reset Value
LP_SLT	ANA_BA+0x0C	R/W	Low Power Sleep Time Register	0xFFFF_FFFF

Bits	Description	
[31:0]	Sleep_time	Sleep timer [0] = 0 * RCL clock [1] = 1 * RCL clock [2] = 2 * RCL clock [3] = 3 * RCL clock …

4.3.5.5 Low Power 1.5V Reset Control（LP_1P5V_RST）

Register	Offset	R/W	Description	Reset Value
LP_1P5V_RST	ANA_BA+0x10	R/W	Digital 1.5V Region Reset Control Register	0x0000_0108

Bits	Description	
[31:9]	Reserved	Reserved.
[8]	reset_en	1.5V reset enable bit 0 = Reset disabled. 1 = Reset enabled.
[7:0]	reset_dly_time	Digital 1.5V Reset Delay Selection 0 = Reserved 1 = Max time-out period is 1 * RCL. 2 = Max time-out period is 2 * RCL. 3 = Max time-out period is 3 * RCL. … 256 = Max time-out period is 256 * RCL.

4.3.5.6 Low Power Interrupt Control (LP_INT_CTRL)

Register	Offset	R/W	Description	Reset Value

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LP_INT_CTRL	ANA_BA+0x14	R/W	Low Power Interrupt Control Register	0x0000_0001

Bits	Description	
[31:18]	Reserved	Reserved.
[17]	Tmr32k_wk_flg	32k Timer Wake Up Flag. Write 1 to clear this bit.
[16]	P56_wk_flg	P56 Wake Up Flag. Write 1 to clear this bit.
[15:10]	Reserved	Reserved
[9]	Sleep_int_flg	DeepSleep/Sleep Wake Up Interrupt Flag. Write 1 to clear this bit.
[8]	Standby_int_flg	Standby Wake Up Interrupt Flag. Write 1 to clear this bit.
[7:2]	Reserved	Reserved
[1]	Sleep_int_en	DeepSleep/Sleep Wake Up Interrupt Enable Bit. 0 = Disabled 1 = Enabled
[0]	Standby_int_en	Standby Wake Up Interrupt Enable Bit. 0 = Disabled 1 = Enabled

4.3.5.7 Low Power Analog Control0(LP_ANA_CTRL0)

Register	Offset	R/W	Description	Reset Value
LP_ANA_CTRL0	ANA_BA+0x18	R/W	Low Power Analog Control0	0x0333_3336

Bits	Description	
[31:27]	Reserved	Reserved.
[26:24]	DVDD_LDO_SEL	DVDD LDO Output Voltage Selection 000 = 1.32V 001 = 1.393V 010 = 1.466V …(step size = 73mV) 111 = 1.82V
[23]	Reserved	Reserved.
[22:20]	VDDDIV2_LDO_SEL	DIV2 LDO Output Voltage Selection. 000 = 1.32V 001 = 1.393V 010 = 1.466V …(step size = 73mV) 111 = 1.82V
[19]	Reserved	Reserved.
[18:16]	VDDIF_LDO_SEL	IF LDO Output Voltage Selection. 000 = 1.32V 001 = 1.393V 010 = 1.466V …(step size = 73mV) 111 = 1.82V

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[15]	Reserved	Reserved.
[14:12]	VDDLO_LDO_SEL	PLL LDO Output Voltage Selection. 000 = 1.32V 001 = 1.393V 010 = 1.466V …(step size = 73mV) 111 = 1.82V
[11]	Reserved	Reserved.
[10:8]	VDDVCO_LDO_SEL	VCO LDO Output Voltage Selection. 000 = 1.32V 001 = 1.393V 010 = 1.466V …(step size = 73mV) 111 = 1.82V
[7]	Reserved	Reserved.
[6:4]	VDDDPLL_LDO_SEL	DPLL LDO Output Voltage Selection. 000 = 1.32V 001 = 1.393V 010 = 1.466V …(step size = 73mV) 111 = 1.82V
[3:1]	VDDRX_LDO_SEL	RX LDO Output Voltage Selection. 000 = 1.32V 001 = 1.393V 010 = 1.466V …(step size = 73mV) 111 = 1.82V
[0]	EN_LDO	Control the RF relate LDO, when this bit set 0, all RF LDO will shuct down.

4.3.5.8 Low Power Analog Control1(LP_ANA_CTRL1)

Register	Offset	R/W	Description	Reset Value
LP_ANA_CTRL1	ANA_BA+0x1C	R/W	Low Power Analog Control1	0x0112_10C0

Bits	Description	
[31:25]	Reserved	Reserved.
[24]	XTAL_IB_CTL	Crystal Oscillator Current Control Bit.
[23:21]	Reserved	Reserved.
[20:16]	RC_I_TUNE	Charge Current Selection. RCL output frequency can be changed through changing the value of RC_I_TUNE 00000 = 46.7nA 00001 = 48.4nA …(step size = 1.7nA) 11111 = 99nA

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[15:13]	Reserved	Reserved.
[12:8]	VBG_TRIM	VBG Voltage Calibration Bit 00000 = 1.2V 00001 = 1.2063V 00010 = 1.2126V …(step size = 6.3mV) Default value: 0x10000
[7:4]	DVDD_LP_VSEL	Low Power LDO Output Voltage Selection 0000 = 200mV 0001 = 315mV 0010 = 430mV …(step size = 115mV) 1111 = 1950mV
[3]	DVDD_HP_SEL	High LDO Internal And External Capacitor Selection 0 = Internal capacitor 1 = External capacitor
[2]	DVDD_LP_SEL	Low LDO Internal And External Capacitor Selection 0 = Internal capacitor 1 = External capacitor
[1]	Reserved	Reserved.
[0]	EN_SRE	Low Power LDO Slew Rate Enhance Enable Bit 0 = Disabled 1 = Enabled.

4.3.5.9 Low Power Analog Control2(LP_ANA_CTRL2)

Register	Offset	R/W	Description	Reset Value
LP_ANA_CTRL2	ANA_BA+0x20	R/W	Low Power Analog Control2	0x0000_FF00

Bits	Description	
[31:18]	Reserved	Reserved.
[17:16]	extclk_en	External Clock Enable [1]: external RC32K clock enable bit(P56) 0 = external RC32K clock enabled 1 = external RC32K clock disabled [0]: external RC16M clock enable bit(P51) 0 = external RC16M clock enabled 1 = external RC16M clock disabled
[15:0]	Reserved	Reserved.

4.3.5.10 Low Power Miscellany(LP_MISC)

Register	Offset	R/W	Description	Reset Value
LP_MISC	ANA_BA+0x24	R/W	Low Power Miscellany Register	0x0000_0002

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Bits	Description	
[31:2]	Reserved	Reserved.
[1]	RC_16M_CTRL	RCH Control Bit. This bit is set when resetting. Otherwise, this bit should be cleared to 0 when executing in low power mode.
[0]	DPLL_CLK_SEL	DPLL Reference Clock Selection 0 = RC oscillator 1 = HXT oscillator

4.3.5.11 Analog BOD&LVR Control (ANA_BOD_LVR_CTRL)

Register	Offset	R/W	Description	Reset Value
ANA_BOD_LVR_CTRL	ANA_BA+0x28	R/W	Analog BOD&LVR Control Register	0x0000_0010

Bits	Description	
[31:5]	Reserved	Reserved.
[4:2]	BOD_SEL	BOD Reference Voltage Selection. 000 = 2V 001 = 2.2V 010 = 2.4V 011 = 2.6V 101 = 3.0V Others = reserved
[1]	EN_BOD	BOD Enable Bit. 0 = BOD not work 1 = BOD works
[0]	EN_LVR	LVR Enable Bit. 0 = LVR not work 1 = LVR works

4.3.5.12 Analog RC&DPLL Control (ANA_RC_DPLL_CTRL)

Register	Offset	R/W	Description	Reset Value
ANA_RC_DPLL_CTRL	ANA_BA+0x2C	R/W	Analog RC&DPLL Control Register	0x0001_0080

Bits	Description	
[31:18]	Reserved	Reserved.
[17:16]	DPLL_CP_ISEL	DPLL Control Signal, used for debug.
[15:8]	Reserved	Reserved.
[7:0]	RC_16M_FRQ	RCH Fine Tuning

4.3.5.13 Analog Status(ANA_ST)

Register	Offset	R/W	Description	Reset Value
ANA_ST	ANA_BA+0x30	RO	Analog Status Register	0x00000337

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Bits	Description	
[31:10]	Reserved.	Reserved.
[9]	En_ls	The Current States Of The Corresponding Control Bit. They reflect the states of register LP_FL_CTRL1 in 3V region.
[8]	En_dvdd_hp	
[7]	Xtal_en	
[6]	En_dpll	
[5]	En_rc_16m	
[4]	En_rc_32k_lp	
[3]	En_dvdd_lp	
[2]	Ce_int	
[1]	En_pmu	
[0]	Pwr_up	

4.3.5.14 Analog 1.5V Reserved (ANA_1P5V_RSV)

Register	Offset	R/W	Description	Reset Value
ANA_1P5V_RSV	ANA_BA+0x34	R/W	Analog 1.5V Reserved	0x0002_FF01

Bits	Description	
[31:25]	Reserved	Reserved.
[24]	Scan_mode	
[23:21]	Reserved	Reserved.
[20]	TST_TEMP	Temperature Detection Test Enable Bit. When this bit is set, it means to test VBG output voltage.
[19]	TST_DAC_VREF	DAC Reference Voltage Test Enable Bit. When this bit is set, it means to test VBG output voltage.
[18:17]	TEMP_GC	Temperature Test Gain Control: 00 = 0.82~1.71V 01 = 0.6~1.77V 10 = 0.388~1.829V 11 = 0.181~1.884V
[16]	EN_TEMP	Temperature detection enable bit. 1 = Enabled 0 = Disabled
[15:3]	Reserved	Reserved
[2]	RESERVED_LOW_1P5<2>	Adjust the current in the VCO that does not change with temperature. Default value: 0x0
[1]	RESERVED_LOW_1P5<1>	Whether the output voltage of LPF is pulled down to ground. 1: Pulled down to ground 0: Not pulled down to ground. Default value: 0x0
[0]	RESERVED_LOW_1P5<0>	Whether the output voltage of the CP module is voltage following.

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		1: Voltage following. 0: Not voltage following. Default value: 0x1

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4.4 RF Operation

4.4.1 Overview

A RF transceiver (TRX) is embedded in PAN2025. TRX is a GFSK transceiver operating in the worldwide ISM frequency band at 2400~2483.5MHz. Burst mode transmission and 1Mbps or 250Kbps air data rate make them suitable for applications requiring ultra low power consumption. The embedded packet processing engines enable their full operation with a very simple MCU as a radio system. Auto re-transmission and auto acknowledgement give reliable link without any MCU interference.

4.4.2 Features

- GFSK modulation
- Data rate: 1Mbps, 250Kbps
- CRC8/CRC16
- Support 1to 32 or 64 bytes payload length
- RF communicationmode : PAN2025B is recommended to communicate in RX mode.

4.4.3 Block Diagram

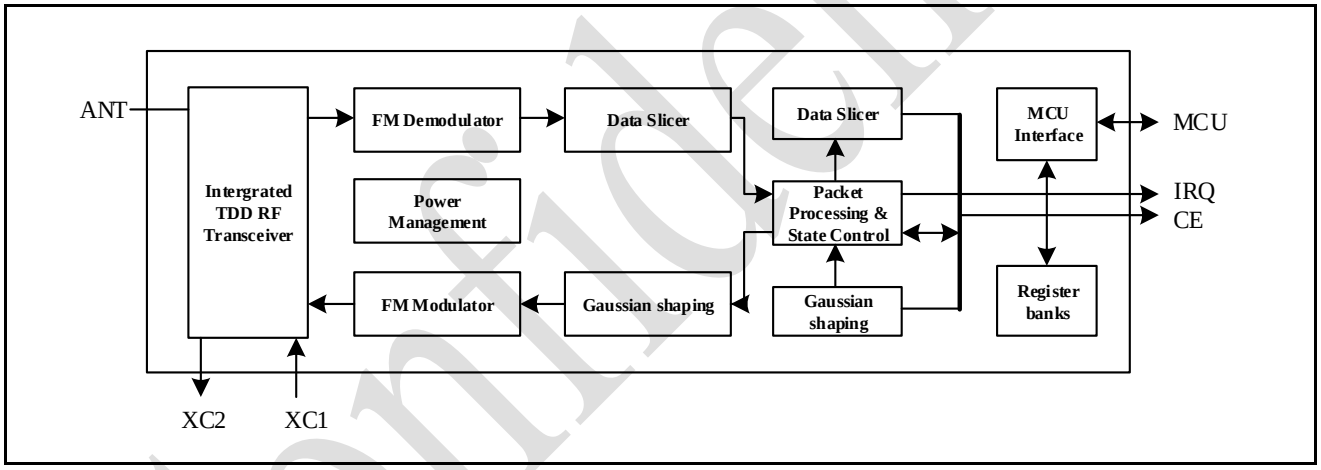

Figure 4-10RF Block Diagram

4.4.4 State Control

4.4.4.1 State Control Diagram

- Internal signal: POR,VDD
- Internal register: CE, PWR_UP_DIG, PRIM_RX, EN_AA, NO_ACK, ARC, ARD
- System information: Time out, ACK received, ARD elapsed, ARC_CNT, TX FIFO empty, ACK packet transmitted, Packet received

TRX has built-in state machines that control the state transition between different modes.

When auto acknowledge feature is disabled, state transition will be fully controlled by MCU.

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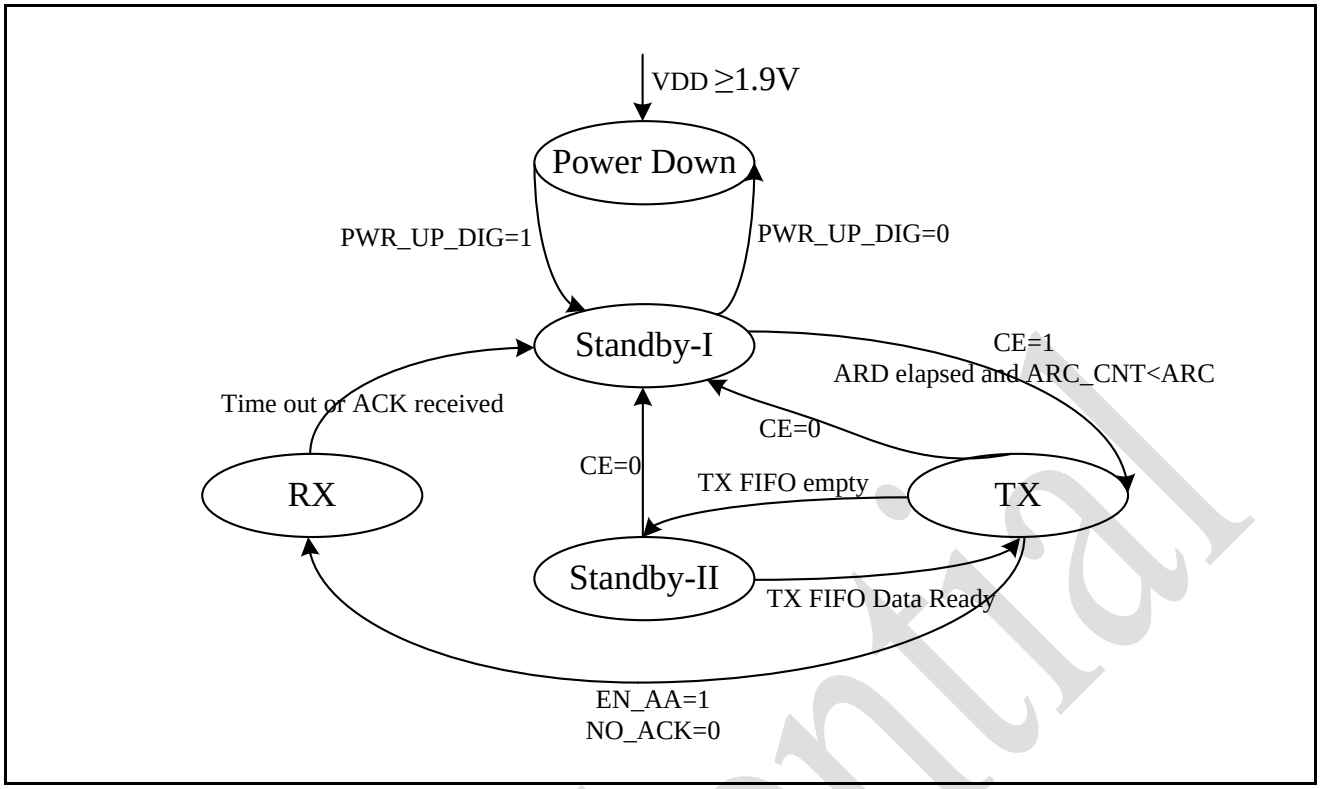

Figure 4-11 PTX (PRIM_RX=0) State Control Diagram

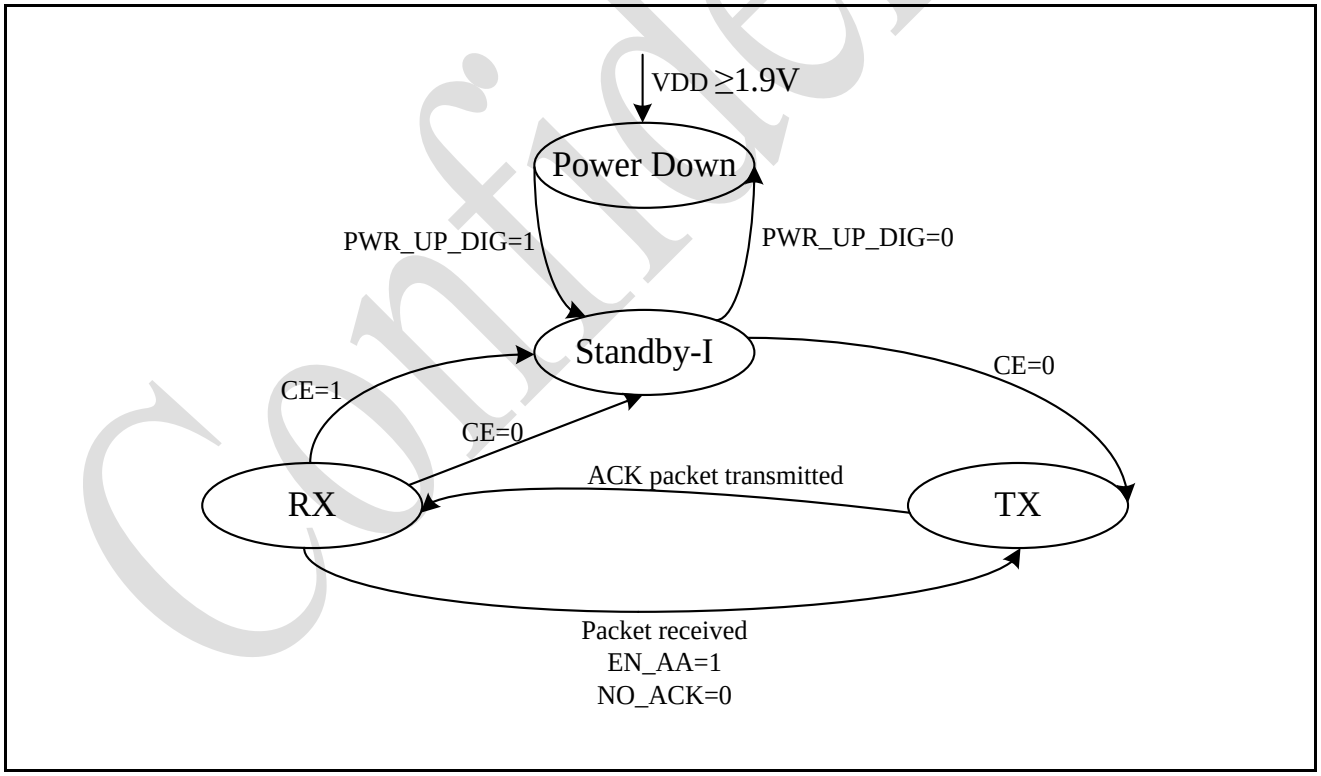

Figure 4-12PRX (PRIM_RX=1) State Control Diagram

4.4.4.2 Power Down Mode

In power down mode the baseband main FSM is in sleep mode with minimal current consumption. Power down mode is entered by setting the PWR_UP_DIG or EN_PMU_DIG bit in the CONFIG

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register to low.

4.4.4.3 Standby-I Mode

By setting the PWR_UP_DIG bit in the CONFIG register to 1 and de-asserting CE to 0, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start-up time. In this mode, part of the crystal oscillator is active. This is also the mode which the TRX returns to from TX or RX mode when CE is set low.

4.4.4.4 Standby-II Mode

Compared with standby-I mode, more clock buffers are active than in standby-I mode and much more current is used in standby-II mode. Standby-II occurs when CE is high on a PTX device with empty TX FIFO. If a new packet is uploaded to the TX FIFO in this mode, the device will automatically enter TX mode and the packet is transmitted.

4.4.4.5 TX Mode

- PTX device (PRIM_RX=0)

The TX mode is an active mode where the PTX device transmits a packet. To enter this mode from power down mode, the PTX device must set PWR_UP_DIG bit high and PRIM_RX bit low, moreover a payload in the TX FIFO, and a high pulse on the CE for more than 10μs. The PTX device stays in TX mode until it finishes transmitting the current packet. If CE = 0 it returns to standby-I mode. If CE = 1, the next action is determined by the status of the TX FIFO. If the TX FIFO is not empty the PTX device remains in TX mode, transmitting the next packet. If the TX FIFO is empty the PTX device goes into standby-II mode.

If the auto retransmission is enabled (EN_AA=1) and auto acknowledgement is required (NO_ACK=0), the PTX device will enter TX mode from standby-I mode when ARD elapsed and the number of retried is less than ARC.

- PRX device (PRIM_RX=1)

The PRX device will enter TX mode from RX mode only when EN_AA=1 and NO_ACK=0 in received packet to transmit acknowledge packet with pending payload in TX FIFO.

4.4.4.6 RX Mode

- PRX device (PRIM_RX=1)

The RX mode is an active mode where the RF radio is configured to be a receiver. To enter this mode from standby-I mode, the PRX device must set PWR_UP_DIG bit high, PRIM_RX bit high and the CE pin high. Or PRX device can enter this mode from TX mode after transmitting an acknowledge packet when EN_AA=1 and NO_ACK=0 in received packet.

In this mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the packet processing engine. The packet processing engine continuously searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFO. If the RX FIFO is full, the received packet will be discarded.

The PRX device remains in RX mode until the MCU configures it to standby-I mode or power down mode.

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- PTX device (PRIM_RX=0)

The PTX device will enter RX mode from TX mode only when EN_AA=1 and NO_ACK=0 to receive acknowledge packets.

4.4.5 Packet Processing

4.4.5.1 Packet Format

The packet format has a preamble, address, packet control, payload and CRC field.

For enhanced packet format, the packet control is 10 bits, and for normal packet format, the packet control is 0 bit.

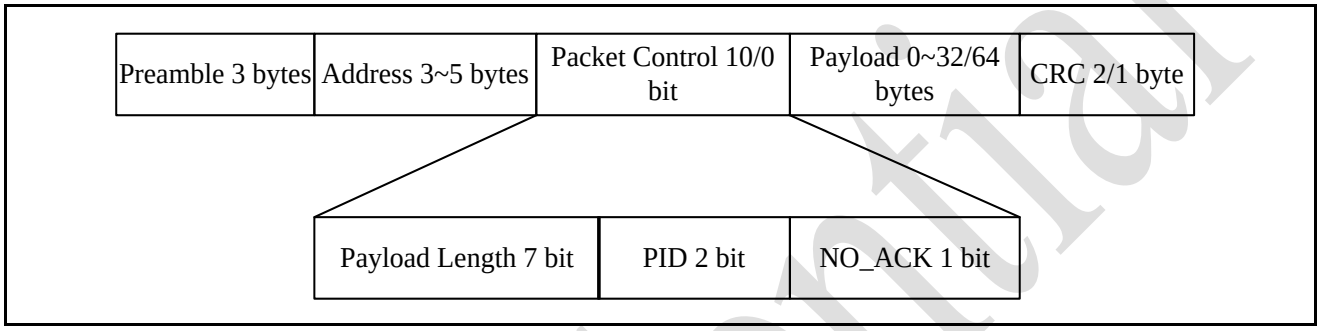

Figure 4-13 Packet Format

- Preamble

The preamble is a bit sequence used to detect 0 and 1 levels in the receiver. The preamble is 3 bytes long and is 0x710F55. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

- Address

This is an address for the receiver to ensure that the packet is detected by the target receiver. The address field can be configured to be 3, 4, or 5 bytes long by the AW register.

The PRX device can be up to six data pipes to support up to six PTX devices with unique addresses. All six PTX device addresses are searched simultaneously. In PRX side, the data pipes are enabled with the bits in theEN_RXADDR register. By default only data pipe 0 are enabled.

Each data pipe address is configured in the RX_ADDR_PX registers.

Each pipe can have up to 5 bytes configurable address. Data pipe 0 and pipe 1 has a unique 5 byte address. Data pipes 2-5 share the 4 most significant address bytes of pipe 1. The LSB byte must be unique for all 6 pipes.

To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet.

On the PRX the RX_ADDR_Pn, defined as the pipe address, must be unique. On the PTX the TX_ADDR must be the same as the RX_ADDR_P0 on the PTX, and as the pipe address for the designated pipe on the PRX.

No other data pipe can receive data until complete packet is received by a data pipe that has detected

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its address. When multiple PTX devices are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

- Packet Control

When Dynamic Payload Length function is enabled, the packet control field contains a 7 bit payload length field, a 2 bit PID (Packet Identity) field and, a 1 bit NO_ACK flag.

- Payload length

The payload length field is only used if the enhance function is enabled.

- PID

The 2 bit PID field is used to detect whether the received packet is new or retransmitted. PID prevents the PRX device from presenting the same payload more than once to the MCU. The PID field is incremented at the TX side for each new packet received. The PID and CRC fields are used by the PRX device to determine whether a packet is old or new. When several data packets are lost on the link, the PID fields may become equal to the last received PID. If a packet has the same PID as the previous packet, BB compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

- NO_ACK

The NO_ACK flag is only used when the auto acknowledgement feature is isused. Setting the flag high, tells the receiver that the packet is not auto acknowledged.

The PTX can set the NO_ACK flag bit in the Packet Control Field with the command: W_TX_PAYLOAD_NOACK. However, the function must first be enabled in the FEATURE register by setting the EN_DYN_ACK bit. When you use this option, the PTX goes directly to standby-I mode after transmitting the packet and the PRX does not transmit an ACK packet when it receives the packet.

- Payload

The payload is the user defined content of the packet. It can be 0 to 64 bytes wide, and it is transmitted on-air as it is uploaded (unmodified) to the device.

The PAN2025 provides two alternatives for handling payload length, static and dynamic payload length. The static payload length of each of the six data pipes can be individually set.

The default option is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the RX_PW_Px registers. The payload length on the transmitter side is set by the number of bytes in the TX_FIFO and must equal the value in the RX_PW_Px register on the receiver side. Each pipe has its own payload length.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets with variable payload length to the receiver. This means that it is not necessary for a system with different payload lengths to scale the packet length to the longest payload.

With DPL feature the PAN2025 can decode the payload length of the received packet automatically instead of using the RX_PW_Px registers. The MCU can read the length of the received payload by using the command: R_RX_PL_WID.

In order to enable DPL the EN_DPL bit in the FEATURE register must be set. In RX mode the DYNPD register must be set. A PTX that transmitted to a PRX with DPL enabled must have the

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DPL_P0 bit in DYNPD set.

- CRC

The CRC is the error detection mechanism in the packet. The number of bytes in the CRC is set by the CRCO bit in the CONFIG register. It may be either 1 or 2 bytes and is calculated over the address, Field, and Payload.

The polynomial for 1 byte CRC is $X^8 + X^2 + X + 1$. Initial value is 0xFF. The polynomial for 2 byte CRC is $X^{16} + X^{12} + X^5 + 1$. Initial value is 0xFFFF.

No packet will be accepted on receiver side if the CRC fails when CRC is enabled.

4.4.5.2 Packet Handling

PAN2025 uses burst mode for payload transmission and receive.

The transmitter fetches payload from TX FIFO, automatically assembles it into packet and transmits the packet in a very short burst period with 1Mbps or 250Kbps air data rate.

After transmission, if the PTX packet has the NO_ACK flag set, PAN2025 sets TX_DS and gives an active low interrupt IRQ to MCU. If the PTX is ACK packet, the PTX needs receive ACK from the PRX and then asserts the TX_DS IRQ.

The receiver automatically validates and disassembles received packets, if there is a valid packet within the new payload, it will write the payload into RX FIFO, set RX_DR and give an active low interrupt IRQ to MCU.

When auto acknowledgement is enabled (EN_AA=1), the PTX device will automatically wait for the acknowledge packet after transmission, and re-transmit the original packet with the delay of ARD until an acknowledge packet is received or the number of re-transmission exceeds a threshold ARC. If the latter happens, PAN2025 will set MAX_RT and give an active low interrupt IRQ to MCU. Two packet loss counters (ARC_CNT and PLOS_CNT) increment every time a packet is lost. The ARC_CNT counts the number of retransmission for the current transaction. The PLOS_CNT counts the total number of retransmissions since the last channel change. ARC_CNT is reset by initiating a new transaction. PLOS_CNT is reset by writing to the RF_CH register. It is possible to use the information in the OBSERVE_TX register to make an overall assessment of the channel quality.

The PTX device will retransmit if its RX FIFO is full but received ACK frame has payload.

As an alternative for PTX device to retransmit automatically, it is possible to manually set the PAN2025 to retransmit a packet several times. This is done by the REUSE_TX_PL command.

When auto acknowledgement is enabled, the PRX device will automatically check the NO_ACK field in the received packet. If NO_ACK=0, it will automatically send an acknowledge packet to PTX device. If EN_ACK_PAY is set, the acknowledge packet can also include pending payload in TX FIFO.

4.4.6 Data and Control Interface

4.4.6.1 TX/RX FIFO

The data FIFOs are used to store payloads that are transmitted (TX FIFO) or payloads that are received and ready to be clocked out (RX FIFO). The FIFOs are accessible in both PTX mode and

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PRX mode.

The following FIFOs are present in PAN2025:

- TX two level 32 byte FIFO or one level 64 byte FIFO
- RX two level 32 byte FIFO or one level 64 byte FIFO

Both FIFOs have a controller and are accessible by using dedicated commands. A TX FIFO in PRX can store payload for ACK packets to two different PTX devices. If the TX FIFO contains more than one payload to a pipe, payloads are handled using the first in first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO by using the FLUSH_TX command.

The users can write payload into TX FIFO in PTX mode by W_TX_PAYLOAD and W_TX_NO_ACK commands. The users also can write payload for ACK packets into TX FIFO in PRX mode by W_ACK_PAYLOAD command. If TX_DS and MAX_RT interruptions happen, payload is cleared in the TX FIFO.

The users can read payload in RX FIFO in PRX mode by R_RX_PAYLOAD command or read ACK payload in RX FIFO in PTX mode by R_RX_PAYLOAD command. In DYNPD mode the length of the payload needs to be read by R_RX_PL_WID command. The payload is cleared in the RX FIFO, while the users can use R_RX_PAYLOAD command to finish reading payload.

In the FIFO_STATUS register it is possible to read if the TX and RX FIFO are full or empty. The TX_REUSE bit is also available in the FIFO_STATUS register. TX_REUSE is set by the command REUSE_TX_PL and is reset by the command W_TX_PAYLOAD or FLUSH_TX.

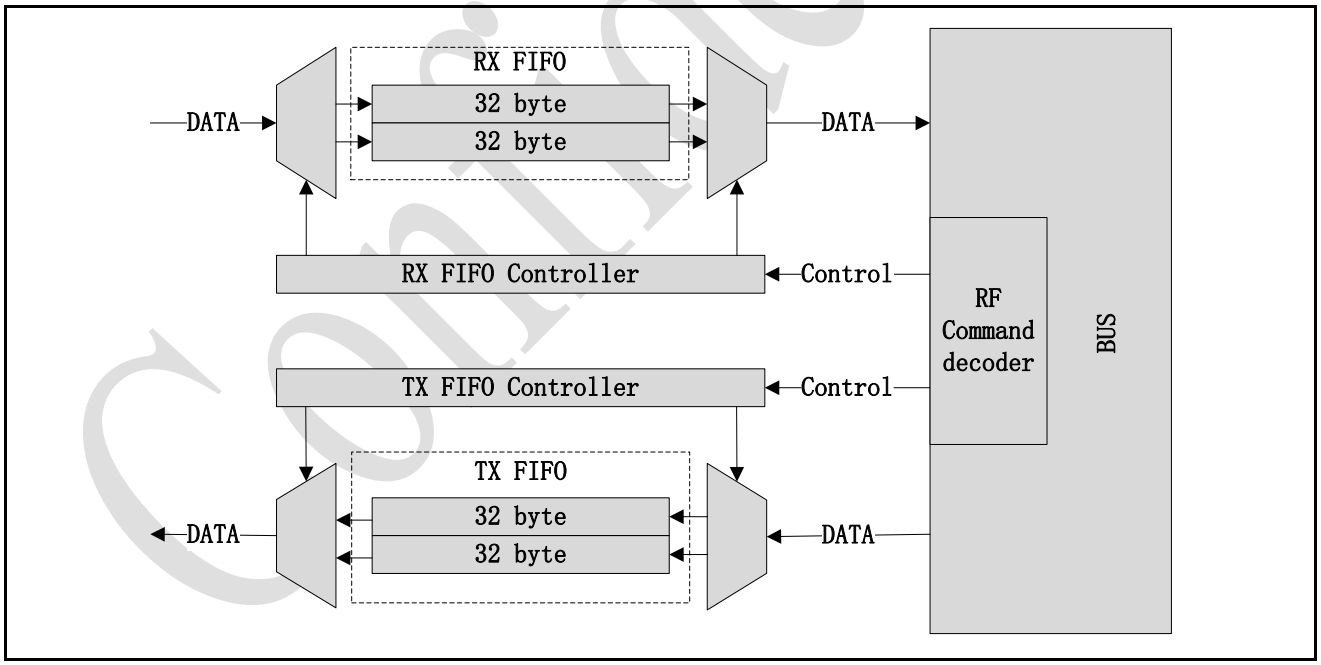

Figure 4-14 FIFO Block Diagram

4.4.6.2 Interrupt

In PAN2025 there is an active low interrupt (IRQ), which is activated when TX_DS IRQ, RX_DR IRQ or MAX_RT IRQ are set high by the state machine in the STATUS register. The IRQ resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the CONFIG register is used to select the IRQ sources that are allowed to assert the IRQ. By setting one of the

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MASK bit high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

The 3 bit pipe information in the STATUS register is updated during the IRQ high to low transition. If the STATUS register is read during an IRQ high to low transition, the pipe information is unreliable.

4.4.7 RF Register Map

Register	Offset	R/W	Description	Reset Value
RF Base Address: **RF_BA = 0x5000_5000**				
CONFIG	RF_BA+0x000	R/W	Configuration register	0x0C
EN_AA	RF_BA+0x004	R/W	RX Auto-reply Enable Register	0x01
EN_RXADDR	RF_BA+0x008	R/W	RX Channel Enable Register	0x01
SETUP_AW	RF_BA+0x00C	R/W	Address Widths Configuration Register	0x03
SETUP_RETR	RF_BA+0x010	R/W	Auto Transmission Configuration Register	0x03
RF_CH	RF_BA+0x014	R/W	RF Channel Configuration Register	0x4E
RF_SETUP	RF_BA+0x018	R/W	RF Parameter Configuration Register	0x00
STATUS	RF_BA+0x01C	R/W	Status Register	0x0E
OBSERVE_TX	RF_BA+0x020	R	Transmit State Register	0x00
DATAOUT_0	RF_BA+0x024	R	Data Read Register0 (used for test)	0x00
DATAOUT_1	RF_BA+0x028	R	Data Read Register1 (used for test)	0x80
DATAOUT_2	RF_BA+0x02C	R	Data Read Register2 (used for test)	0xF8
DATAOUT_3	RF_BA+0x030	R	Data Read Register3 (used for test)	0x0F
RX_ADDR_P0_0	RF_BA+0x034	R/W	Data Pipe0 Receive Address Register0	0xE7
RX_ADDR_P0_1	RF_BA+0x038	R/W	Data Pipe0 Receive Address Register1	0xE7
RX_ADDR_P0_2	RF_BA+0x03C	R/W	Data Pipe0 Receive Address Register2	0xE7
RX_ADDR_P0_3	RF_BA+0x040	R/W	Data Pipe0 Receive Address Register3	0xE7
RX_ADDR_P0_4	RF_BA+0x044	R/W	Data Pipe0 Receive Address Register4	0xE7
RX_ADDR_P1_0	RF_BA+0x048	R/W	Data Pipe1 Receive Address Register0	0xC2
RX_ADDR_P1_1	RF_BA+0x04C	R/W	Data Pipe1 Receive Address Register1	0xC2
RX_ADDR_P1_2	RF_BA+0x050	R/W	Data Pipe1 Receive Address Register2	0xC2
RX_ADDR_P1_3	RF_BA+0x054	R/W	Data Pipe1 Receive Address Register3	0xC2
RX_ADDR_P1_4	RF_BA+0x058	R/W	Data Pipe1 Receive Address Register4	0xC2
RX_ADDR_P2	RF_BA+0x05C	R/W	Data Pipe2 Receive Address Register	0×C3
RX_ADDR_P3	RF_BA+0x060	R/W	Data Pipe3 Receive Address Register	0×C4
RX_ADDR_P4	RF_BA+0x064	R/W	Data Pipe4 Receive Address Register	0×C5
RX_ADDR_P5	RF_BA+0x068	R/W	Data Pipe5 Receive Address Register	0×C6
TX_ADDR_0	RF_BA+0x06C	R/W	Transmit address0	0×E7
TX_ADDR_1	RF_BA+0x070	R/W	Transmit address Register1	0×E7
TX_ADDR_2	RF_BA+0x074	R/W	Transmit address Register2	0×E7
TX_ADDR_3	RF_BA+0x078	R/W	Transmit address Register3	0×E7
TX_ADDR_4	RF_BA+0x07C	R/W	Transmit address Register4	0×E7
RX_PW_P0	RF_BA+0x080	R/W	RX Payload Length of Data Pipe0	0×00

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RX_PW_P1	RF_BA+0x084	R/W	RX Payload Length of Data Pipe1	0×00
RX_PW_P2	RF_BA+0x088	R/W	RX Payload Length of Data Pipe2	0×00
RX_PW_P3	RF_BA+0x08C	R/W	RX Payload Length of Data Pipe3	0×00
RX_PW_P4	RF_BA+0x090	R/W	RX Payload Length of Data Pipe4	0×00
RX_PW_P5	RF_BA+0x094	R/W	RX Payload Length of Data Pipe5	0×00
FIFO_STATUS	RF_BA+0x098	R	FIFO Status Register	0×11
PN006_SET_0	RF_BA+0x09C	R/W	PN006 Demodulator Configuration Register0	0×45
PN006_SET_1	RF_BA+0x0A0	R/W	PN006 Demodulator Configuration Register1	0×7E
PN006_SET_2	RF_BA+0x0A4	R/W	PN006 Demodulator Configuration Register2	0×1B
PN006_SET_3	RF_BA+0×A8	R/W	PN006 Demodulator Configuration Register3	0×FF
PN006_SET_4	RF_BA+0×AC	R/W	PN006 Demodulator Configuration Register4	0×78
PN006_SET_5	RF_BA+0×B0	R/W	PN006 Demodulator Configuration Register5	0×FC
PN006_SET_6	RF_BA+0×B4	R/W	PN006 Demodulator Configuration Register6	0×73
PN006_SET_7	RF_BA+0×B8	R/W	PN006 Demodulator Configuration Register7	0×00
DEMOD_CAL_0	RF_BA+0×BC	R/W	Modem Parameter Register 0	0×05
DEMOD_CAL_1	RF_BA+0×C0	R/W	Demodulator Parameter Register 1	0×41
DEMOD_CAL_2	RF_BA+0×C4	R/W	Demodulator Parameter Register 2	0×7C
DEMOD_CAL_3	RF_BA+0×C8	R/W	Demodulator Parameter Register 3	0×1F
DEMOD_CAL_4	RF_BA+0×CC	R/W	Demodulator Parameter Register 4	0×00
DEMOD_CAL_5	RF_BA+0×D0	R/W	Demodulator Parameter Register 5	0×02
DEMOD_CAL_6	RF_BA+0×D4	R/W	Demodulator Parameter Register 6	0×00
DEMOD_CAL_7	RF_BA+0×D8	R/W	Demodulator Parameter Register 7	0×20
DEMOD_CAL_8	RF_BA+0×DC	R/W	Demodulator Parameter Register 8	0×5A
RF_CAL2_0	RF_BA+0×E0	R/W	Additional RF Register 0	0×08
RF_CAL2_1	RF_BA+0×E4	R/W	Additional RF Register 1	0×C2
RF_CAL2_2	RF_BA+0×E8	R/W	Additional RF Register 2	0×FF
RF_CAL2_3	RF_BA+0×EC	R/W	Additional RF Register 3	0×97
RF_CAL2_4	RF_BA+0×F0	R/W	Additional RF Register 4	0×AB
RF_CAL2_5	RF_BA+0×F4	R/W	Additional RF Register 5	0×42
RF_CAL2_6	RF_BA+0×F8	R/W	Additional RF Register 6	0×FF
RF_CAL2_7	RF_BA+0×FC	R/W	Additional RF Register 7	0×64
RF_CAL2_8	RF_BA+0×100	R/W	Additional RF Register 8	0×CF
RF_CAL2_9	RF_BA+0×104	R/W	Additional RF Register 9	0×24
DEM_CAL2_0	RF_BA+0x108	R/W	Additional Demodulator Register 0	0×91
DEM_CAL2_1	RF_BA+0x10C	R/W	Additional Demodulator Register 1	0×CB
DEM_CAL2_2	RF_BA+0x110	R/W	Additional Demodulator Register 2	0×D3
DEM_CAL2_3	RF_BA+0x114	R/W	Additional Demodulator Register 3	0×BA
DEM_CAL2_4	RF_BA+0x118	R/W	Additional Demodulator Register 4	0×78
DEM_CAL2_5	RF_BA+0x11C	R/W	Additional Demodulator Register 5	0×88
DEM_CAL2_6	RF_BA+0x120	R/W	Additional Demodulator Register 6	0×0B
DEM_CAL2_7	RF_BA+0x124	R/W	Additional Demodulator Register 7	0×A8
DEM_CAL2_8	RF_BA+0x128	R/W	Additional Demodulator Register 8	0×AA

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DYNPD	RF_BA+0x12C	R/W	Dynamic Payload Length Enable Register	0×00
FEATURE	RF_BA+0x130	R/W	Feature Register	0×00
RF_CAL_0	RF_BA+0x134	R/W	RF Parameter Register 0	0×80
RF_CAL_1	RF_BA+0x138	R/W	RF Parameter Register 1	0×02
RF_CAL_2	RF_BA+0x13C	R/W	RF Parameter Register 2	0×A0
RF_CAL_3	RF_BA+0x140	R/W	RF Parameter Register 3	0×88
RF_CAL_4	RF_BA+0x144	R/W	RF Parameter Register 4	0×71
RF_CAL_5	RF_BA+0x148	R/W	RF Parameter Register 5	0×BB
RF_CAL_6	RF_BA+0x14C	R/W	RF Parameter Register 6	0×61
RF_CAL_7	RF_BA+0x150	R/W	RF Parameter Register 7	0×54
RF_CAL_8	RF_BA+0x154	R/W	RF Parameter Register 8	0×61
RF_CAL_9	RF_BA+0x158	R/W	RF Parameter Register 9	0×80
BB_CAL_0	RF_BA+0x15C	R/W	Digital Baseband Parameter Register 0	0×0A
BB_CAL_1	RF_BA+0x160	R/W	Digital Baseband Parameter Register 1	0×6D
BB_CAL_2	RF_BA+0x164	R/W	Digital Baseband Parameter Register 2	0×24
BB_CAL_3	RF_BA+0x168	R/W	Digital Baseband Parameter Register 3	0×24
BB_CAL_4	RF_BA+0x16C	R/W	Digital Baseband Parameter Register 4	0×4E
BB_CAL_5	RF_BA+0x170	R/W	Digital Baseband Parameter Register 5	0×20
BB_CAL_6	RF_BA+0x174	R/W	Digital Baseband Parameter Register 6	0×7F
BB_CAL_7	RF_BA+0x178	R/W	Digital Baseband Parameter Register 7	0×9B
BB_CAL_8	RF_BA+0x17C	R/W	Digital Baseband Parameter Register 8	0×E4
BB_CAL_9	RF_BA+0x180	R/W	Digital Baseband Parameter Register 9	0×00
RF_CE	RF_BA+0x184	R/W	RF CE Register	0×00
RF_CMD	RF_BA+0x188	R/W	RF Command Register	0×00
RF_FIFO	RF_BA+0x18C	R/W	RF FIFO Register	0×00
RF_PL_WIDTH	RF_BA+0x190	R	RF Payload Configuration Register	0×00
CHIP_ID	RF_BA+0x194~0x198	R	Chip Identification Register	0×5051
DEVICE_ID	RF_BA+0x19C~0x1A8	R	Device Identification Register	0x50505050

4.4.8 RF Register Description

4.4.8.1 Configuration register(CONFIG)

Register	Offset	R/W	Description	Reset Value
CONFIG	RF_BA+0x000	R/W	Configuration register	0x0C

Bits	Descriptions	
[7]	EN_PMU_DIG	Baseband main FSM mode selection (Premise PWR_UP_DIG = 1): 1 = main FSM enter STANDBY 0 = main FSM enter POWER_DOWN
[6]	MASK_RX_DR	Mask interrupt caused by RX_DR:

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		1 = Interrupt not reflected on the IRQ pin 0 = Reflect RX_DR as active low interrupt on the IRQ pin
[5]	MASK_TX_DS	Mask interrupt caused by TX_DS: 1 = Interrupt not reflected on the IRQ pin 0 = Reflect TX_DS as active low interrupt on the IRQ pin
[4]	MASK_MAX_RT	Mask interrupt caused by MAX_RT: 1 = Interrupt not reflected on the IRQ pin 0 = Reflect MAX_RT as active low interrupt on theIRQ pin
[3]	EN_CRC	Enable CRC. Forced high if one of the bits in theEN_AA is high. 1 = CRC enabled 0 = CRC disabled
[2]	CRC_SEL	CRC selection: 1 = CRC16 0 = CRC8
[1]	PWR_UP_DIG	Baseband main FSM mode selection (Premise EN_PM_DIG = 1): 1 = main FSM enter STANDBY 0 = main FSM enter POWER_DOWN
[0]	PRIM_RX	RX/TX control: 1 = PRX 0 = PTX

4.4.8.2 RX Auto Acknowledgment Enable Register(EN_AA)

Register	Offset	R/W	Description	Reset Value
EN_AA	RF_BA+0x004	R/W	RX Auto-reply Enable Register	0x01

Bits	Descriptions	
[7:6]	Reserved	Reserved
[5]	ENAA_P5	Enable auto-reply data pipe 5
[4]	ENAA_P4	Enable auto-reply data pipe 4
[3]	ENAA_P3	Enable auto-reply data pipe 3
[2]	ENAA_P2	Enable auto-reply data pipe 2
[1]	ENAA_P1	Enable auto-reply data pipe 1
[0]	ENAA_P0	Enable auto-reply data pipe 0

4.4.8.3 RX Channel Enable Register(EN_RXADDR)

Register	Offset	R/W	Description	Reset Value
EN_RXADDR	RF_BA+0x008	R/W	RX Channel Enable Register	0x01

Bits	Descriptions	
[7:6]	Reserved	Reserved
[5]	ERX_P5	Enable data pipe 5

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[4]	ERX_P4	Enable data pipe 4
[3]	ERX_P3	Enable data pipe 3
[2]	ERX_P2	Enable data pipe 2
[1]	ERX_P1	Enable data pipe 1
[0]	ERX_P0	Enable data pipe 0

4.4.8.4 Address WidthsConfiguration Register(SETUP_AW)

Register	Offset	R/W	Description	Reset Value
SETUP_AW	RF_BA+0x00C	R/W	Address Widths Configuration Register	0x03

Bits	Descriptions	
[7:2]	Reserved	Reserved
[1:0]	AW	RX/TX Address field width: 00 = Illegal 01 = 3 bytes 10 = 4 bytes 11 =5 bytes LS Byte is used if address width is below 5

4.4.8.5 Auto Transmission Configuration Register(SETUP_RETR)

Register	Offset	R/W	Description	Reset Value
SETUP_RETR	RF_BA+0x010	R/W	Auto Transmission Configuration Register	0x03

Bits	Descriptions	
[7:4]	ARD	Auto Retransmit Delay: 0000 = Wait 250μs 0001 = Wait 500μs 0010 = Wait 750μs …….. 1111 = Wait 4000μs (Delay defined from end of transmission to start ofnext transmission)
[3:0]	ARC	Auto Retransmit Count: 0000 =Communication mode without re-transmit, without ACK 0001 = Up to 1 Re-Transmit with ACK …… 1111 = Up to 15 Re-Transmit with ACK

4.4.8.6 RF Channel Configuration Register(RF_CH)

Register	Offset	R/W	Description	Reset Value
RF_CH	RF_BA+0x014	R/W	RF Channel Configuration Register	0x4E

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Bits	Descriptions	
[7]	RF_CH_7	Channel_decorder decimal jitter function. 1 = All the decimal jitter. 0 = If FRA_SPI_IN_EN is set to 1, only 0, 0.5, 0.25, 0.75 are jittered. If FRA_SPI_IN_EN is set to 0, none are jittered.
[6:0]	RF_CH	Sets the frequency channel fc<7:0>= 64+RF_CH<6:0>

4.4.8.7 RF Parameter Configuration Register(RF_SETUP)

Register	Offset	R/W	Description	Reset Value
RF_SETUP	RF_BA+0x018	R/W	RF Parameter Configuration Register	0x00

Bits	Descriptions	
[7:6]	RF_DR	Sets Data Rate: 00 = 1Mbps 01 =Reserved 11 =250Kbps 10 = Reserved
[5]	VCO_NO_DLY	If en_vco_cal is set to 0 and there is a trigger signal, vco_cal_done will change to 0 for a while and no calibration will be executed. If en_vco_cal is set to 1, once the trigger signal comes, vco_cal_done will change to 0 at once. And it starts to calibrate after the delay. After correction, vco_cal_done will return to 1. This process means that the delay time is always valid. If vco_no_dly is set to 1 and en_vco_cal is set to 0, vco_cal_done keeps 1. If en_vco_cal is set, vco_cal_done changes to 0 immediately once the trigger signal comes. At the same time, the correction begins. After the correction ends, vco_cal_done returns to 1. This process means that there is no delay time. This process is illustrated in the following table.

vco_no_dly / en_vco_cal	1	0
0	vco_cal_done keeps 1	-
1	vco_cal_done changes to 0 immediately once the trigger signal comes. At the same time, the correction begins. After the correction ends, vco_cal_done returns to 1.	-

[4]	SEL_CHAN_H	If this bit is set to 0, For RX: fvco=2*(2338+fc<7:0>) INT[8:0]=INT $\left(\frac{fvco}{16M}\right) - 3$ FRA[22:0]=($\frac{fvco}{16M}$-INT($\frac{fvco}{16M}$)) $* 2^{23}$

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		For TX: fvco=2*(2336+fc<7:0>+-delta_f) If this bit is set to 1, For RX: fvco=2*(2252+fc<7:0>) For TX: fvco=2*(2250+fc<7:0>+-delta_f)
[3:0]	Reserved	Reserved

4.4.8.8 Status Register(STATUS)

Register	Offset	R/W	Description	Reset Value
STATUS	RF_BA+0x01C	R/W	Status Register	0x0E

Bits	Descriptions	
[7]	Reserved	Reserved
[6]	RX_DR	Data Ready RX FIFO interrupt. Asserted whennew data arrives RX FIFO. Write 1 to clear bit.
[5]	TX_DS	Data Sent TX FIFO interrupt. In the mode without auto-retransmission, interrupt happens after data complete transmitting. In the mode with auto-retransmission, this bit can only be pulled up after the transmitter has received ACK signal. Write 1 to clear bit.
[4]	MAX_RT	Failed interrupt bit when reaching the maximum transmission times. Write 1 to clear bit. If MAX_RT has been asserted, it mustbe cleared to enable further communication.
[3:1]	RX_P_NO	Data pipe numberread from RX_FIFO (Read-only) 000-101 = Data Pipe Number 110 = Not Used 111 = RX FIFO is empty
[0]	TX_FULL	TX FIFO full flag (Read-only) 1 = TX FIFO is full 0 = Available locations in TX FIFO

4.4.8.9 Transmit State Register(OBSERVE_TX)

Register	Offset	R/W	Description	Reset Value
OBSERVE_TX	RF_BA+0x020	R	Transmit State Register	0x00

Bits	Descriptions	
[7:4]	PLOS_CNT	Packet Loss Counter. The counter stops counting when it reaches a maximum of 15. The counter is reset when writing RF_CH. Communication can continue without resetting this value.
[3:0]	ARC_CNT	Auto-retransmission Times Counter. ARC_CNT adds one when auto-transmit adds one. When ARC_CNT reaches the limitation, it will be regarded as lost package and PLOS_CNT adds one.

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		The counter is resetwhen there is new data written into TX FIFO.

4.4.8.10 Data Read Register0(DATAOUT_0)

Register	Offset	R/W	Description	Reset Value
DATAOUT_0	RF_BA+0x024	R	Data Read Register0 (used for test)	0x00

Bits	Descriptions	
[7:0]	Reserved	Reserved

4.4.8.11 Data Read Register1(DATAOUT_1)

Register	Offset	R/W	Description	Reset Value
DATAOUT_1	RF_BA+0x028	R	Data Read Register1 (used for test)	0x80

Bits	Descriptions	
[7:4]	VCO_CODE	VCO Calibration Results.
[3:0]	Reserved	Reserved

4.4.8.12 Data Read Register2(DATAOUT_2)

Register	Offset	R/W	Description	Reset Value
DATAOUT_2	RF_BA+0x02C	R	Data Read Register2 (used for test)	0xF8

Bits	Descriptions	
[7:4]	RCCAL_OUT[3:0]	RC Calibration Results.
[3:0]	TWO_POINT_CODE	Two-point Calibration Code.

4.4.8.13 Data Read Register3(DATAOUT_3)

Register	Offset	R/W	Description	Reset Value
DATAOUT_3	RF_BA+0x030	R	Data Read Register3 (used for test)	0x0F

Bits	Descriptions	
[7:4]	Reserved	Reserved
[3]	Tp_cal_done	Two-point Calibration End Flag
[2]	Vco_cal_done	VCO Calibration End Flag
[1:0]	RCCAL_OUT[5:4]	RC Calibration Results.

4.4.8.14 Data Pipe0 Receive Address Register0(RX_ADDR_P0_0)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P0_0	RF_BA+0x034	R/W	Data Pipe0 Receive Address Register0	0xE7

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Bits	Descriptions	
[7:0]	RX_ADDR_P0_0	Receive address of data pipe 0. The maximumlength is 5 Bytes. (LS Byte is written first. The address length is defined by SETUP_AW).

4.4.8.15 Data Pipe0 Receive Address Register1(RX_ADDR_P0_1)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P0_1	RF_BA+0x038	R/W	Data Pipe0 Receive Address Register1	0xE7

Bits	Descriptions	
[7:0]	RX_ADDR_P0_1	Receive address of data pipe 0. The maximumlength is 5 Bytes. (LS Byte is written first. The address length is defined by SETUP_AW).

4.4.8.16 Data Pipe0 Receive Address Register2(RX_ADDR_P0_2)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P0_2	RF_BA+0x03C	R/W	Data Pipe0 Receive Address Register2	0xE7

Bits	Descriptions	
[7:0]	RX_ADDR_P0_2	Receive address of data pipe 0. The maximumlength is 5 Bytes. (LS Byte is written first. The address length is defined by SETUP_AW).

4.4.8.17 Data Pipe0 Receive Address Register3(RX_ADDR_P0_3)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P0_3	RF_BA+0x040	R/W	Data Pipe0 Receive Address Register3	0xE7

Bits	Descriptions	
[7:0]	RX_ADDR_P0_3	Receive address of data pipe 0. The maximumlength is 5 Bytes. (LS Byte is written first. The address length is defined by SETUP_AW).

4.4.8.18 Data Pipe0 Receive Address Register4(RX_ADDR_P0_4)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P0_4	RF_BA+0x044	R/W	Data Pipe0 Receive Address Register4	0xE7

Bits	Descriptions	
[7:0]	RX_ADDR_P0_4	Receive address of data pipe 0. The maximumlength is 5 Bytes. (LS Byte is written first. The address length is defined by SETUP_AW).

4.4.8.19 Data Pipe1 Receive Address Register0(RX_ADDR_P1_0)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P1_0	RF_BA+0x048	R/W	Data Pipe1 Receive Address Register0	0xC2

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Bits	Descriptions	
[7:0]	RX_ADDR_P1_0	Receive address of data pipe 1. The maximumlength is 5 Bytes. (LS Byte is written first. The address length is defined by SETUP_AW).

4.4.8.20 Data Pipe1 Receive Address Register1(RX_ADDR_P1_1)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P1_1	RF_BA+0x04C	R/W	Data Pipe1 Receive Address Register1	0xC2

Bits	Descriptions	
[7:0]	RX_ADDR_P1_1	Receive address of data pipe 1. The maximumlength is 5 Bytes. (LS Byte is written first. The address length is defined by SETUP_AW).

4.4.8.21 Data Pipe1 Receive Address Register2(RX_ADDR_P1_2)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P1_2	RF_BA+0x050	R/W	Data Pipe1 Receive Address Register2	0xC2

Bits	Descriptions	
[7:0]	RX_ADDR_P1_2	Receive address of data pipe 1. The maximumlength is 5 Bytes. (LS Byte is written first. The address length is defined by SETUP_AW).

4.4.8.22 Data Pipe1 Receive Address Register3(RX_ADDR_P1_3)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P1_3	RF_BA+0x054	R/W	Data Pipe1 Receive Address Register3	0xC2

Bits	Descriptions	
[7:0]	RX_ADDR_P1_3	Receive address of data pipe 1. The maximumlength is 5 Bytes. (LS Byte is written first. The address length is defined by SETUP_AW).

4.4.8.23 Data Pipe1 Receive Address Register4(RX_ADDR_P1_4)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P1_4	RF_BA+0x058	R/W	Data Pipe1 Receive Address Register4	0xC2

Bits	Descriptions	
[7:0]	RX_ADDR_P1_4	Receive address of data pipe 1. The maximumlength is 5 Bytes. (LS Byte is written first. The address length is defined by SETUP_AW).

4.4.8.24 Data Pipe2 Receive Address Register(RX_ADDR_P2)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P2	RF_BA+0x05C	R/W	Data Pipe2 Receive Address Register	0×C3

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Bits	Descriptions	
[7:0]	RX_ADDR_P2	Receive address of data pipe 2. Only LSB. MS Bytesare equal to RX_ADDR_P1[39:8].

4.4.8.25 Data Pipe3 Receive Address Register(RX_ADDR_P3)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P3	RF_BA+0x060	R/W	Data Pipe3 Receive Address Register	0×C4

Bits	Descriptions	
[7:0]	RX_ADDR_P3	Receive address of data pipe 3. Only LSB. MS Bytesare equal to RX_ADDR_P1[39:8].

4.4.8.26 Data Pipe4 Receive Address Register(RX_ADDR_P4)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P4	RF_BA+0x064	R/W	Data Pipe4 Receive Address Register	0×C5

Bits	Descriptions	
[7:0]	RX_ADDR_P4	Receive address of data pipe 4. Only LSB. MS Bytesare equal to RX_ADDR_P1[39:8].

4.4.8.27 Data Pipe5 Receive Address Register(RX_ADDR_P5)

Register	Offset	R/W	Description	Reset Value
RX_ADDR_P5	RF_BA+0x068	R/W	Data Pipe5 Receive Address Register	0×C6

Bits	Descriptions	
[7:0]	RX_ADDR_P5	Receive address of data pipe 5. Only LSB. MS Bytesare equal to RX_ADDR_P1[39:8].

4.4.8.28 Transmit address Register0(TX_ADDR_0)

Register	Offset	R/W	Description	Reset Value
TX_ADDR_0	RF_BA+0x06C	R/W	Transmit address Register0	0×E7

Bits	Descriptions	
[7:0]	TX_ADDR_0	Transmit address. (LS Byte is written first) Used in the PTX mode only. RX_ADDR_P0_0is equal to this address in order to receive ACK automatic response.

4.4.8.29 Transmit address Register1(TX_ADDR_1)

Register	Offset	R/W	Description	Reset Value

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TX_ADDR_1	RF_BA+0x070	R/W	Transmit address Register1	0×E7

Bits	Descriptions	
[7:0]	TX_ADDR_1	Transmit address. (LS Byte is written first) Used in the PTX mode only. RX_ADDR_P0_1is equal to this address in order to receive ACK automatic response.

4.4.8.30 Transmit address Register2(TX_ADDR_2)

Register	Offset	R/W	Description	Reset Value
TX_ADDR_2	RF_BA+0x074	R/W	Transmit address Register2	0×E7

Bits	Descriptions	
[7:0]	TX_ADDR_2	Transmit address. (LS Byte is written first) Used in the PTX mode only. RX_ADDR_P0_2is equal to this address in order to receive ACK automatic response.

4.4.8.31 Transmit address Register3(TX_ADDR_3)

Register	Offset	R/W	Description	Reset Value
TX_ADDR_3	RF_BA+0x078	R/W	Transmit address Register3	0×E7

Bits	Descriptions	
[7:0]	TX_ADDR_3	Transmit address. (LS Byte is written first) Used in the PTX mode only. RX_ADDR_P0_3is equal to this address in order to receive ACK automatic response.

4.4.8.32 Transmit address Register4(TX_ADDR_4)

Register	Offset	R/W	Description	Reset Value
TX_ADDR_4	RF_BA+0x07C	R/W	Transmit address Register4	0×E7

Bits	Descriptions	
[7:0]	TX_ADDR_4	Transmit address. (LS Byte is written first) Used in the PTX mode only. RX_ADDR_P0_4is equal to this address in order to receive ACK automatic response.

4.4.8.33 RX Payload Length of Data Pipe0(RX_PW_P0)

Register	Offset	R/W	Description	Reset Value
RX_PW_P0	RF_BA+0x080	R/W	RX Payload Length of Data Pipe0	0×00

Bits	Descriptions

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[7]	Reserved	Reserved
[6:0]	RX_PW_P0	RX Payload Length of Data Pipe 0 (1 to32/64 bytes). 0 = Not used 1 = 1 byte … 32/64 = 32/64 bytes

4.4.8.34 RX Payload Length od Data Pipe1(RX_PW_P1)

Register	Offset	R/W	Description	Reset Value
RX_PW_P1	RF_BA+0x084	R/W	RX Payload Length of Data Pipe1	0×00

Bits	Descriptions	
[7]	Reserved	Reserved
[6:0]	RX_PW_P1	RX Payload Length of Data Pipe 1 (1 to32/64 bytes). 0 = Not used 1 = 1 byte … 32/64 = 32/64 bytes

4.4.8.35 RX Payload Length of Data Pipe2(RX_PW_P2)

Register	Offset	R/W	Description	Reset Value
RX_PW_P2	RF_BA+0x088	R/W	RX Payload Length of Data Pipe2	0×00

Bits	Descriptions	
[7]	Reserved	Reserved
[6:0]	RX_PW_P2	RX Payload Length of Data Pipe 2 (1 to32/64 bytes). 0 = Not used 1 = 1 byte … 32/64 = 32/64 bytes

4.4.8.36 RX Payload Length of Data Pipe3(RX_PW_P3)

Register	Offset	R/W	Description	Reset Value
RX_PW_P3	RF_BA+0x08C	R/W	RX Payload Length of Data Pipe3	0×00

Bits	Descriptions	
[7]	Reserved	Reserved
[6:0]	RX_PW_P3	RX Payload Length of Data Pipe 3 (1 to32/64 bytes). 0 = Not used 1 = 1 byte …

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		32/64 = 32/64 bytes

4.4.8.37 RX Payload Length of Data Pipe4(RX_PW_P4)

Register	Offset	R/W	Description	Reset Value
RX_PW_P4	RF_BA+0x090	R/W	RX Payload Length of Data Pipe4	0×00

Bits	Descriptions	
[7]	Reserved	Reserved
[6:0]	RX_PW_P4	RX Payload Length of Data Pipe 4 (1 to32/64 bytes). 0 = Not used 1 = 1 byte … 32/64 = 32/64 bytes

4.4.8.38 RX Payload Length of Data Pipe5(RX_PW_P5)

Register	Offset	R/W	Description	Reset Value
RX_PW_P5	RF_BA+0x094	R/W	RX Payload Length of Data Pipe5	0×00

Bits	Descriptions	
[7]	Reserved	Reserved
[6:0]	RX_PW_P5	RX Payload Length of Data Pipe 5 (1 to32/64 bytes). 0 = Not used 1 = 1 byte … 32/64 = 32/64 bytes

4.4.8.39 FIFO Status Register(FIFO_STATUS)

Register	Offset	R/W	Description	Reset Value
FIFO_STATUS	RF_BA+0x098	R	FIFO Status Register	0×11

Bits	Descriptions	
[7]	Reserved	Reserved
[6]	TX_REUSE	Call The Instruction Bit Of The Last Frame Transmission Data If command REUSE_TX_PL is used, this bit is set. The last frame data will be retransmitted. It can be reset by the commandsW_TX_PAYLOAD,W_TX_PAYLOAD_NO-ACK, DEACTIVATE and FLUSH_TX.
[5]	TX_FULL	TX FIFO Full Flag. 1 = TX FIFO is full. 0 = Available locationsin TX FIFO.
[4]	TX_EMPTY	TX FIFO Empty Flag:

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		1 = TX FIFO is empty 0 =There are data in TX FIFO
[3:2]	Reserved	Reserved
[1]	RX_FULL	RX FIFO Full Flag: 1 = RX FIFO is full 0 =Available locationsin RX FIFO
[0]	RX_EMPTY	RX FIFO Empty Flag. 1 = RX FIFO is empty 0 = There are data in RX FIFO

4.4.8.40 PN006 Demodulator Configuration Register0(PN006_SET_0)

Register	Offset	R/W	Description	Reset Value
PN006_SET_0	RF_BA+0×9C	R/W	PN006 Demodulator Configuration Register0	0×45

Bits	Descriptions	
[7]	SAR_ADC_CLK_RISING_SEL	SAR ADC Data Sampling Clock Selection 1 =Rising edge sampling 0 = Falling edge sampling
[6]	AGGRESSIVE	Demodulator Data Rate Synchronization Unit Speed Selection 1 =Large step adjustment, fast 0 = Small step adjustment, slow
[5:0]	GAIN2	Demodulator data center value adjusts the amplitude of the loop's reference waveform.

4.4.8.41 PN006 Demodulator Configuration Register1(PN006_SET_1)

Register	Offset	R/W	Description	Reset Value
PN006_SET_1	RF_BA+0×A0	R/W	PN006 Demodulator Configuration Register1	0×7E

Bits	Descriptions	
[7]	DEMOD_TEST	Demodulator test.
[6:4]	TX_DIV2_BIAS_TAIL[2:0]	VCO%2 Control
[3:0]	GAIN1	Demodulator's data center value adjusts the amplitude of the loop's reference waveform.

4.4.8.42 PN006 Demodulator Configuration Register2(PN006_SET_2)

Register	Offset	R/W	Description	Reset Value
PN006_SET_2	RF_BA+0×A4	R/W	PN006 Demodulator Configuration Register2	0×1B

Bits	Descriptions	
[7]	DSSS_EN	DSSS Modulation Selection Bit 0 =GFSK mode (XN297L mode)

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		1 =DSSS mode (PAN2412 mode)
[6]	Reserved	Reserved
[5:2]	PTH	Preamble Threshold Configuration for the Receiver Digital Demodulator. 24bits preamble threshold = PTH + 16 1000 = 24bits 0110 = 22bits 0000 = 16bits
[1]	DECODE_INV	Preamble Bitwise Inverse Bit. It's set to 1 usually. Transmitter and receiver both need to be executed. 1 = Not Bitwise inversed. 0 = Bitwise inversed.
[0]	SYNC_SEL	4 times sampling

4.4.8.43 PN006 Demodulator Configuration Register3(PN006_SET_3)

Register	Offset	R/W	Description	Reset Value
PN006_SET_3	RF_BA+0×A8	R/W	PN006 Demodulator Configuration Register3	0×FF

Bits	Descriptions	
[7:5]	PA1ST_GC_CTL[2:0]	Control the output of each bit of PA1ST_GC 0 = Corresponding bit output 0 1 = Corresponding bit output 1
[4:2]	PA2ST_RAMP_CTL[2:0]	Control the output of each bit of PA2ST_GC 0 = Corresponding bit output 0 1 = Corresponding bit output 1
[1:0]	Reserved	Reserved

4.4.8.44 PN006 Demodulator Configuration Register4(PN006_SET_4)

Register	Offset	R/W	Description	Reset Value
PN006_SET_4	RF_BA+0×AC	R/W	PN006 Demodulator Configuration Register4	0×78

Bits	Descriptions	
[7:6]	DATA_OFF_TIME[1:0]	Time interval between TX DATA ending and EN_PAO pull-down: DATA_OFF_TIME[1:0] × 1, unit is us. Range: [0,15]us. Default value: 1us
[5:4]	PAOUT_SET_TIME[1:0]	Time interval between EN_PAO pull-up and TRX pull-up: PAOUT_SET_TIME[1:0] × 1, unit is us. Range: [0,3]us. Default value: 3us
[3:0]	PA2_SET_TIME[3:0]	Time interval between EN_PA2ST pull-up and EN_PAO pull-up: PA2_SET_TIME[3:0] × 16, unit is us. Range: [0,240]us.

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		Default value: 128us

4.4.8.45 PN006 Demodulator Configuration Register5(PN006_SET_5)

Register	Offset	R/W	Description	Reset Value
PN006_SET_5	RF_BA+0×B0	R/W	PN006 Demodulator Configuration Register5	0×FC

Bits	Descriptions	
[7:6]	PA1OFF_TIME[1:0]	Time interval between EN_PA2ST pull-down and EN_PA1ST pull-down: PA1OFF_TIME[1:0] × 2, unit is us. Range: [0,30]us. Default value: 30us
[5:2]	PA2OFF_TIME[3:0]	Time interval between EN_PAO pull-down and EN_PA2ST pull-down: PA2OFF_TIME[3:0] × 2, unit is us. Range: [0,30]us. Default value: 30us
[1:0]	DATA_OFF_TIME[3:2]	Time interval between TX DATA ending and EN_PAO pull-down: DATA_OFF_TIME[3:2] × 1, unit is us. Range: [0,15]us. Default value: 1us

4.4.8.46 PN006 Demodulator Configuration Register6(PN006_SET_6)

Register	Offset	R/W	Description	Reset Value
PN006_SET_6	RF_BA+0×B4	R/W	PN006 Demodulator Configuration Register6	0×73

Bits	Descriptions	
[7]	Reserved	Reserved
[6:4]	PA2ST_BC_CTL[2:0]	Control the output of each bit of PA2ST_BC 0 = Corresponding bit output 0 1 = Corresponding bit output 1
[3:2]	Reserved	Reserved
[1:0]	PA1OFF_TIME[3:2]	Time interval between EN_PA2ST pull_down and EN_PA1ST pull-down: PA1OFF_TIME[3:2] × 1, unit is us. Range: [0,30]us. Default value: 30us

4.4.8.47 PN006 Demodulator Configuration Register7(PN006_SET_7)

Register	Offset	R/W	Description	Reset Value
PN006_SET_7	RF_BA+0×B8	R/W	PN006 Demodulator Configuration Register7	0×00

Bits	Descriptions	
[7:0]	Reserved	Reserved

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4.4.8.48 Demodulator Parameter Register0(DEMOD_CAL_0)

Register	Offset	R/W	Description	Reset Value
DEMOD_CAL_0	RF_BA+0×BC	R/W	Modem Parameter Register 0	0×05

Bits	Descriptions	
[7:5]	GAUSS_SCALE[2:0]	Gauss Filter Output to Delta-Sigma Signal Size Adjustment. The output signal size determines the size of the transmit modulation frequency offset. 1111 = Small signal … 1000 = Medium signal … 0000 = Large signal
[4]	EN_PA1ST_TST	When chip_mode=1, EN_PA1ST is controlled by this bit.
[3]	EN_TX_TST	When chip_mode=1, EN_TX is controlled by this bit.
[2]	FRA_SPI_IN_EN	This bit only work when RF_CH_7=0: 0=No dithering. 1 =Some special frequencys add dithering.
[1]	EN_TX_SYN_TST	When chip_mode=1, EN_TX_SYN is controlled by this bit.
[0]	SCR_EN	Scrambling Enable Bit. 0 = Scrambling disabled. 1 = Scrambling enabled.

4.4.8.49 Demodulator Parameter Register 1(DEMOD_CAL_1)

Register	Offset	R/W	Description	Reset Value
DEMOD_CAL_1	RF_BA+0×C0	R/W	Demodulator Parameter Register 1	0×41

Bits	Descriptions	
[7]	TP_CODE_OFFSET[0]	Two-point correction offset (with signed number) 000 = 0 100 = -4 001 = 3 111 = -1
[6]	EN_VCO_CAL	VCO Auto Calibration Enable Bit. VCO Auto Calibration means every code from calibration will be reserved in the internal register. 1 = Enabled. VCO Auto calibration executes if trigger condition meets. 0 = Disabled. Code are configured by MANUL_VCO_CODE.
[5:4]	SYNC_BYPASS	Control whether dig2's synchronizer is by_pass
[3]	EN_PA2ST_TST	When chip_mode=1, EN_PA2ST is controlled by this bit.
[2:1]	GAUSS_CTRL	Transmit Way Selection.

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		gauss_inbgauss_outb 11 = dac_basalNormal output 10 = Normal outputdac_basal2 01 = dac_basalNormal output 00 = Normal outputNormal output Global Transmit Way Selection 11 = Open-loop out of band 10 = In band 01 = Closed loop out of band 00 =Two point
[0]	GAUSS_SCALE[3]	Gauss Filter Output to Delta-Sigma Signal Size Adjustment. The output signal size determines the size of the transmit modulation frequency offset. 1111 = Small signal … 1000 = Medium signal … 0000 = Large signal

4.4.8.50 Demodulator Parameter Register 2(DEMOD_CAL_2)

Register	Offset	R/W	Description	Reset Value
DEMOD_CAL_2	RF_BA+0×C4	R/W	Demodulator Parameter Register 2	0×7C

Bits	Descriptions	
[7:2]	DAC_BASAL_INBAND	GF2(in band) output data initial value in pre-send phase.
[1:0]	TP_CODE_OFFSET[2:1]	Two-point correction offset (with signed number) 000 = 0 100 = -4 001 = 3 111 = -1

4.4.8.51 Demodulator Parameter Register 3(DEMOD_CAL_3)

Register	Offset	R/W	Description	Reset Value
DEMOD_CAL_3	RF_BA+0×C8	R/W	Demodulator Parameter Register 3	0×1F

Bits	Descriptions	
[7]	SHIFT_OFFSET	PLL Delta-Sigma Modulator Shift Offset Enable Bit. 1 = Enabled 0 = Disabled
[6]	INT_MODE_EN	PLL Operation Mode Selection 1 = Integer mode 0 = Decimal mode

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[5:0]	DAC_BASAL_OUTBAND	GF1(out of band) output to DAC initial value in pre-send mode.

4.4.8.52 Demodulator Parameter Register 4(DEMOD_CAL_4)

Register	Offset	R/W	Description	Reset Value
DEMOD_CAL_4	RF_BA+0×CC	R/W	Demodulator Parameter Register 4	0×00

Bits	Descriptions	
[7:6]	CTL_DITHER_LSB[1:0]	PLL Delta-Sigma Modulator Jitter Coefficient Configuration. 111 = Coefficient is 7 000 = Coefficient is 0
[5]	CTL_DITHER_SHAPE	PLL Delta-Sigma Modulator Jitter Module Enable Bit. 1 = Enabled 0 = Disabled
[4]	DIV2_EN	PLL Delta-Sigma Modulator Divided by 2 Module Enable Bit. 1 = Enabled 0 = Disabled
[3]	DS_SHIFT	PLL Delta-Sigma Modulator Shift Enable Bit. 1 = Enabled 0 = Disabled
[2]	INV_CLK_EN	PLL Delta-Sigma Modulator Reverse Working Mode Enable Bit. 1 = Enabled 0 = Disabled
[1]	MASH2_MODE	PLL Delta-Sigma Modulator mash2 Mode Enable Bit. 1 = Enabled 0 = Disabled
[0]	Reserved	Reserved

4.4.8.53 Demodulator Parameter Register 5(DEMOD_CAL_5)

Register	Offset	R/W	Description	Reset Value
DEMOD_CAL_5	RF_BA+0×D0	R/W	Demodulator Parameter Register 5	0×02

Bits	Descriptions	
[7:5]	GAUSS_INBAND_DELAY[2:0]	In Band Transmit Delay Adjustment. 11111 = Long delay 00000 = Short delay
[4]	CHIP_MODE	Chip Enter Test Mode Configuration 1 = Enter test mode 0 = Exit test mode
[3]	CARR_MOSI	Substitute MOSI, single carrier enters. 1 = Enabled
[2]	CARR_CSK	Substitute CSK, single carrier enters. 1 = Enabled

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[1]	CLK_EN	PLL Delta-Sigma Modulator Clock Enable Bit. 1 = Enabled 0 =Disabled
[0]	CTL_DITHER_LSB[2]	PLL Delta-Sigma Modulator Jitter Coefficient Configuration. 111 = Coefficient is 7 000 = Coefficient is 0

4.4.8.54 Demodulator Parameter Register 6(DEMOD_CAL_6)

Register	Offset	R/W	Description	Reset Value
DEMOD_CAL_6	RF_BA+0×D4	R/W	Demodulator Parameter Register 6	0×00

Bits	Descriptions	
[7:3]	GAUSS_OUTBAND_DELAY[4:0]	Out of Band Transmit Delay Adjustment. 11111 = Long delay 00000 = Short delay
[2]	Reserved	Reserved
[1:0]	GAUSS_INBAND_DELAY[4:3]	In Band Transmit Delay Adjustment. 11111 = Long delay 00000 = Short delay

4.4.8.55 Demodulator Parameter Register 7(DEMOD_CAL_7)

Register	Offset	R/W	Description	Reset Value
DEMOD_CAL_7	RF_BA+0×D8	R/W	Demodulator Parameter Register 7	0×20

Bits	Descriptions	
[7]	PHASE_ADJ	Adjust the sampling phase of the transmitted data by the 16M clock in gauss_filter.
[6]	TWO_POINT_SPI_TRIG	Two Point Calibration SPI Trigger Signal. This bit is falling-edge triggered.
[5:2]	TWO_POINT_MANUL_CODE_IN	Two Point Calibration Manual Code Configuration.
[1]	EN_TWO_POINT_CAL	Two Point Transmit Auto Calibration Enable Bit. 1 = Enabled. The values are stored in TWO_POINT_CODE_REG. 0 = Disabled.It can't calibrate automatically. Note: Auto cal needs to be performed in STB2 state.
[0]	Reserved	Reserved

4.4.8.56 Demodulator Parameter Register 8(DEMOD_CAL_8)

Register	Offset	R/W	Description	Reset Value
DEMOD_CAL_8	RF_BA+0×DC	R/W	Demodulator Parameter Register 8	0×5A

Bits	Descriptions

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[7]	SPI_CAL_EN	VCO single trigger automatic correction process. Each time the bit is set from 0 to 1, automatic VCO correction process starts. In addition, when changing the working channel, switching chip working mode and entering transceiver state, the VCO automatic calibration process will also be triggered.
[6]	FAST_LOCK_EN	PLL fast lock mode enable bit 1 = Enabled 0 = Disabled.
[5:0]	DF_SEL	Adjust the in-band deviation use with GAUS_SCALE_INBAND 111111 = Big deviation 000000 = Small deviation

4.4.8.57 Additional RF Register 0 (RF_CAL2_0)

Register	Offset	R/W	Description	Reset Value
RF_CAL2_0	RF_BA+0×E0	R/W	Additional RF Register 0	0×08

Bits	Descriptions	
[7:4]	RCCAL_IN[3:0]	IF Correction Bit of Receiving Bandpass Filter.Only valid when RCCAL_EN = 0. 111111: Low IF center frequency 000000: High IF center frequency
[3]	EN_PLL_DIV2	
[2]	EN_TST_BUF	
[1:0]	Reserved	Reserved

4.4.8.58 Additional RF Register 1 (RF_CAL2_1)

Register	Offset	R/W	Description	Reset Value
RF_CAL2_1	RF_BA+0×E4	R/W	Additional RF Register 1	0×C2

Bits	Descriptions	
[7]	EN_PLL_PRE	
[6]	EN_TX_DAC	
[5]	Reserved	Reserved
[4]	EN_RSSI	
[3:2]	Reserved	Reserved
[1:0]	RCCAL_IN[5:4]	IF Correction Bit of Receiving Bandpass Filter.Only valid when RCCAL_EN = 0. 111111: Low IF center frequency 000000: High IF center frequency

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4.4.8.59 Additional RF Register 2 (RF_CAL2_2)

Register	Offset	R/W	Description	Reset Value
RF_CAL2_2	RF_BA+0×E8	R/W	Additional RF Register 2	0×FF

Bits	Descriptions	
[7]	EN_RX_PGA	
[6]	EN_RX_LIMITER	
[5]	Reserved	
[4]	EN_PLL_IB	
[3]	EN_PLL_PFD	
[2]	EN_PLL_CP	
[1]	EN_PLL_LPF	
[0]	EN_PLL_VCO	

4.4.8.60 Additional RF Register 3 (RF_CAL2_3)

Register	Offset	R/W	Description	Reset Value
RF_CAL2_3	RF_BA+0×EC	R/W	Additional RF Register 3	0×97

Bits	Descriptions	
[7]	RSSI_DC_CTL[0]	Signal Intensity Indicating Signal.
[6:4]	Reserved	
[3]	EN_RCCAL	
[2]	EN_RX_LNA	
[1]	EN_RX_MIX	
[0]	EN_RX_MIX_DIV2	

4.4.8.61 Additional RF Register 4 (RF_CAL2_4)

Register	Offset	R/W	Description	Reset Value
RF_CAL2_4	RF_BA+0×F0	R/W	Additional RF Register 4	0×AB

Bits	Descriptions	
[7]	RCCAL_CKINV	RC Calibration Clock Inverse Bit. 1 = Inversed. 0 = Not inversed.
[6]	RCCAL_SEL	RC Calibration Selection 1 = Manual RC calibration 0 = Auto RC calibration
[5]	RCCAL_START	RC Calibration Start Control Bit.
[4:1]	Reserved	Reserved

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[0]	RSSI_DC_CTL[1]	Signal Intensity Indicating Signal.

4.4.8.62 Additional RF Register 5 (RF_CAL2_5)

Register	Offset	R/W	Description	Reset Value
RF_CAL2_5	RF_BA+0×F4	R/W	Additional RF Register 5	0×42

Bits	Descriptions	
[7]	Reserved	Reserved
[6]	EN_RX_BPF	
[5]	RX_BPF_IB_CTL	Filter's Current Control Bit 0 = Small current 1 = Big current
[4]	RX_CHO_SEL_BPF	IF Filter Output
[3]	BYP_FT	PLL Loop Filter Outside, Internal Filter Disconnected 1 = Internal filter disconnected 0 = Internal filter connected
[2]	RX_CHO_SEL_MIX	IF BUF Output after MIX is chosen.
[1:0]	RX_CAP_CTL[1:0]	Coarse Tuning Filter Capacitor Array

4.4.8.63 Additional RF Register 6 (RF_CAL2_6)

Register	Offset	R/W	Description	Reset Value
RF_CAL2_6	RF_BA+0×F8	R/W	Additional RF Register 6	0×FF

Bits	Descriptions	
[7]	RX_MIX_IQS	Mixer IQ channel switch.
[6]	RX_MIX_GC	Mixer Gain Adjustment 1 = High gain 0 = Low gain
[5:4]	RX_PGA_GC[1:0]	PGA Gain Adjustment 11 = High gain
[3]	Reserved	Reserved
[2:0]	RX_BPF_GC_CTL[2:0]	IF Filter Gain Control 000 = Minimal 111 = Maximal

4.4.8.64 Additional RF Register 7 (RF_CAL2_7)

Register	Offset	R/W	Description	Reset Value
RF_CAL2_7	RF_BA+0×FC	R/W	Additional RF Register 7	0×64

Bits	Descriptions	
[7]	Reserved	Reserved

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[6]	RX_MIXER_IB_CTL	Mixer Current Control 0 = Current half
[5:3]	RX_MIX_DIV2_IB[2:0]	Mixer DIV2 current selection which control the bias level.
[2:0]	RX_MIX_DIV2_ISEL[2:0]	Mixer DIV2 Current Selection

4.4.8.65 Additional RF Register 8 (RF_CAL2_8)

Register	Offset	R/W	Description	Reset Value
RF_CAL2_8	RF_BA+0×100	R/W	Additional RF Register 8	0×CF

Bits	Descriptions	
[7]	PLL_LPF_CP	PLL Filter Cp Selection 0 = 8pF 1 = 16pF
[6]	PLL_TX_CTK	VCO Modulator Frequency Offset Bandwidth Selection 0 = 1MHz bandwidth 1 = 2 MHz bandwidth
[5:4]	RX_LNA_CTM[1:0]	LNA Gain Peak Frequency Adjustment
[3:2]	RX_LNA_GC[1:0]	LNA Gain Adjustment
[1]	RX_LNA_IB_CTL	LNA Current Selection 0 = Current half
[0]	Reserved	Reserved

4.4.8.66 Additional RF Register 9 (RF_CAL2_9)

Register	Offset	R/W	Description	Reset Value
RF_CAL2_9	RF_BA+0×104	R/W	Additional RF Register 9	0×24

Bits	Descriptions	
[7:6]	Reserved	Reserved
[5:3]	RX_BALUN_CTM_M	LNA_DC control
[2:0]	RX_BALUN_CTM_N	Balun CTM Adjustment N Node

4.4.8.67 Additional Demodulator Register 0 (DEM_CAL2_0)

Register	Offset	R/W	Description	Reset Value
DEM_CAL2_0	RF_BA+0x108	R/W	Additional Demodulator Register 0	0×91

Bits	Descriptions	
[7:0]	THRESHOLD	Demodulator Code Synchronization Threshold

4.4.8.68 Additional Demodulator Register 1 (DEM_CAL2_1)

Register	Offset	R/W	Description	Reset Value

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DEM_CAL2_1	RF_BA+0x10C	R/W	Additional Demodulator Register 1	0×CB

Bits	Descriptions	
[7:1]	PAYLOAD_SP	Data Field Spreading Code
[0]	CHIP_INV	0 = Chip not inversed. 1 = Chip inversed.(0->1;1->0)

4.4.8.69 Additional Demodulator Register 2 (DEM_CAL2_2)

Register	Offset	R/W	Description	Reset Value
DEM_CAL2_2	RF_BA+0x110	R/W	Additional Demodulator Register 2	0×D3

Bits	Descriptions	
[7]	PREAMBLE[0]	Preamble code
[6:0]	PREAMBLE_SP	Preamble field spreading code

4.4.8.70 Additional Demodulator Register 3 (DEM_CAL2_3)

Register	Offset	R/W	Description	Reset Value
DEM_CAL2_3	RF_BA+0x114	R/W	Additional Demodulator Register 3	0×BA

Bits	Descriptions	
[7:0]	PREAMBLE[8:1]	Preamble Code

4.4.8.71 Additional Demodulator Register 4 (DEM_CAL2_4)

Register	Offset	R/W	Description	Reset Value
DEM_CAL2_4	RF_BA+0x118	R/W	Additional Demodulator Register 4	0×78

Bits	Descriptions	
[7:0]	PREAMBLE[16:9]	Preamble Code

4.4.8.72 Additional Demodulator Register 5 (DEM_CAL2_5)

Register	Offset	R/W	Description	Reset Value
DEM_CAL2_5	RF_BA+0x11C	R/W	Additional Demodulator Register 5	0×88

Bits	Descriptions	
[7:0]	PREAMBLE[24:17]	Preamble Code

4.4.8.73 Additional Demodulator Register 6 (DEM_CAL2_6)

Register	Offset	R/W	Description	Reset Value
DEM_CAL2_6	RF_BA+0x120	R/W	Additional Demodulator Register 6	0×0B

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<table>
<tr><th>Bits</th><th>Descriptions</th><th></th></tr>
<tr><td>[7]</td><td>PIN[0]</td><td>Output PIN Configuration after Chip Enterring Test Mode(MISO/IRQ pin)
<table>
<tr><th>CHIP / PIN</th><th>0</th><th>1</th></tr>
<tr><td>000</td><td>Working mode.
As data input or interrupt output pin.</td><td>Test sensitivity mode.
As demodulator data or clock output pin.</td></tr>
<tr><td>110</td><td>-</td><td>Test receive mode.
As limit I and Q two way output pin.</td></tr>
</table></td></tr>
<tr><td>[6]</td><td>EN_RX</td><td>RX and PLL Simultaneous Opening.
1 = Simultaneous open
0 = Asynchronous open</td></tr>
<tr><td>[5]</td><td>DELAY1</td><td>PLL Open Loop Enable Bit.
PLLopen-loop state can be used as carrier drift test for transmission.
1 = PLL open-loop enabled
0 =PLL open-loop controlled by state machine.</td></tr>
<tr><td>[4]</td><td>DELAY0</td><td>Whether Demodulator Superimpose the Received Initial Offset.
The demodulator doesn’t superimpose the initial offset which cantest receiver sensitivity.
1 = Not superimpose the initial offset
0 = Superimpose the initial offset. Error code caused by center frequency offset can be cancelled in receiving state.</td></tr>
<tr><td>[3]</td><td>TH1</td><td>In standby-II mode, LDO(except LDO of DVDD) Enable Bit.
In test mode, this bit is set to 1 when testing transmit single carrier and receive sensitivity
1 = Enabled
0 = Disabled</td></tr>
<tr><td>[2:0]</td><td>PREAMBLE[27:25]</td><td>Preamble code</td></tr>
</table>

4.4.8.74 Additional Demodulator Register 7 (DEM_CAL2_7)

Register	Offset	R/W	Description	Reset Value
DEM_CAL2_7	RF_BA+0x124	R/W	Additional Demodulator Register 7	0×A8

<table>
<tr><th>Bits</th><th>Descriptions</th><th></th></tr>
<tr><td>[7:2]</td><td>FRA_SPI_IN[5:0]</td><td></td></tr>
<tr><td>[1:0]</td><td>PIN[2:1]</td><td>Output PIN Configuration after Chip Entering Test Mode(MISO/IRQ pin)
<table>
<tr><th>CHIP / PIN</th><th>0</th><th>1</th></tr>
<tr><td>000</td><td>Working mode.</td><td>Test sensitivity mode.
As demodulator data or clock</td></tr>
</table></td></tr>
</table>

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			As data input or interrupt output pin.	output pin.
		110	-	Test receive mode. As limit I and Q two way output pin.

4.4.8.75 Additional Demodulator Register 8 (DEM_CAL2_8)

Register	Offset	R/W	Description	Reset Value
DEM_CAL2_8	RF_BA+0x128	R/W	Additional Demodulator Register 8	0×AA

Bits	Descriptions	
[7:6]	VCO_DLY_SEL	The delay from vco_cal triggered to started. That is, the charging time for the filter capacitor. 00 = 3us 01 = 6us 10 = 9us 11 = 12us
[5:0]	FRA_SPI_IN[11:6]	

4.4.8.76 Dynamic Payload Length Enable Register(DYNPD)

Register	Offset	R/W	Description	Reset Value
DYNPD	RF_BA+0x12C	R/W	Dynamic Payload Length Enable Register	0×00

Bits	Descriptions	
[7:6]	Reserved	Reserved
[5]	DPL_P5	Enable dynamic payload length data pipe 5. (Requires EN_DPL and ENAA_P5)
[4]	DPL_P4	Enable dynamic payload length data pipe 4. (Requires EN_DPL and ENAA_P4)
[3]	DPL_P3	Enable dynamic payload length data pipe 3. (Requires EN_DPL and ENAA_P3)
[2]	DPL_P2	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
[1]	DPL_P1	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
[0]	DPL_P0	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P0)

4.4.8.77 Feature Register(FEATURE)

Register	Offset	R/W	Description	Reset Value
FEATURE	RF_BA+0x130	R/W	Feature Register	0×00

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Bits	Descriptions	
[7]	LVR_OUT	LVR_OUT state(Read-only) 0 = Low voltage reset
[6]	MUX_PA_IRQ	The IRQ pin output: 0 = IRQ signal 1 = EN_PA signal
[5]	CE_SEL	CE control: 0 = CE is controlled by the pin 1 = CE is controlled by SPI command
[4:3]	DATA_LEN_SEL	FIFO length: 11 = 64byte 00 = 32byte
[2]	EN_DPL	Enable Dynamic Payload Length
[1]	EN_ACK_PAY	Enable Payload with ACK
[0]	EN_NOACK	Enable theW_TX_PAYLOAD_NOACK command

4.4.8.78 RF Parameter Register0(RF_CAL_0)

Register	Offset	R/W	Description	Reset Value
RF_CAL_0	RF_BA+0x134	R/W	RF Parameter Register 0	0×80

Bits	Descriptions	
[7]	S_RES_1P2G[0]	1.2G divided by 2 resistance: 00 = 2.2K 01 = 1.76K 10 = 1.46K 11 = 1.25K
[6:4]	CP_SHIFT_IP_SEL	PLL_CP_CHIFT charge current control 000 = 0uA 001 =1.25uA … 111 = 1.75uA
[3:1]	CP_SHIFT_IN_SEL	PLL_CP_SHIFT discharge current control 000 = 0uA 001 =1.25uA … 111 = 1.75uA
[0]	EN_CP_SHIFT	PLL_CP_SHIFT Module Enable Bit 1 = Enabled 0 = Disabled

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4.4.8.79 RF Parameter Register1(RF_CAL_1)

Register	Offset	R/W	Description	Reset Value
RF_CAL_1	RF_BA+0x138	R/W	RF Parameter Register 1	0×02

Bits	Descriptions	
[7]	TST_DAC	
[6]	TST_LVR	
[5]	TST_RSSI	
[4]	TST_VBG	
[3]	Reserved	Reserved
[2:1]	S_RES_2P4G	2.4G divided by 2 resistance: 00 = 1.5K 01 = 1.2K 10 = 1.0K 11 =0.85K
[0]	S_RES_1P2G[1]	1.2G divided by 2 resistance: 00 = 2.2K 01 = 1.76K 10 = 1.46K 11 = 1.25K

4.4.8.80 RF Parameter Register 2(RF_CAL_2)

Register	Offset	R/W	Description	Reset Value
RF_CAL_2	RF_BA+0x13C	R/W	RF Parameter Register 2	0×A0

Bits	Descriptions	
[7:6]	PLL_IB_ISEL[1:0]	VCO Current Control
[5:4]	PLL_IPTAT_ISEL[1:0]	VCO Current Control
[3:2]	Reserved	Reserved
[1]	TST_ADC	
[0]	TST_BPF	

4.4.8.81 RF Parameter Register 3(RF_CAL_3)

Register	Offset	R/W	Description	Reset Value
RF_CAL_3	RF_BA+0x140	R/W	RF Parameter Register 3	0×88

Bits	Descriptions	
[7:4]	VCO_RX_CODE_IN	RX VCO Frequency Selection. These bits are only valid when EN_VCO_CAL=0. 1111 = High frequency band

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		0000 = Low frequency band
[3:0]	VCO_TX_CODE_IN	TX VCO Frequency Selection. These bits are only valid when EN_VCO_CAL=0. 1111 = High frequency band 0000 = Low frequency band

4.4.8.82 RF Parameter Register 4(RF_CAL_4)

Register	Offset	R/W	Description	Reset Value
RF_CAL_4	RF_BA+0x144	R/W	RF Parameter Register 4	0×71

Bits	Descriptions	
[7:5]	PLL_PRE_ISEL[2:0]	PLL 2 frequency division input DC control
[4]	PLL_PRE_TAILEN	Pre-2 Frequency Divider Enabling Control in PRECAL
[3]	Reserved	Reserved
[2]	MANUAL_VCO_ CODE	It's only valid when EN_VCO_CAL=0. 1 = Use the code defined by BB_CAL2<7:0> 0 = Use the auto-calibrated code.
[1]	DATAOUT_S	DATAOUT Register Output Selection signal 1 = Output analog_data[6:0] 0 = OutputVCO_CODE[3:0]
[0]	IRQ_inv_sel	IRQOutput Inverse Bit 1 = Output inversed 0 = Output not inversed

4.4.8.83 RF Parameter Register 5(RF_CAL_5)

Register	Offset	R/W	Description	Reset Value
RF_CAL_5	RF_BA+0x148	R/W	RF Parameter Register 5	0×BB

Bits	Descriptions	
[7]	PLL_DIV2_IB_CTL[0]	PLL 2 frequency division current control
[6:4]	PLL_DIV2_ISEL[2:0]	PLL 2 frequency division input DC control
[3]	PLL_DIV2_TAILEN	Post-2 Frequency Divider Enabling Control in PRECAL
[2:0]	PLL_PRE_IB_CTL[2:0]	PLL 2 frequency division current control

4.4.8.84 RF Parameter Register 6(RF_CAL_6)

Register	Offset	R/W	Description	Reset Value
RF_CAL_6	RF_BA+0x14C	R/W	RF Parameter Register 6	0×61

Bits	Descriptions	
[7:6]	PLL_VCO_FC_SEL[1:0]	VCO Manual calibration of process foot

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[5:2]	PLL_RX_VCO_ISEL	VCO RX Current Control.
[1:0]	PLL_DIV2_IB_CTL[2:1]	PLL 2 frequency division current control

4.4.8.85 RF Parameter Register 7(RF_CAL_7)

Register	Offset	R/W	Description	Reset Value
RF_CAL_7	RF_BA+0x150	R/W	RF Parameter Register 7	0×54

Bits	Descriptions	
[7:6]	PLL_LPF_R3[1:0]	PLL Filter R3 Selection 00 = 2K 01 = 4K 10 = 6K 11 = 8K
[5:4]	PLL_LPF_RZ[1:0]	PLL Filter Rz Selection 00 = 50K 01 = 70K 10 = 90K 11 = 110K
[3:2]	PLL_LPF_VSEL[1:0]	PLL Calibration Reference Voltage 00 = 638mV 01 = 738mV 10 = 838mV 11 = 938mV
[1:0]	Reserved	Reserved

4.4.8.86 RF Parameter Register 8(RF_CAL_8)

Register	Offset	R/W	Description	Reset Value
RF_CAL_8	RF_BA+0x154	R/W	RF Parameter Register 8	0×61

Bits	Descriptions	
[7:6]	PLL_PFD_DELAY[1:0]	PLL PFD Deadtime Control 00 =500ps 01 = 650ps 10 = 800ps 11 = 950ps
[5:2]	PLL_CP_ISEL[3:0]	PLL Filter CP Current Selection 0000 = 0uA … 1111 = 37.5uA
[1:0]	PLL_LPF_C3[1:0]	PLL Filter C3 Selection 00 = 16pF 01 = 20pF

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		10 = 24pF 11 = 28pF

4.4.8.87 RF Parameter Register 9(RF_CAL_9)

Register	Offset	R/W	Description	Reset Value
RF_CAL_9	RF_BA+0x158	R/W	RF Parameter Register 9	0×80

Bits	Descriptions	
[7:4]	PLL_TX_VCO_ISEL	VCO TX Current Control
[3:1]	Reserved	Reserved
[0]	TST_CTL	Vctl external voltage valid control bit (Only used for test) 0: Vctl invalid 1: Vctl valid

4.4.8.88 Digital Baseband Parameter Register 0 (BB_CAL_0)

Register	Offset	R/W	Description	Reset Value
BB_CAL_0	RF_BA+0x15C	R/W	Digital Baseband Parameter Register 0	0×0A

Bits	Descriptions	
[7:6]	RX_SETUP_TIME[1:0]	RX RF Channel PLL Stable Time. The calculation formula: RX_SETUP_TIME×16. The unit is us.
[5:0]	RX_ACK_TIME	The longest time of waiting ACK after PTX entering receive mode. The transmission will be regarded failed if exceeding this time. The calculation formula: 1Mbps + DSSS: RX_ACK_TIME×512 us. 1Mbps + GFSK: RX_ACK_TIME×32+31.5 us. 250Kbps + GFSK: RX_ACK_TIME×128+127.5 us.

4.4.8.89 Digital Baseband Parameter Register 1 (BB_CAL_1)

Register	Offset	R/W	Description	Reset Value
BB_CAL_1	RF_BA+0x160	R/W	Digital Baseband Parameter Register 1	0×6D

Bits	Descriptions	
[7:3]	TX_SETUP_TIME	The time interval between transmit PA enabled and PLL open-loop. The calculation formula: TX_SETUP_TIME×16. The unit is us.
[2:0]	RX_SETUP_TIME[4:2]	RX RF Channel PLL Stable Time. The calculation formula: RX_SETUP_TIME×16. The unit is us.

4.4.8.90 Digital Baseband Parameter Register 2 (BB_CAL_2)

Register	Offset	R/W	Description	Reset Value

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BB_CAL_2	RF_BA+0x164	R/W	Digital Baseband Parameter Register 2	0×24

Bits	Descriptions	
[7:5]	TRX_TIME	The time interval between PLL open-loop and transmitting data. The calculation formula: TRX_TIME×8+7.5. The unit is us.
[4:0]	PA1_SET_TIME	The time interval between EN_PA1ST pull-up and EN_PA2ST pull-up. The calculation formula: PA1_SET_TIME×16. The unit is us. Range: [0,496]us Default value: 64us.

4.4.8.91 Digital Baseband Parameter Register 3 (BB_CAL_3)

Register	Offset	R/W	Description	Reset Value
BB_CAL_3	RF_BA+0x168	R/W	Digital Baseband Parameter Register 3	0×24

Bits	Descriptions	
[7:0]	Reserved	Reserved

4.4.8.92 Digital Baseband Parameter Register 4 (BB_CAL_4)

Register	Offset	R/W	Description	Reset Value
BB_CAL_4	RF_BA+0x16C	R/W	Digital Baseband Parameter Register 4	0×4E

Bits	Descriptions	
[7:2]	Reserved	Reserved
[1]	INVERTER_CAL	Re_data Inverse Bit 1 = Inversed 0 = Not inversed
[0]	DAC_MODE	Dac_out[5:0] output inverse bit. Dac_out[5:0] is the input of DAC data. 1:dac_out[5:0]<= [0:5] 0:dac_out[5:0]<= [5:0]

4.4.8.93 Digital Baseband Parameter Register 5 (BB_CAL_5)

Register	Offset	R/W	Description	Reset Value
BB_CAL_5	RF_BA+0x170	R/W	Digital Baseband Parameter Register 5	0×20

Bits	Descriptions	
[7:0]	Reserved	Reserved

4.4.8.94 Digital Baseband Parameter Register 6 (BB_CAL_6)

Register	Offset	R/W	Description	Reset Value
BB_CAL_6	RF_BA+0x174	R/W	Digital Baseband Parameter Register 6	0×7F

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Bits	Descriptions	
[7:5]	PA2ST_CTM[2:0]	PA2ST Peak Point adjustment
[4:3]	PA1ST_ISEL[1:0]	PA1ST Bias Current Control
[2:0]	TX_DIV2_BIAS_CLK[2:0]	VCO%2 Circuit Control

4.4.8.95 Digital Baseband Parameter Register 7 (BB_CAL_7)

Register	Offset	R/W	Description	Reset Value
BB_CAL_7	RF_BA+0x178	R/W	Digital Baseband Parameter Register 7	0×9B

Bits	Descriptions	
[7:5]	TX_DAC_VREF_H[2:0]	DAC Reference Voltage Selection
[4]	EN_PA_DIV2_TAIL	VCO%2 Circuit Tail Current Enable Control
[3]	EN_TX_DIV2	VCO%2 Enable Circuit
[2:0]	PA1ST_CTM[2:0]	PA1ST Peak Point adjustment

4.4.8.96 Digital Baseband Parameter Register 8 (BB_CAL_8)

Register	Offset	R/W	Description	Reset Value
BB_CAL_8	RF_BA+0x17C	R/W	Digital Baseband Parameter Register 8	0×E4

Bits	Descriptions	
[7:6]	PA_ICTR[1:0]	PA Bias Current Configuration. Select the ratio of constant source current source to PTAT current source
[5]	TX_DAC_LPF_BW	DAC Filter Baseband Control
[4:3]	TX_DAC_GC[1:0]	DAC Output Gain Control
[2:0]	TX_DAC_VREF_L[2:0]	DAC Reference Voltage Select

4.4.8.97 Digital Baseband Parameter Register 9 (BB_CAL_9)

Register	Offset	R/W	Description	Reset Value
BB_CAL_9	RF_BA+0x180	R/W	Digital Baseband Parameter Register 9	0×00

Bits	Descriptions	
[7:1]	Reserved	Reserved
[0]	PA_ICTR[2]	PA Bias Current Configuration. Select the ratio of constant source current source and PTAT current source

4.4.8.98 RF CE Register (RF_CE)

Register	Offset	R/W	Description	Reset Value
RF_CE	RF_BA+0x184	R/W	RF CE Register	0×00

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Bits	Descriptions	
[7:1]	Reserved	Reserved
[0]	CE	CE

4.4.8.99 RF Command Register (RF_CMD)

Register	Offset	R/W	Description	Reset Value
RF_CMD	RF_BA+0x188	R/W	RF Command Register	0×00

Bits	Descriptions	
[7:0]	RF_CMD	8'b0110_0001 : R_RX_PAYLOAD 8'b1010_0000 : W_TX_PAYLOAD 8'b1110_0001 : FLUSH_TX 8'b1110_0010 : FLUSH_RX 8'b1110_0011 : REUSE_TX_PL 8'b0111_0011 : ACTIVE 8'b1000_1100 : DEACTIVE 8'b1010_1PPP : W_ACK_PAYLOAD 8'b1011_0000 : W_TX_PAYLOAD_NOACK 8'b0101_1010 : RST_HOLD 8'b1010_0101 : RST_RELS 8'b1111_1111 : NOP

4.4.8.100 RF FIFO Register (RF_FIFO)

Register	Offset	R/W	Description	Reset Value
RF_FIFO	RF_BA+0x18C	R/W	RF FIFO Register	0×00

Bits	Descriptions	
[7:0]	RF_FIFO	TX MODE:TX data payload register 1 ~ 64 bytes RX MODE:RX data payload register 1 ~ 64 bytes

4.4.8.101 RF Payload Configuration Register (RF_PL_WIDTH)

Register	Offset	R/W	Description	Reset Value
RF_PL_WIDTH	RF_BA+0x190	R	RF Payload Configuration Register	0×00

Bits	Descriptions	
[7:0]	RF_FIFO	The width of the payload.

4.4.8.102 Chip Identification Register (CHIP_ID)

Register	Offset	R/W	Description	Reset Value
CHIP_ID	RF_BA+0x194~0x198	R	Chip Identification Register	0×5051

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Bits	Descriptions	
[15:0]	CHIP_ID	Chip ID. {0x8CD,0x8CC}

Note: Initial values of all registers (including read/write) after on-chip reset are shown in the table.

When accessing multi-byte registers/addresses/data, the order of reading/writing is low bytes followed by high bytes. The high bit in a single byte is before the low bit.

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4.5 Flash Memory Controller (FMC)

4.5.1 Overview

The PAN2025 series are equipped with 32 Kbytes on-chip embedded flash for application and Data Flash to store some application dependent data. A User Configuration block is provided for system initialization. A size configurable loader ROM (LDROM) shared with 29K APROM is used for In-System-Programming (ISP) function. This chip also supports In-Application-Programming (IAP) function, user can switch the code executing without resetting the chip after the embedded flash updated

4.5.2 Features

- Supports 29KB (default) application ROM (APROM).
- Supports 2KB (default) loader ROM (LDROM).
- Supports size configurable for APROM and LDROM, the total size of them is 31KB.
- Supports configurable Data Flash size to share with APROM.
- Supports 16 bytes page erase for all embedded flash.
- Supports 512 bytes page erase for all embedded flash.
- Supports CRC-32 checksum calculation function.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory.

4.5.3 Block Diagram

The flash memory controller (FMC) consists of AHB slave interface, flash control registers, flash initialization controller, flash operation control and embedded flash memory. Figure 4-15 shows the block diagram of flash memory controller.

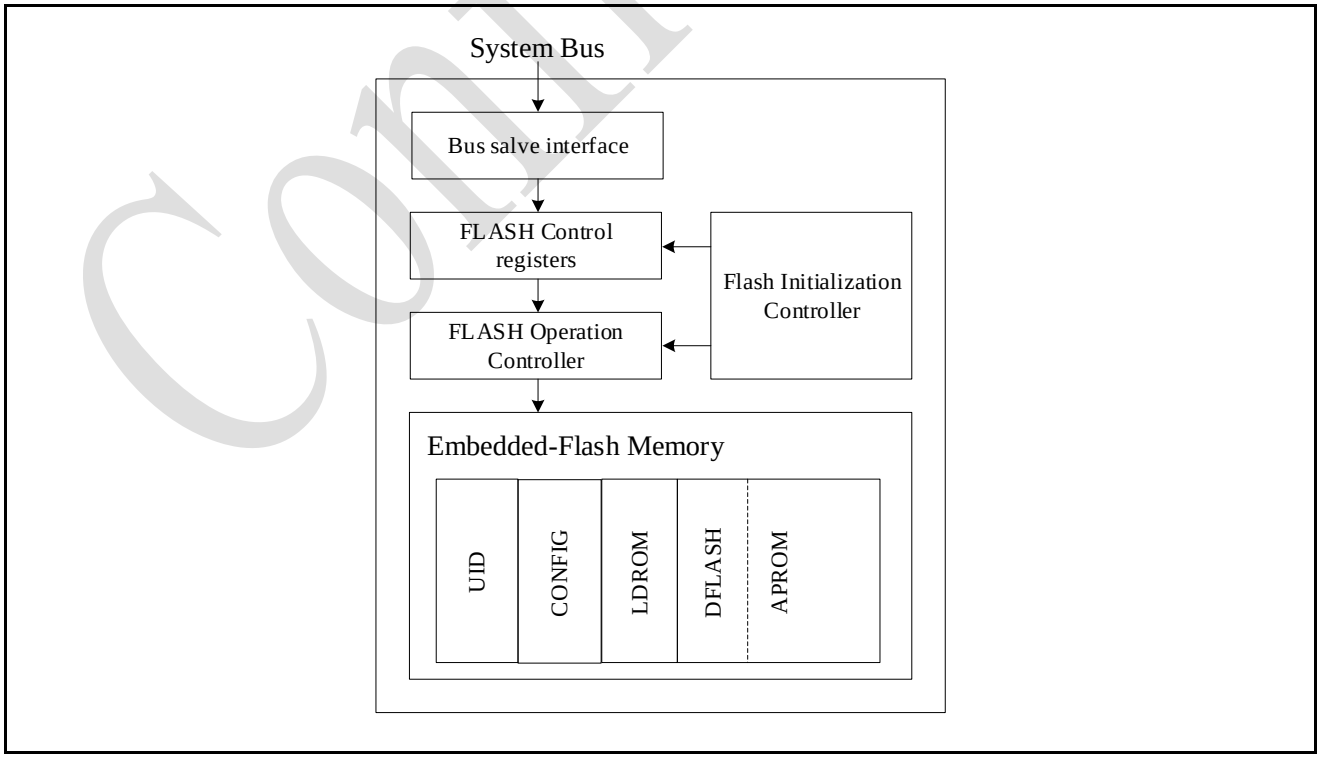

Figure 4-15 Flash Memory Control Block Diagram

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- Bus Slave Interface

There are single bus slave interfaces in flash memory controller for CPU to perform the instruction data fetch and ISP control registers.

- Flash Control Registers

All the ISP control and status registers are in the flash control registers. The detailed registers description is in the Register Description section

- Flash Initialization Controller

Once chip is powered on or active from reset, the flash initialization controller will start to access flash automatically, check the flash stability, and reload User Configuration content to the flash control registers for system initialization.

- Flash Operation Controller

The flash operations, such as checksum, flash erase, flash program, and flash read operation, have specific control timing for embedded flash memory. The flash operation controller generates those control timing by requests from the flash control registers and the flash initialization controller.

- Embedded Flash Memory

The embedded flash memory is the main memory for user application code and parameters. It consists of the user configuration block, 2 KB LDROM, 29 KB APROM with Data Flash. The page erase flash size is 512B, and program bit width is 16 bits.The size of APROM and LDROM can be configured by APAEND_DIS (CONFIG3[16]) and APAEND (CONFIG3 [14:0]), and the total size of APROM and LDROM is 31KB.

4.5.4 Functional Description

The FMC functions include the memory organization, boot selection, IAP, ISP, the embedded flash programming, and checksum calculation.

4.5.4.1 Memory Organization

The FMC memory consists of the embedded flash memory. The embedded flash memory is programmable, and includes APROM, LDROM, Data Flash and the User Configuration block. The address map includes flash memory map and four system address maps: LDROM with IAP, LDROM without IAP, APROM with IAP, and APROM without IAP functions.

4.5.4.2 LDROM, APROM and Data Flash

LDROM is designed for a loader to implement In-System-Programming (ISP) function by user. The size is configured by user: the flash address starts from 0x0010_0000 and lasts to 0x0010_07FF (default). APROM is the main memory for user applications. The flash address starts from 0x0000_0000 to 0x0000_73FF (default). Data Flash is used to store application parameters (not instruction). Data Flash is shared with APROM and the size is configurable. The base address of Data Flash is determined by DFBA (CONFIG1[19:0]) and end address is APROM end address. All the embedded flash memory is 512 bytes page erased.

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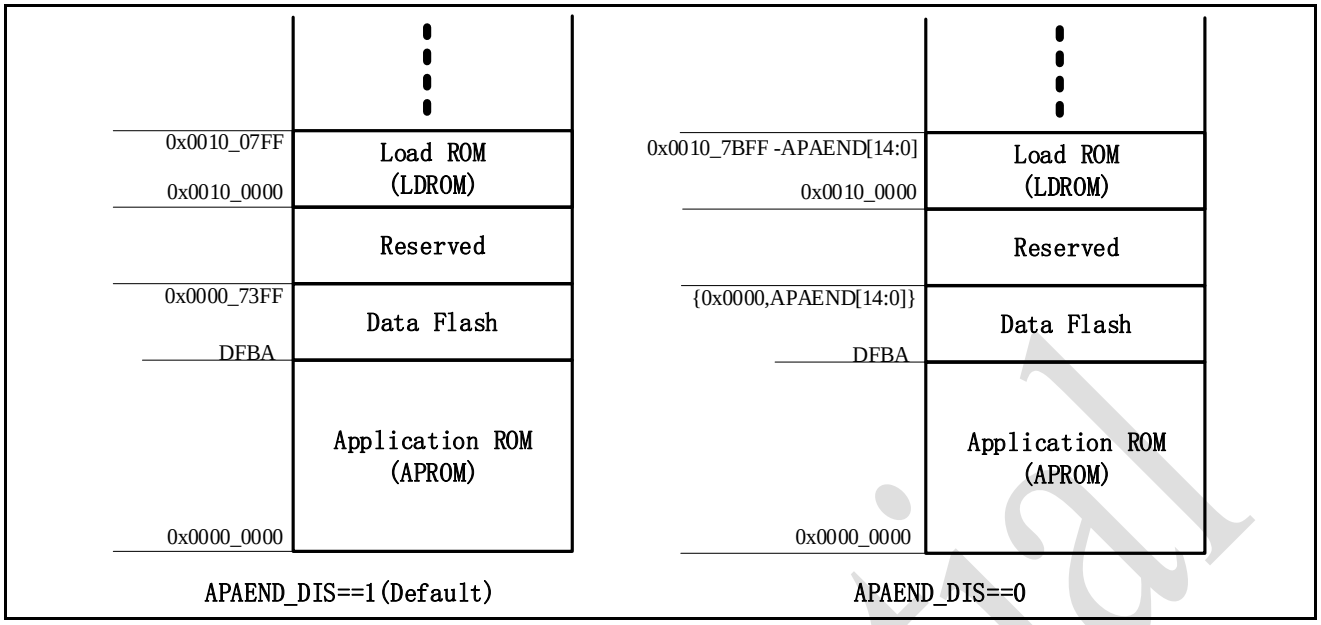

Figure 4-16 APROM, LDROM and Data Flash share with a 31K Flash

4.5.4.3 User Configuration Block

User Configuration block is internal programmable configuration area for boot options, such as flash security lock, boot select, brown-out voltage level, APROM Flash end address, and Data Flash base address. It works like a fuse for power on setting. It is loaded from flash memory to its corresponding control registers during chip power on. User can set these bits according to different application requests. User Configuration block can be updated by ISP function and located at 0x0030_0000 with four 32 bits words (CONFIG0, CONFIG1,CONFIG2 and CONFIG3). Any change on User Configuration block will affect the following system reboot.

4.5.4.3.1. CONFIG0 (Address = 0x0030_0000)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
CBS		Reserved				LOCK	Reserved

Bits	Descriptions	
[31:8]	Reserved	Reserved
[7:6]	CBS	Chip Booting Selection When CBS[0] = 0 with IAP mode, the LDROM base address is mapping to 0x100000 and APROM base address is mapping to 0x0. User can access both APROM and LDROM without boot switching. In other words, the code in LDROM and APROM can be called by each other. CBS value is valid.

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		00 = Boot from LDROM with IAP mode. 01 = Boot from LDROM without IAP mode. 10 = Boot from APROM with IAP mode. 11 = Boot from APROM without IAP mode. **Note**:BS (FMC_ISPCTL[1]) is only be used to control boot switching when CBS[0] = 1. VECMAP (FMC_ISPSTS[23:9]) is only be used to remap 0x0~0x1FF when CBS[0] = 0.
[5:2]	Reserved	Reserved
[1]	LOCK	Security Lock Control 0 = Flash memory content is locked. 1 = Flash memory content is locked except ALOCK (CONFIG2[7:0]) is 0x5A.
[0]	Reserved	Reserved

4.5.4.3.2. CONFIG1 (Address = 0x0030_0004)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved				DFBA			
15	14	13	12	11	10	9	8
DFBA							
7	6	5	4	3	2	1	0
DFBA							

Bits	Descriptions	
[31:20]	Reserved	Reserved
[19:0]	DFBA	Data Flash Base Address This register works only when DFEN (CONFIG0[0]) is set to 0. If DFEN (CONFIG0[0]) is set to 0, the Data Flash base address is defined by user. Since on-chip flash erase unit is 512 bytes, it is mandatory to keep bit 8-0 as 0.

4.5.4.3.3. CONFIG2 (Address = 0x0030_0008)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
ALOCK							

Bits	Descriptions	
[31:8]	Reserved	Reserved

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[7:0]	ALOCK	Advance Security Lock Control 0x5A = Flash memory content is unlocked if LOCK (CONFIG0[1]) is set to 1. Others = Flash memory content is locked. Note: ALOCK will be programmed as 0x5A after executing page erase or whole chip erase

4.5.4.3.4. CONFIG3 (Address = 0x0030_000C)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							APAEND_DIS
15	14	13	12	11	10	9	8
Reserved	APAEND						
7	6	5	4	3	2	1	0
APAEND							

Bits	Descriptions	
[31:17]	Reserved	Reserved
[16]	APAEND_DIS	APROM Address END Disable 1=APROM is 29K, and LDROM is 2K. APROM starts from 0x0000_0000 to 0x0000_73FF. LDROM starts from 0x0010_0000 to 0x0100_07FF. 0=APROM end address is configured by APAEND[14:0], APROM starts from 0x0000_0000 to {0x0000, APAEND[14:0]}. LDROM starts from 0x0010_0000 to {0x0100, 7BFF-APAEND[14:0]}.The total size of APROM and LDROM is 31KB.
[15]	Reserved	Reserved
[14:0]	APAEND	APROM Address END; APAEND_DIS=1: APROM is 29K, and LDROM is 2K. APROM starts from 0x0000_0000 to {0x0000_73FF }.LDROM starts from 0x0010_0000 to {0x0100_07FF}. APAEND_DIS=0: APROM end address is configured by APAEND[14:0], APROM starts from 0x0000_0000 to {0x0000, APAEND[14:0]}. LDROM starts from 0x0010_0000 to {0x0100, 7BFF-APAEND[14:0]}. The total size of APROM and LDROM is 31KB. If Data Flash used, DFBA[15:0]should be litter than APAEND[14:0], Since on-chip flash erase unit is 512 bytes, APAEND is mandatory to keep bit 8-0 as 1.

4.5.4.4 Flash Memory Map

In the PAN2025 series, the flash memory map is different from system memory map. The system memory map is used for CPU to fetch code or data from FMC memory. The flash memory map is used for ISP function to read, program or erase FMC memory. Figure 4-17 shows the flash memory map.

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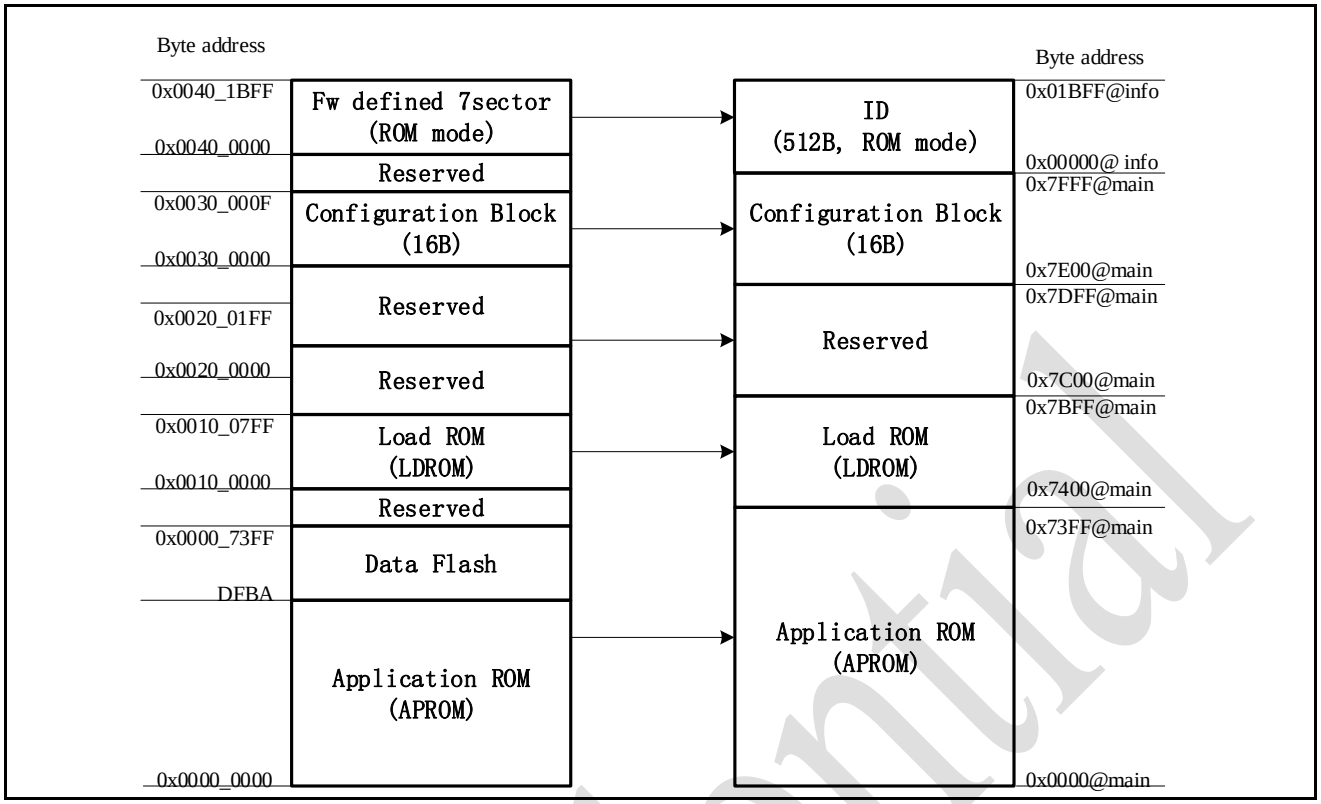

Figure 4-17 Flash Memory Map

4.5.4.5 System Memory Map with IAP Mode

The system memory map is used by CPU to fetch code or data from FMC memory. LDROM(0x0010_0000~0x0010_07FF) address map is the same as in the flash memory map. The Data Flash is shared with APROM and the Data Flash base address is defined by CONFIG1. The content of CONFIG1 is loaded into DFBA (Data Flash Base Address Register) at the flash initialization. The DFBA~APAEND is the Data Flash region for CPU data access, and 0x0000_0200~(DFBA-1) is APROM region for CPU instruction access.

The address from 0x0000_0000 to 0x0000_01FF is called system memory vector. APROM and LDROM can map to the system memory vector for CPU starting up. There are two kinds of system memory map with IAP mode when chip booting: (1) LDROM with IAP, and (2) APROM with IAP.

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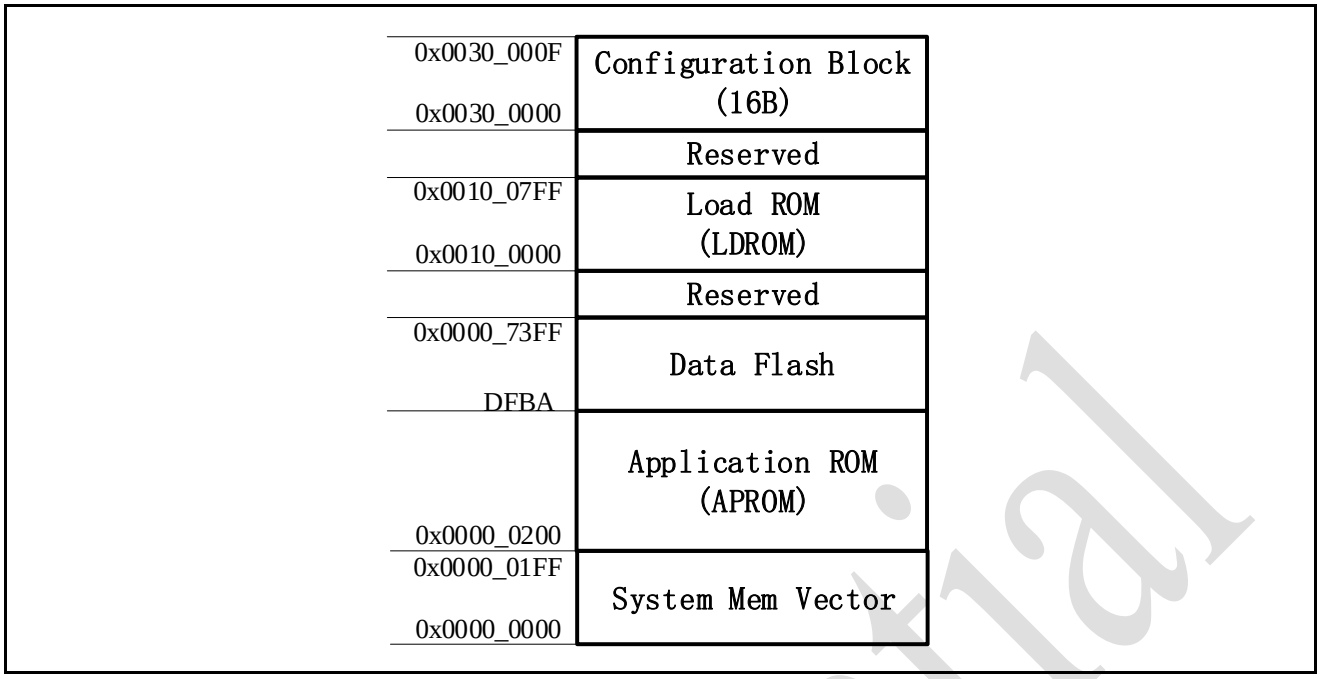

Figure 4-18 System Memory Map with IAP Mode

In LDROM with IAP mode, the default value of {VECMAP[11:0], 9'h000} is 0x100000 and the first page of LDROM (0x0010_0000 ~ 0x0010_01FF) is mapped to the system memory vector for CPU instruction or data access.

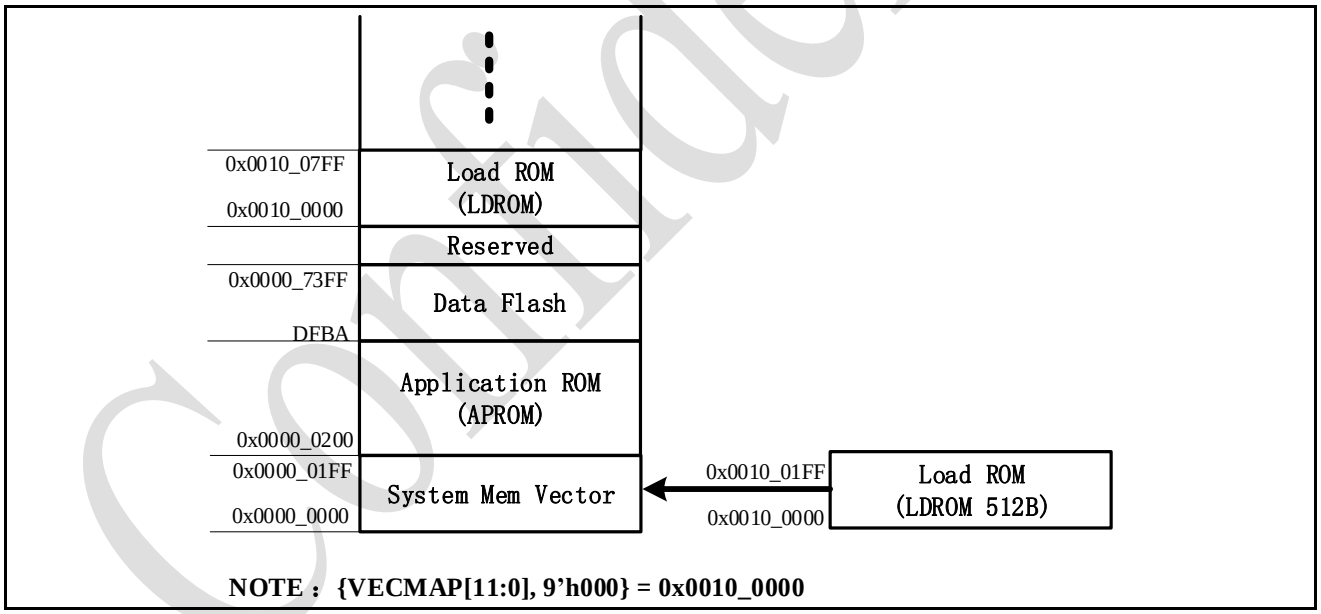

Figure 4-19 LDROM with IAP Mode

In APROM with IAP mode, the default value of {VECMAP[11:0], 9'h000} is 0x000000 and the first page of APROM (0x0000_0000~0x0000_01FF) is mapped to the system memory vector for CPU instruction or data access.

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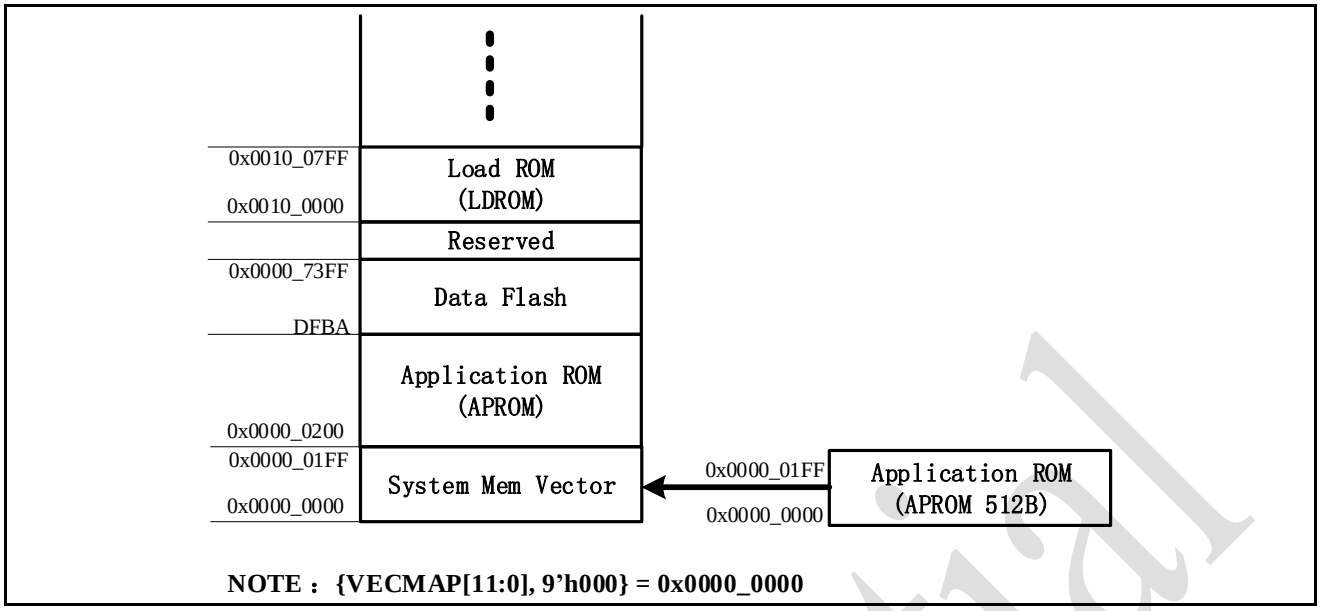

Figure 4-20 APROM with IAP Mode

In system memory map with IAP mode, APROM and LDROM can remap to the system memory vector when CPU running. User can write the target remap address to FMC_ISPADDR register and then trigger ISP procedure with the "Vector Page Remap" command (0x2E). In VECMAP (FMC_ISPSTS[23:9]), shows the finial system memory vector mapping address.

4.5.4.6 System Memory Map without IAP mode

The system memory vector mapping is not supported. There are two kinds of system memory map without IAP mode when chip booting: (1) LDROM without IAP, (2) APROM without IAP. In LDROM without IAP mode, LDROM base is mapped to 0x0000_0000. CPU program cannot run to access APROM. In APROM without IAP mode, APROM base is mapped to 0x0000_0000. CPU program cannot run to access LDROM. The Data Flash is shared with APROM and the Data Flash base address is defined by CONFIG1. The content of CONFIG1 is loaded into DFBA (Data Flash Base Address Register) at the flash initialization. The DFBA~0x0000_73FF is the Data Flash region for CPU data access, and 0x0000_0000~(DFBA-1) is APROM region for CPU instruction access.

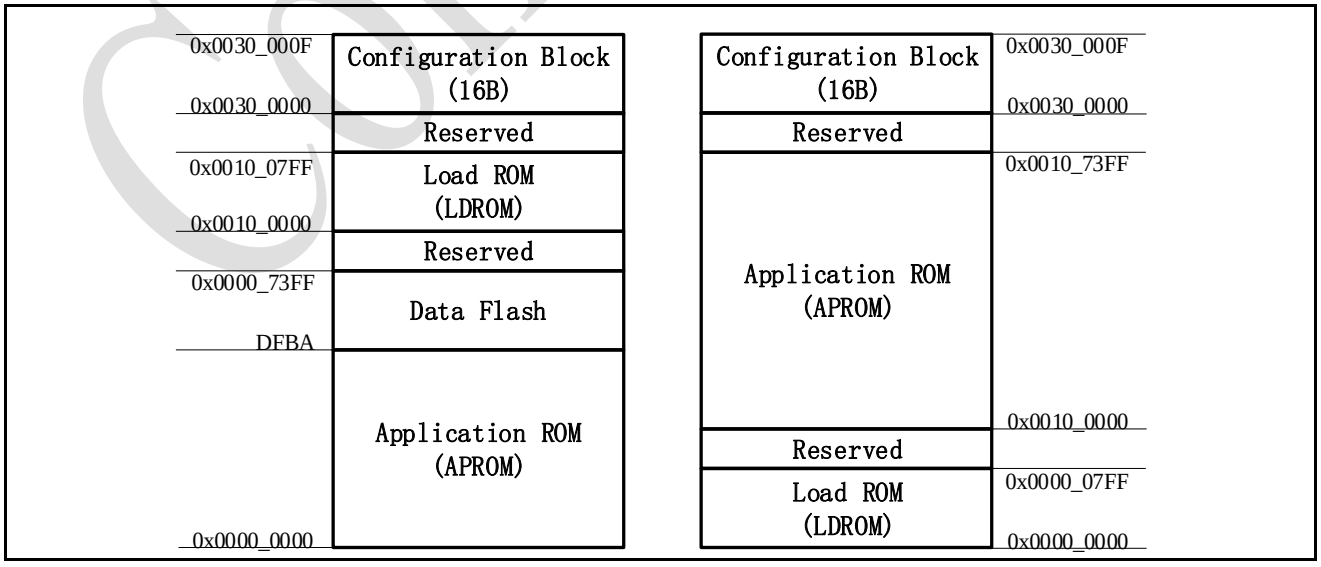

Figure 4-21 System Memory Map without IAP Mode

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4.5.4.7 Boot Selection

The PAN2025 provides four booting sources for user select. They are LDROM with IAP, LDROM without IAP, APROM with IAP, and APROM without IAP. The booting source and system memory map are set by CBS (CONFIG0[7:6]).

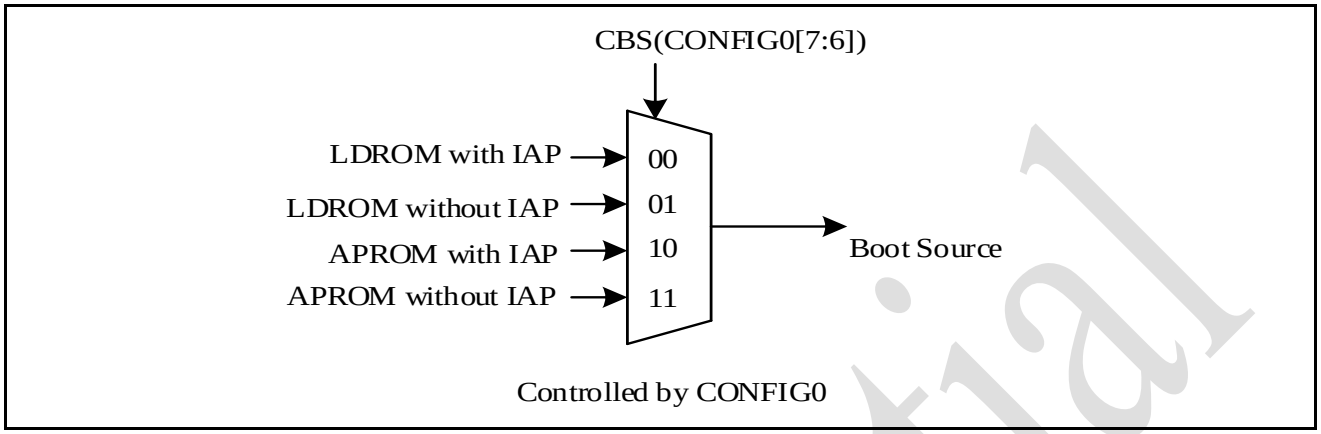

Figure 4-22 Boot Source Selection

Table 4-6 Vector Mapping Support Table

CBS[1:0]	Boot Selection/System Memory Map	Vector Mapping Support
00	LDROM with IAP	Yes
01	LDROM without IAP	No
10	APROM with IAP	Yes
11	APROM without IAP	No

4.5.4.8 In-Application-Programming (IAP)

The PAN2025 series provide In-Application-Programming (IAP) function for user to switch the code execution between APROM and LDROM. User can enable the IAP function by booting chip and setting the chip boot selection bits in CBS (CONFIG0[7:6]) as 10 or 00.

Once chip boots with IAP function is enabled, any executable code (align to 512 bytes) can be mapped to the system memory vector(0x0000_0000~0x0000_01FF) any time. Users can change the remap address to FMC_ISPADDR and then trigger ISP procedure with the “Vector Page Remap” command.

4.5.4.9 In-System-Programming (ISP)

The PAN2025 series support In-System-Programming (ISP) function allowing the embedded flash memory to be reprogrammed under software control. ISP can be performed without removing the microcontroller from the system through the firmware and on-chip connectivity interface, such as UART, I2C, and SPI.

The PAN2025 ISP provides the following functions for embedded flash memory.

- Supports flash page erase function
- Supports flash data program function

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- Supports flash data read function
- Supports company ID read function
- Supports device ID read function
- Supports unique ID read function
- Supports CRC32 read function
- Supports memory checksum calculation function
- Supports system memory vector remap function

4.5.4.9.1. ISP Commands

Table 4-7 ISP Command List

ISP Command	FMC_ISPCMD	FMC_ISPADDR	FMC_ISPDAT
FLASH Page Erase	0x22	Valid address of flash memory origination. It must be 512 bytes page alignment.	N/A
FLASH 32-bit Program	0x21	Valid address of flash memory origination	FMC_ISPDAT: Programming Data
FLASH Read	0x00	Valid address of flash memory origination	FMC_ISPDAT: Return Data
Read Company ID	0x0B	0x0000_0000(user mode) 0x0040_0040(ROM mode)	FMC_ISPDAT: 0xFFFF_FFFF
Read Device ID	0x0C	0x0000_0004(user mode) 0x0040_0084(ROM mode)	FMC_ISPDAT: 0xFFFF_FFFF
Read CRC32 Checksum	0x0D	Keep address of "Run Checksum Calculation"	FMC_ISPDAT: Return Checksum
Run CRC32 Checksum Calculation	0x2D	Valid start address of memory origination It must be 512 bytes page alignment	FMC_ISPDAT: Size It must be 512 bytes alignment
Read Unique ID	0x04	0x0000_0000 (user mode) 0x0040_0020(ROM mode) **Note**: only care FMC_ISPADDR[4:2]	FMC_ISPDAT: Unique ID Word 0
		0x0000_0004 (user mode) 0x0040_0024(ROM mode) **Note**: only care FMC_ISPADDR[4:2]	FMC_ISPDAT: Unique ID Word 1
		0x0000_0008 (user mode) 0x0040_0028(ROM mode) **Note**: only care FMC_ISPADDR[4:2]	FMC_ISPDAT: Unique ID Word2
		0x0000_000C (user mode) 0x0040_002C(ROM mode) **Note**: only care FMC_ISPADDR[4:2]	FMC_ISPDAT: Unique ID Word3
Read Unique Company ID	0x04	0x0000_0010 (user mode) 0x0040_0030(ROM mode) **Note**: only care FMC_ISPADDR[4:2]	FMC_ISPDAT: Unique Company ID Word 0
		0x0000_0014 (user mode) 0x0040_0034(ROM mode) **Note**: only care FMC_ISPADDR[4:2]	FMC_ISPDAT: Unique Company ID Word 1

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		0x0000_0018 (user mode) 0x0040_0038(ROM mode) **Note**: only care FMC_ISPADDR[4:2]	FMC_ISPDAT: Unique Company ID Word 2
		0x0000_001C (user mode) 0x0040_003C(ROM mode) **Note**: only care FMC_ISPADDR[4:2]	FMC_ISPDAT: Unique Company ID Word 3
Vector Remap	0x2E	Valid address in APROM or LDROM. It must be 512 bytes alignment	N/A
Wafer ID		0x0040_00C0	2 Words
ROM Version		0x0040_01C0	4 Words

4.5.4.9.2. ISP Procedure

The FMC provides embedded flash memory read, erase and program operation. Several control bits of FMC control register are write-protected, thus it is necessary to be unlocked before setting.

After unlocking the protected register bits, user needs to set the FMC_ISPCTL control register to decide to update LDROM, APROM or user configuration block, and then set ISPEN (FMC_ISPCTL[0]) to enable ISP function.

Once the FMC_ISPCTL register is set properly, user can set FMC_ISPCMD (refer above ISP command list) for specify operation. Set FMC_ISPADDR for target flash memory based on flash memory origination. FMC_ISPDAT can be used to set the data to program or used to return the read data according to FMC_ISPCMD.

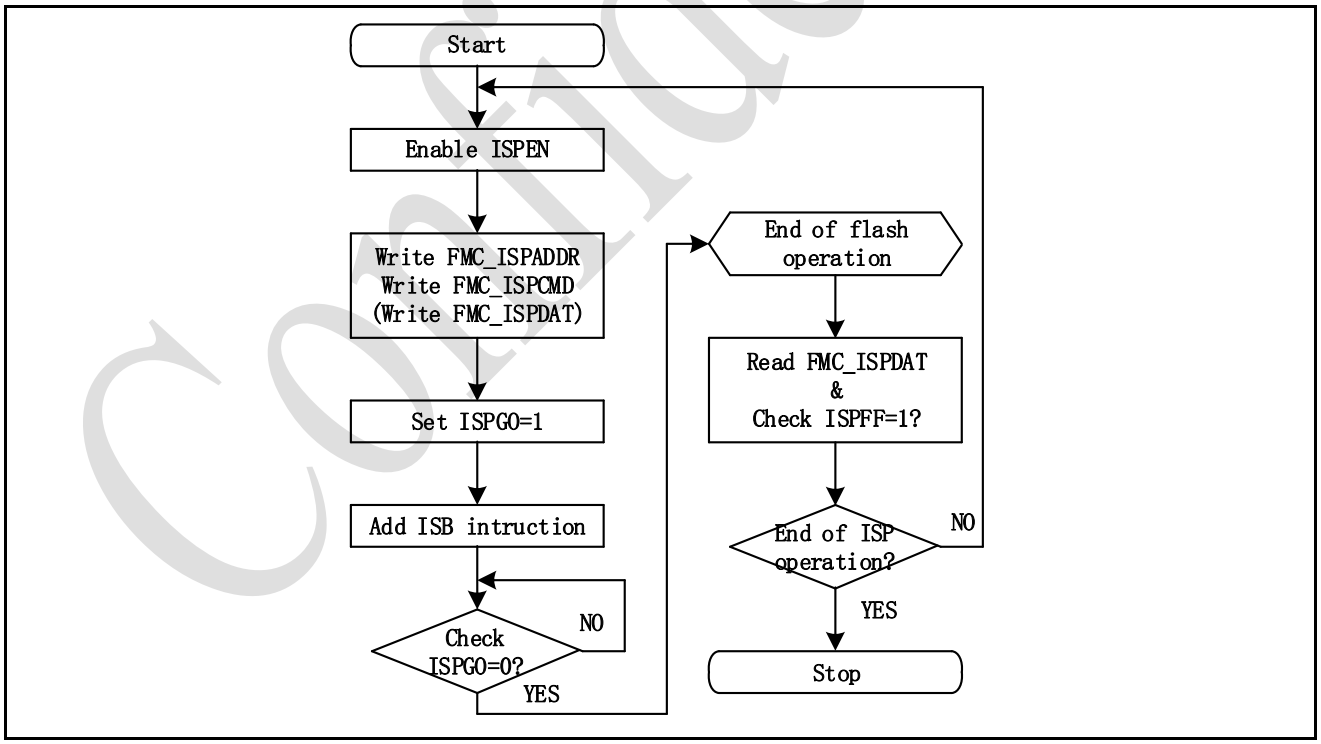

Figure 4-23 ISP Procedure Example

Finally, set ISPGO (FMC_ISPTRG[0]) register to perform the relative ISP function. The ISPGO (FMC_ISPTRG[0]) bit is self-cleared when ISP function has been done. To make sure ISP function has been finished before CPU goes ahead, ISB (Instruction Synchronization Barrier) instruction is

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used right after ISPGO (FMC_ISPTRG[0]) setting.

Several error conditions will be checked after ISP is completed. If an error condition occurs, ISP operation is not started and the ISP fail flag will be set instead. ISPFF (FMC_ISPSTS[6]) flag can only be cleared by software. The next ISP procedure can be started even ISPFF (FMC_ISPSTS[6]) bit is kept as 1. Therefore, it is recommended to check the ISPFF (FMC_ISPSTS[6]) bit and clear it after each ISP operation if it is set to 1.

When the ISPGO (FMC_ISPTRG[0]) bit is set, CPU will wait for ISP operation to finish during this period; the peripheral still keeps working as usual. If any interrupt request occurs, CPU will not service it till ISP operation has finished. When ISP operation has finished, the ISPGO bit will be cleared by hardware automatically. User can check whether ISP operation is finished or not by the ISPGO (FMC_ISPTRG[0]) bit. User should add ISB (Instruction Synchronization Barrier) instruction next to the instruction in which ISPGO (FMC_ISPTRG[0]) bit is set 1 to ensure correct execution of the instructions following ISP operation.

4.5.4.10 CRC32 Checksum Calculation

The PAN2025 series support the Cyclic Redundancy Check (CRC-32) checksum calculation function to help user quickly check the memory content includes APROM and LDROM. The CRC-32 polynomial is below:

CRC32: $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$

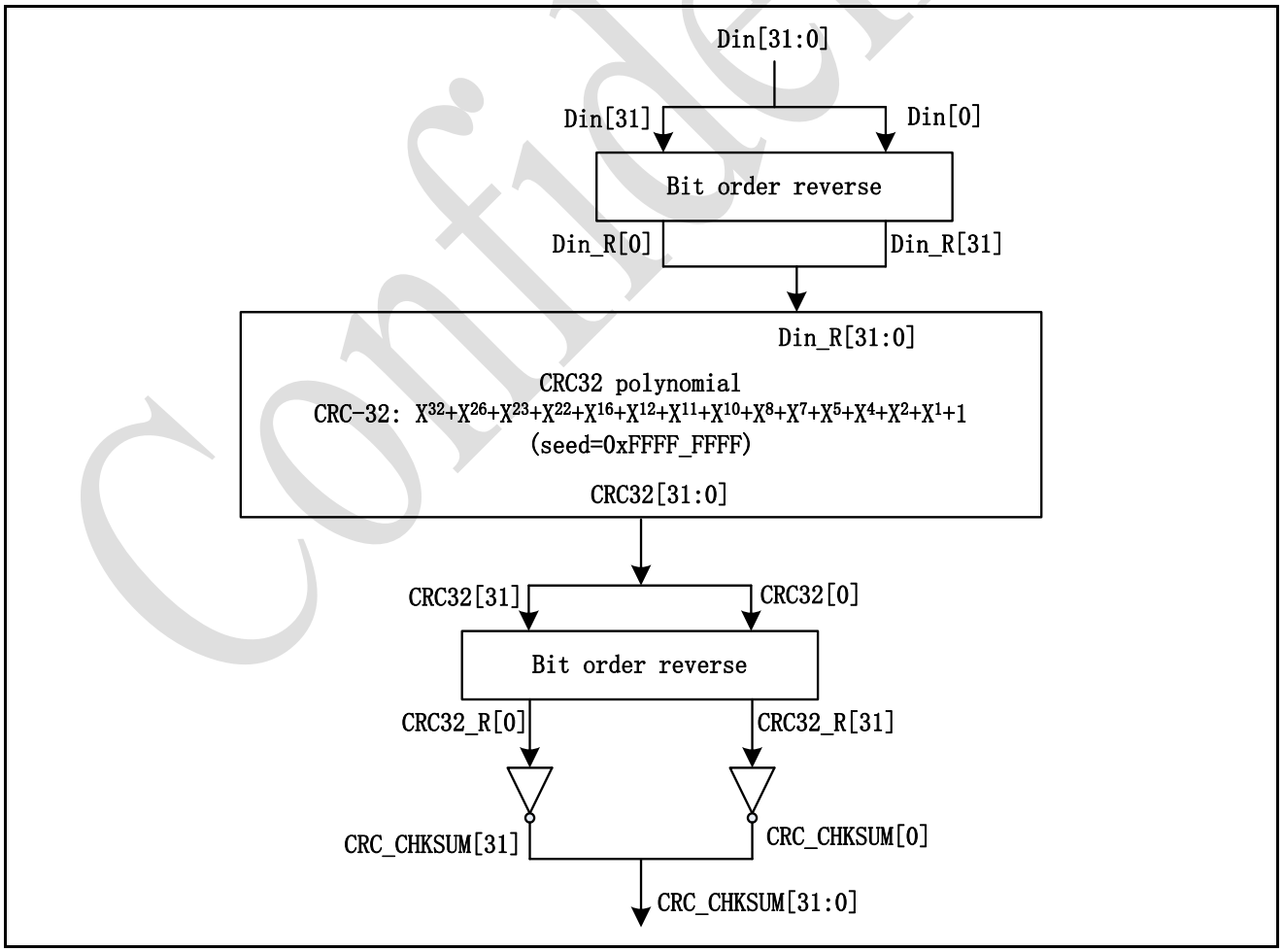

Figure 4-24 CRC-32 Checksum Calculation

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The following three steps show the CRC-32 checksum calculation completely.

1. Perform ISP “Run Memory Checksum” operation: user has to set the memory starting address (FMC_ISPADDR) and size (FMC_ISPDAT) to calculate. Both address and size have to be 4 bytes alignment, the size should be must be multiples of 4 bytes and the starting address is absolute address, in Figure 4-17 Flash Memory Map, it refers to byte address from flash perspect.

2. Perform ISP “Read Memory Checksum” operation: the FMC_ISPADDR should be kept as the same as step 1.

3. Read FMC_ISPDAT to get checksum: The checksum is read from FMC_ISPDAT. If the checksum is 0x0000_0000, it must be one of two conditions (1) Checksum calculation is in-progress, (2) Address and size is over device limitation.

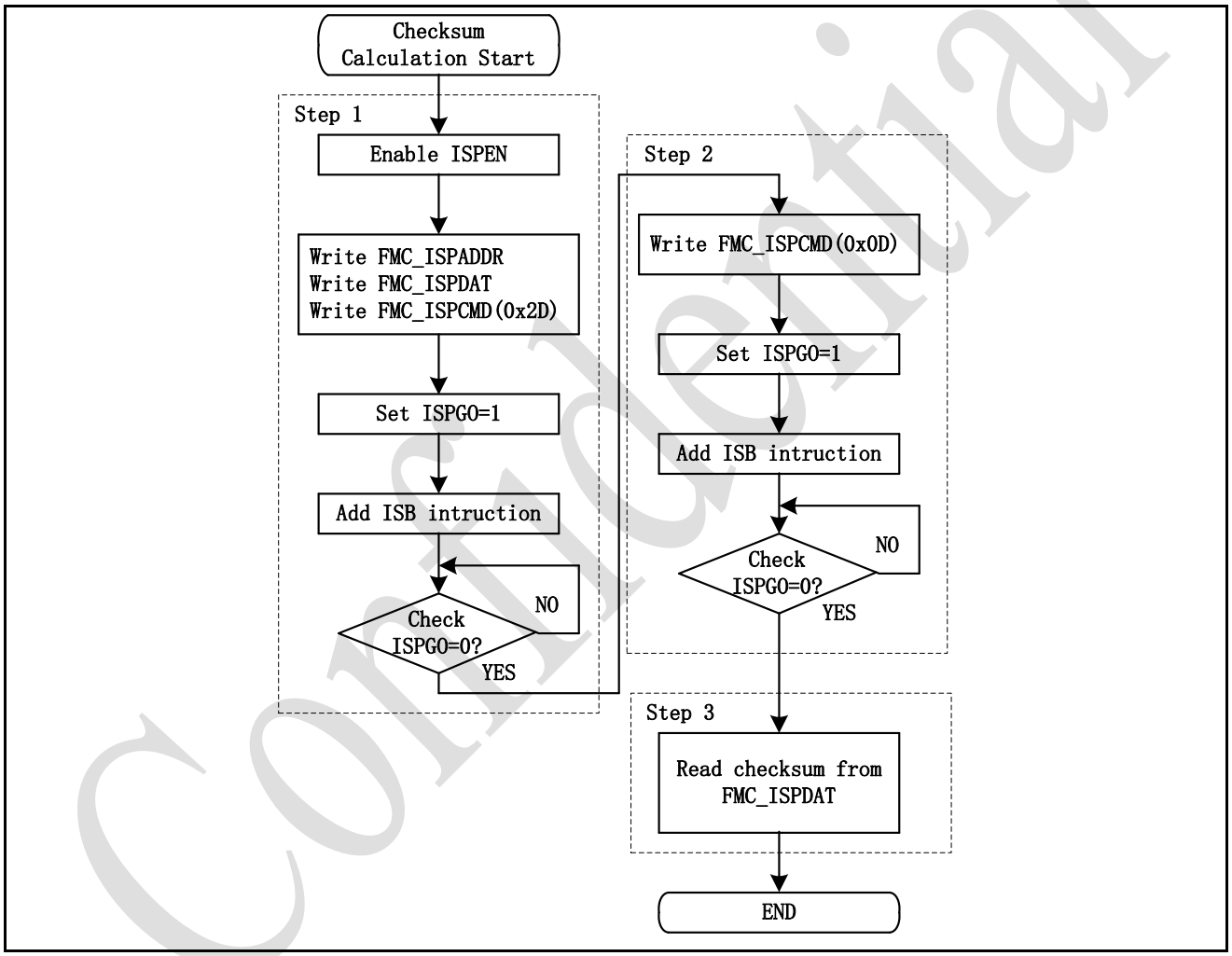

Figure 4-25 CRC-32 Checksum Calculation Flow

4.5.5 FMC Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
FMC Base Address: **FMC_BA = 0x4005_0000**				

FMC_ISPCTL	FMC_BA+0x00	R/W	ISP Control Register	0x0000_000X
FMC_ISPADDR	FMC_BA+0x04	R/W	ISP Address Register	0x0000_0000
FMC_ISPDAT	FMC_BA+0x08	R/W	ISP Data Register	0x0000_0000
FMC_ISPCMD	FMC_BA+0x18	R/W	ISP Command Register	0x0000_0000
FMC_ISPTRG	FMC_BA+0x1C	R/W	ISP Trigger Control Register	0x0000_0000
FMC_DFBA	FMC_BA+0x20	R	Data Flash Base Address	0xXXXX_XXXX
FMC_FATCTL	FMC_BA+0x24	R/W	Flash Access Time Control Register	0x0000_0000
FMC_ISPSTS	FMC_BA+0x40	R/W	ISP Status Register	0xX0X0_000X
FMC_ISPCFG0	FMC_BA+0x50	R	ISP Configure0 Register	0xFFFF_FFFF
FMC_ISPCFG1	FMC_BA+0x54	R	ISP Configure1 Register	0xFFFF_FFFF
FMC_ISPCFG2	FMC_BA+0x58	R	ISP Configure2 Register	0xFFFF_FFFF
FMC_ISPCFG3	FMC_BA+0x5C	R	ISP Configure3 Register	0xFFFF_FFFF

4.5.6 FMC Register Description

4.5.6.1 ISP Control Register (FMC_ISPCTL)

Register	Offset	R/W	Description	Reset Value
FMC_ISPCTL	FMC_BA+0x00	R/W	ISP Control Register	0x0000_000X

Bits	Descriptions	
[31:6]	Reserved	Reserved.
[5]	LDUEN	LDROM Update Enable (Write Protect) 0 = LDROM cannot be updated. 1 = LDROM can be updated.
[4]	CFGUEN	CONFIG Update Enable Bit (Write Protect) 0 = CONFIG cannot be updated. 1 = CONFIG can be updated.
[3]	APUEN	APROM Update Enable Bit (Write Protect) 0 = APROM cannot be updated when the chip runs in APROM. 1 = APROM can be updated when the chip runs in APROM.
[2]	Reserved	Reserved
[1]	BS	Boot Select (Read Only) This bit can also act as chip booting status flag, which can be used to check where chip is booted from. This bit is initiated with the inversed value of CBS[1] (CONFIG0[7]) after any reset is happened except CPU reset (CPURF is 1) or system reset (SYSRF) 0 = Booting from APROM. 1 = Booting from LDROM.
[0]	ISPEN	ISP Enable Bit (Write Protect) Set this bit to enable the ISP function. 0 = ISP function disabled. 1 = ISP function enabled.

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4.5.6.2 ISP Address (FMC_ISPADDR)

Register	Offset	R/W	Description	Reset Value
FMC_ISPADDR	FMC_BA+0x04	R/W	ISP Address Register	0x0000_0000

Bits	Descriptions	
[31:0]	ISPADDR	ISP Address The PAN2025 is equipped with embedded flash. ISPADDR[1:0] must be kept 00 for ISP 32-bit operation. and ISPADDR[8:0] must be kept all 0 for Vector Page Re-map Command For CRC32 Checksum Calculation command, this field is the flash starting address for checksum calculation, 512 bytes alignment is necessary for checksum calculation. The specific relationship between ISP command and FMC_ISPADDR can be related to Table 4-7.

4.5.6.3 ISP Data Register (FMC_ISPDAT)

Register	Offset	R/W	Description	Reset Value
FMC_ISPDAT	FMC_BA+0x08	R/W	ISP Data Register	0x0000_0000

Bits	Descriptions	
[31:0]	ISPDAT	ISP Data Write data to this register before ISP program operation. Read data from this register after ISP read operation. To run CRC32 Checksum Calculation command, ISPDAT is the memory size (byte) and 16 bytes alignment. For ISP Read Checksum command, ISPDAT is the checksum result. If ISPDAT = 0x0000_0000, it means that (1) the checksum calculation is in progress, or (2) the memory range for checksum calculation is incorrect. The specific relationship between ISP command and FMC_ISPDAT can be related to Table 4-7.

4.5.6.4 ISP Command Register (FMC_ISPCMD)

Register	Offset	R/W	Description	Reset Value
FMC_ISPCMD	FMC_BA+0x18	R/W	ISP Command Register	0x0000_0000

Bits	Descriptions	
[31:7]	Reserved	Reserved
[6:0]	CMD	ISP CMD ISP command table is shown below: 0x00 = FLASH Read. 0x04 = Read Unique ID. 0x0B = Read Company ID.

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		0x0C = Read Device ID. 0x0D = Read CRC32 Checksum. 0x21 = FLASH 32-bit Program. 0x22 = FLASH Page Erase. 0x23 = FLASH whole chip Erase (ROM mode). 0x2D = Run CRC32 Checksum Calculation. 0x2E = Vector Remap. The other commands are invalid.

4.5.6.5 ISP Trigger Control Register (FMC_ISPTRG)

Register	Offset	R/W	Description	Reset Value
FMC_ISPTRG	FMC_BA+0x1C	R/W	ISP Trigger Control Register	0x0000_0000

Bits	Descriptions	
[31:1]	Reserved	Reserved
[0]	ISPGO	ISP Start Trigger (Write Protect) Write 1 to start ISP operation and this bit will be cleared to 0 by hardware automatically when ISP operation has finished. 0 = ISP operation has finished. 1 = ISP is in progress.

4.5.6.6 Data Flash Base Address Register (FMC_DFBA)

Register	Offset	R/W	Description	Reset Value
FMC_DFBA	FMC_BA+0x20	R	Data Flash Base Address	0xXXXX_XXXX

Bits	Descriptions	
[31:20]	Reserved	Reserved
[19:0]	DFBA	Data Flash Base Address This register indicates Data Flash start address. It is a read only register. The Data Flash is shared with APROM. The content of this register is loaded from CONFIG1 This register is valid when DFEN (CONFIG0[0]) =0 .

4.5.6.7 Flash Access Time Control Register (FMC_FATCTL)

Register	Offset	R/W	Description	Reset Value
FMC_FATCTL	FMC_BA+0x24	R/W	Flash Access Time Control Register	0x0000_0000

Bits	Descriptions	
[31:4]	Reserved	Reserved
[3:0]	FATCTL	Reserved Frequency Optimization Mode (Write Protect) The series support adjustable flash access timing to optimize the flash access cycles in

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		different working frequency. $\frac{1}{F_{System\ clock}} \times (latency + 0.5) \geq 30ns$ The unit of system clock frequency is Mhz

4.5.6.8 ISP Status Register (FMC_ISPSTS)

Register	Offset	R/W	Description	Reset Value
FMC_ISPSTS	FMC_BA+0x40	R/W	ISP Status Register	0xX0X0_000X

Bits	Descriptions	
[31:21]	Reserved	Reserved
[20:9]	VECMAP	Vector Page Mapping Address (Read Only) All access to 0x0000_0000~0x0000_01FF is remapped to the flash memory address {VECMAP[11:0], 9'h000} ~ {VECMAP[11:0], 9'h1FF}
[8:3]	Reserved	Reserved
[2:1]	CBS	Boot Selection Of CONFIG (Read Only) This bit is initiated with the CBS (CONFIG0[7:6]) after any reset is happened except CPU reset (RSTS_CPU is 1) or system reset (RSTS_SYS). 00 = LDROM with IAP mode. 01 = LDROM without IAP mode. 10 = APROM with IAP mode. 11 = APROM without IAP mode.
[0]	ISPBUSY	ISP BUSY (Read Only) 0 = ISP operation is finished. 1 = ISP operation is busy.

4.5.6.9 ISP Configure0 Register (FMC_ISPCFG0)

Register	Offset	R/W	Description	Reset Value
FMC_ISPCFG0	FMC_BA+0x50	R	ISP configure Register	0xFFFF_FFFF

Bits	Descriptions	
[31:8]	Reserved	Reserved
[7:6]	CBS	Chip Booting Selection (Read Only) When CBS[0] = 0 with IAP mode, the LDROM base address is mapped to 0x100000 and APROM base address is mapped to 0x0. User could access both APROM and LDROM without boot switching. In other words, the code in LDROM and APROM can be called by each other. CBS value is valid. 00 = Boot from LDROM with IAP mode. 01 = Boot from LDROM without IAP mode. 10 = Boot from APROM with IAP mode.

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		11 = Boot from APROM without IAP mode. **Note**: BS (FMC_ISPCTL[1]) is only be used to control boot switching when CBS[0] = 1. VECMAP (FMC_ISPSTS[23:9]) is only be used to remap 0x0~0x1FF when CBS[0] = 0.
[5:2]	Reserved	Reserved
[1]	LOCK	Security Lock Control (Read Only) 0 = Flash memory content is locked. 1 = Flash memory content is locked except ALOCK (CONFIG2[7:0]) is 0x5A.
[0]	Reserved	Reserved

4.5.6.10 ISP Configure1 Register (FMC_ISPCFG1)

Register	Offset	R/W	Description	Reset Value
FMC_ISPCFG1	FMC_BA+0x54	R	ISP configure Register	0xFFFF_FFFF

Bits	Descriptions	
[31:20]	Reserved	Reserved
[19:0]	DFBA	Data Flash Base Address (Read Only) This register works only when DFEN (CONFIG0[0]) is set to 0. If DFEN (CONFIG0[0]) is set to 0, the Data Flash base address is defined by user. Since on-chip flash erase unit is 512 bytes, it is mandatory to keep bit 8-0 as 0.

4.5.6.11 ISP Configure2 Register (FMC_ISPCFG2)

Register	Offset	R/W	Description	Reset Value
FMC_ISPCFG2	FMC_BA+0x58	R	ISP Configure2 Register	0xFFFF_FFFF

Bits	Descriptions	
[31:8]	Reserved	Reserved
[7:0]	ALOCK	Advance Security Lock Control (Read Only) 0x5A = Flash memory content is unlocked if LOCK (CONFIG0[1]) is set to 1. Others = Flash memory content is locked. **Note**: ALOCK will be programmed as 0x5A after executing page erase or whole chip erase

4.5.6.12 ISP Configure3 Register (FMC_ISPCFG3)

Register	Offset	R/W	Description	Reset Value
FMC_ISPCFG3	FMC_BA+0x5C	R	ISP Configure3 Register	0xFFFF_FFFF

Bits	Descriptions	
[31:17]	Reserved	Reserved
[16]	APAEND_DIS	APROM Address END Disable (Read Only)

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		1=APROM is 29K, and LDROM is 2K. APROM is from 0x0000_0000 to {0x0000_73FF}. LDROM is from 0x0010_0000 to {0x0100_07FF}. 0=APROM end address is configured by APAEND[14:0], APROM is from 0x0000_0000 to {15'h0, APAEND[14:0]}.LDROM is from 0x0010_0000 to 0x0010_00000+(18'h7BFF-APAEND[14:0]}. The total size of APROM and LDROM is 31KB.
[15]	Reserved	Reserved
[14:0]	APAEND	APROM Address END (Read Only) APAEND_DIS=1: APROM is 29K, and LDROM is 2K. APROM is from 0x0000_0000 to {0x0000_73FF}.LDROM starts from 0x0010_0000 to {0x0010_07FF}. APAEND_DIS=0: APROM end address is configured by APAEND[14:0], APROM is from 0x0000_0000 to {15'h0, APAEND[14:0]}.LDROM is start from 0x0010_0000 to 0x0010_0000+(18'h7BFF-APAEND[14:0]}.The total size of APROM and LDROM is 31KB. **Note**: the separation of APROM and LDROM is page aligned, in other words, the size of APROM or LDROM is a integer times of 512 bytes. The page address of APROM is {9'd0 --- APAEND[14:6]}(we have 512 pages totally in main flash)

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4.6 General Purpose I/O (GPIO)

4.6.1 Overview

The PAN2025 has up to 24 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 24 pins are arranged in 6 ports named as P0, P1, P2, P3, P4 and P5. Each of the 24 pins is independent and has the corresponding register bits to control the pin mode function and data. Different package formats correspond to different GPIO numbers. There are 21 pins for QFN32 and 24 pins for QFN40.

The I/O type of each pin can be configured by software individually as Input, Push-pull output, Open-drain output, or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins stays in input mode and each port data register Px_DOUT[n] resets to 1. For Quasi-bidirectional mode, each I/O pin is equipped with a very weak individual pull-up resistor about 110k~ 300kΩ for VDD is from 2.2 V to 3.6 V.

4.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-pull output
  - Open-drain output
  - Input-only with high impendence
- Quasi-bidirectional TTL/Schmitt trigger input mode selected by SYS_Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function
- Supporting high driver and high sink I/O mode

4.6.3 Block Diagram

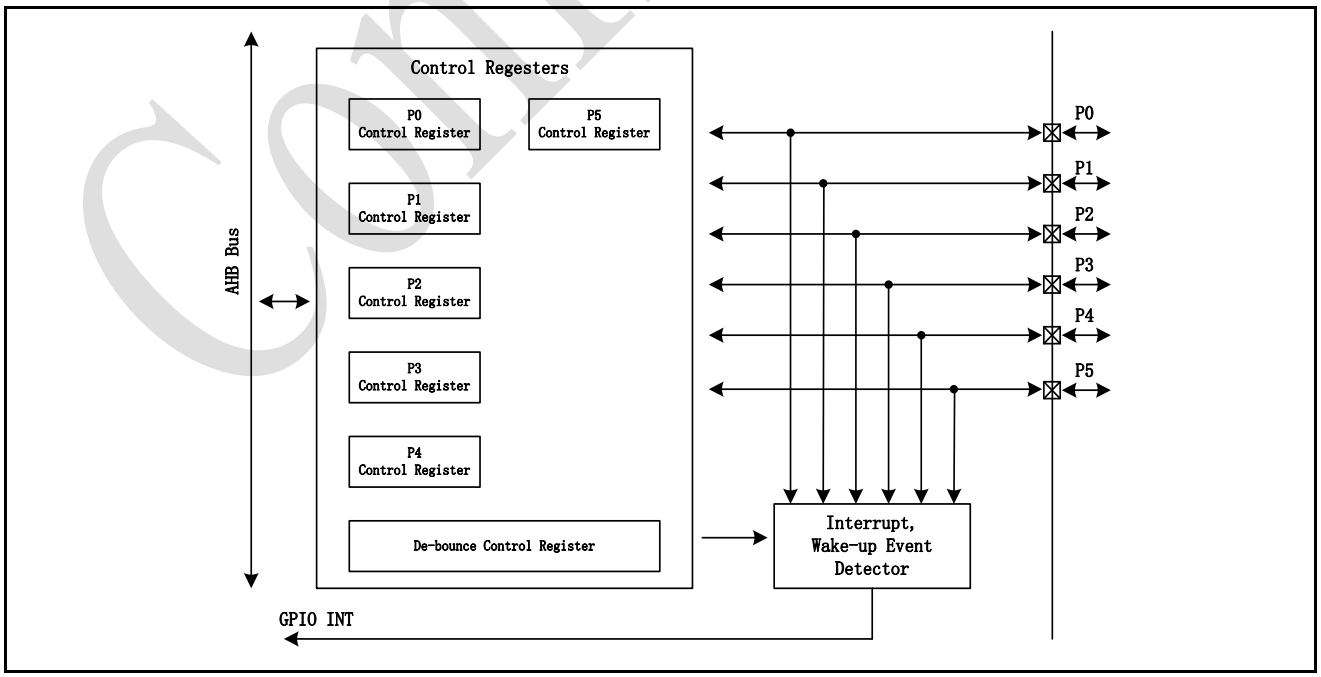

Figure 4-26 GPIO Controller Block Diagram

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4.6.4 Basic Configuration

The GPIO pin functions are configured in SYS_P0_MFP, SYS_P1_MFP, SYS_P2_MFP, SYS_P3_MFP, SYS_P4_MFP and SYS_P5_MFP registers.

4.6.5 Functional Description

4.6.5.1 Input Mode

Set MODEn (Px_MODE[2n+1:2n]) to 00 as the Px.n pin is in Input mode and the I/O pin is in tri-state (high impedance) without output drive capability. The PIN (Px_PIN[n]) value reflects the status of the corresponding port pins.

4.6.5.2 Push-pull Output Mode

Set MODEn (Px_MODE[2n+1:2n]) to 01 as the Px.n pin is in Push-pull Output mode and the I/O pin supports digital output function with source/sink current capability. The bit value in the corresponding DOUT (Px_DOUT[n]) is driven on the pin.

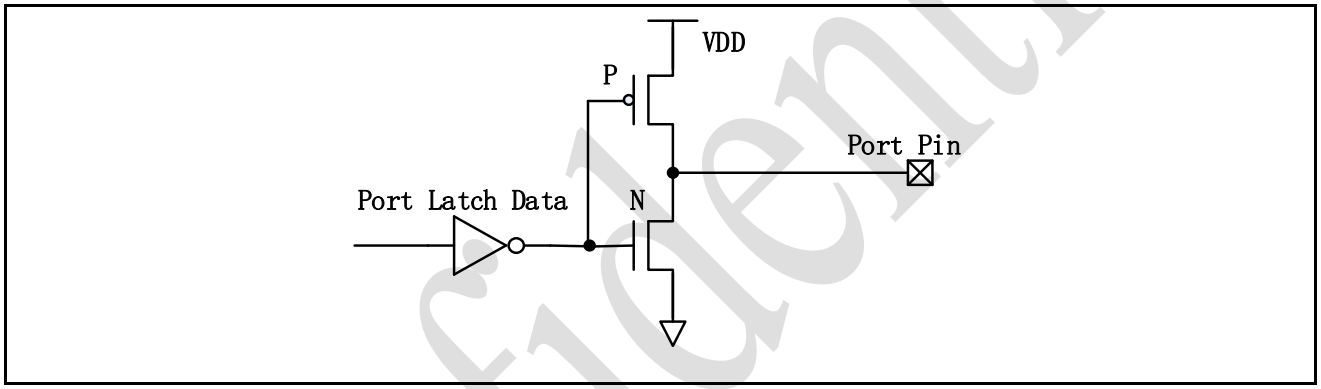

Figure 4-27 Push-Pull Output

4.6.5.3 Open-drain Output Mode

Set MODEn (Px_MODE[2n+1:2n]) to 10 as the Px.n pin is in Open-drain mode and the digital output function of I/O pin supports only sink current capability, an external pull-up register is needed for driving high state. If the bit value in the corresponding DOUT (Px_DOUT[n]) bit is 0, the pin drives a low output on the pin. If the bit value in the corresponding DOUT (Px_DOUT[n]) bit is 1, the pin output drives high that is controlled by external pull high resistor.

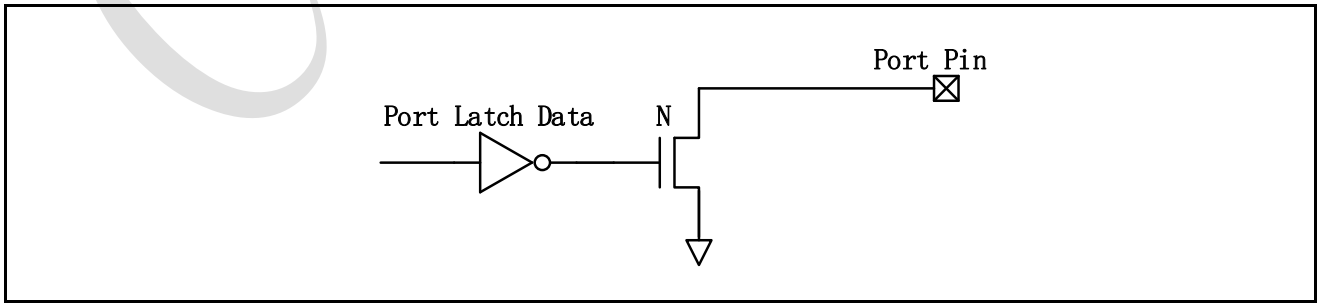

Figure 4-28 Open-Drain Output

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4.6.5.4 Quasi-bidirectional Mode

Set MODEn (Px_MODE[2n+1:2n]) to 11 as the Px.n pin is in Quasi-bidirectional mode and the I/O pin supports digital output and input function at the same time but the source current is only up to hundreds uA. Before the digital input function is performed the corresponding DOUT (Px_DOUT[n]) bit must be set to 1. If the bit value in the corresponding DOUT (Px_DOUT[n]) bit is 0, the pin drives a low output on the pin. If the bit value in the corresponding DOUT (Px_DOUT[n]) bit is 1, the pin status is controlled by the internal pull-up resistor.

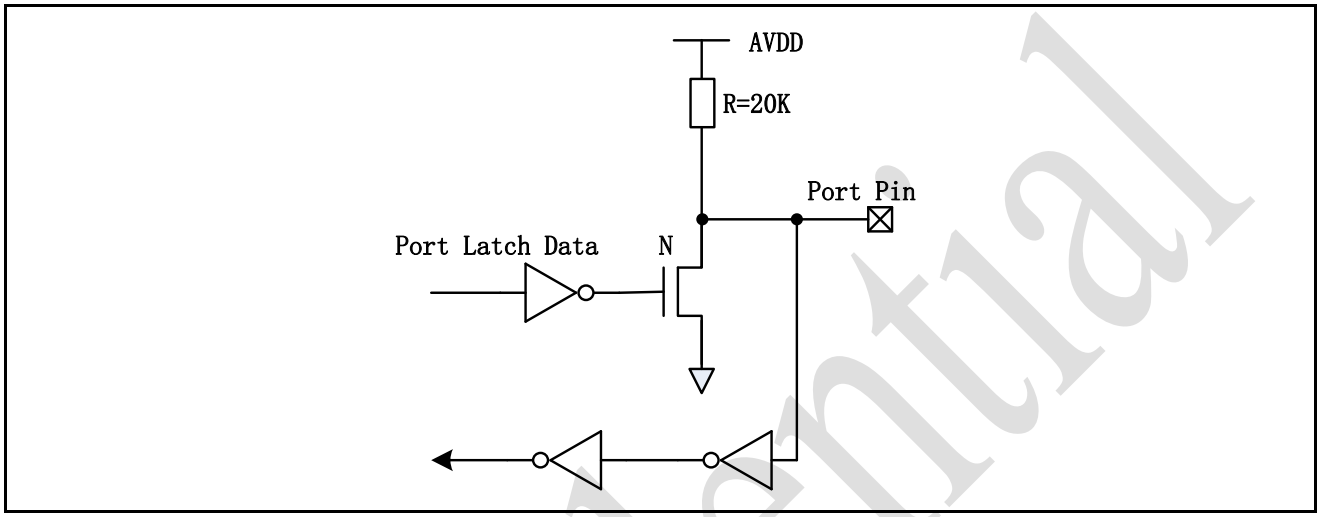

Figure 4-29 Quasi-Bidirectional I/O Mode

4.6.6 GPIO Interrupt and Wake-up Function

Each GPIO pin can be set as a chip interrupt source by setting correlative RHIEN (Px_INTEN[n+16])/ FLIEN (Px_INTEN[n]) bit and TYPE (Px_INTTYPE[n]). There are five types of interrupt conditions can be selected: low level trigger, high level trigger, falling edge trigger, rising edge trigger and both rising and falling edge trigger. For edge trigger condition, user can enable input signal de-bounce function to prevent unexpected interrupt happened which caused by noise. The de-bounce clock source and sampling cycle period can be set by DBCLKSRC (GPIO_DBCTL[4]) and DBCLKSEL (GPIO_DBCTL[3:0]) register.

The GPIO can also be the chip wake-up source when chip enters Idle/Power-down mode. The setting of wake-up trigger condition is the same as GPIO interrupt trigger.

4.6.7 GPIO Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
GPIO Base Address: **GP_BA = 0x4002_0000**				
P0_MODE	GP_BA+0x000	R/W	P0 I/O Mode Control	0x0000_0000
P0_DINOFF	GP_BA+0x004	R/W	P0 Digital Input Path Disable Control	0x00FF_0000
P0_DOUT	GP_BA+0x008	R/W	P0 Data Output Value	0x0000_00FF
P0_DATMSK	GP_BA+0x00C	R/W	P0 Data Output Write Mask	0x0000_0000
P0_PIN	GP_BA+0x010	R	P0 Pin Value	0x0000_00XX

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P0_DBEN	GP_BA+0x014	R/W	P0 De-bounce Enable Control	0x0000_0000
P0_INTTYPE	GP_BA+0x018	R/W	P0 Interrupt Mode Control	0x0000_0000
P0_INTEN	GP_BA+0x01C	R/W	P0 Interrupt Enable Control	0x0000_0000
P0_INTSRC	GP_BA+0x020	R/W	P0 Interrupt Source Flag	0x0000_0000
P1_MODE	GP_BA+0x040	R/W	P1 I/O Mode Control	0x0000_0000
P1_DINOFF	GP_BA+0x044	R/W	P1 Digital Input Path Disable Control	0x00FF_0000
P1_DOUT	GP_BA+0x048	R/W	P1 Data Output Value	0x0000_00FF
P1_DATMSK	GP_BA+0x04C	R/W	P1 Data Output Write Mask	0x0000_0000
P1_PIN	GP_BA+0x050	R	P1 Pin Value	0x0000_00XX
P1_DBEN	GP_BA+0x054	R/W	P1 De-bounce Enable Control	0x0000_0000
P1_INTTYPE	GP_BA+0x058	R/W	P1 Interrupt Mode Control	0x0000_0000
P1_INTEN	GP_BA+0x05C	R/W	P1 Interrupt Enable Control	0x0000_0000
P1_INTSRC	GP_BA+0x060	R/W	P1 Interrupt Source Flag	0x0000_0000
P2_MODE	GP_BA+0x080	R/W	P2 I/O Mode Control	0x0000_0000
P2_DINOFF	GP_BA+0x084	R/W	P2 Digital Input Path Disable Control	0x00FF_0000
P2_DOUT	GP_BA+0x088	R/W	P2 Data Output Value	0x0000_00FF
P2_DATMSK	GP_BA+0x08C	R/W	P2 Data Output Write Mask	0x0000_0000
P2_PIN	GP_BA+0x090	R	P2 Pin Value	0x0000_00XX
P2_DBEN	GP_BA+0x094	R/W	P2 De-bounce Enable Control	0x0000_0000
P2_INTTYPE	GP_BA+0x098	R/W	P2 Interrupt Mode Control	0x0000_0000
P2_INTEN	GP_BA+0x09C	R/W	P2 Interrupt Enable Control	0x0000_0000
P2_INTSRC	GP_BA+0x0A0	R/W	P2 Interrupt Source Flag	0x0000_0000
P3_MODE	GP_BA+0x0C0	R/W	P3 I/O Mode Control	0x0000_0000
P3_DINOFF	GP_BA+0x0C4	R/W	P3 Digital Input Path Disable Control	0x00FF_0000
P3_DOUT	GP_BA+0x0C8	R/W	P3 Data Output Value	0x0000_00FF
P3_DATMSK	GP_BA+0x0CC	R/W	P3 Data Output Write Mask	0x0000_0000
P3_PIN	GP_BA+0x0D0	R	P3 Pin Value	0x0000_00XX
P3_DBEN	GP_BA+0x0D4	R/W	P3 De-bounce Enable Control	0x0000_0000
P3_INTTYPE	GP_BA+0x0D8	R/W	P3 Interrupt Mode Control	0x0000_0000
P3_INTEN	GP_BA+0x0DC	R/W	P3 Interrupt Enable Control	0x0000_0000
P3_INTSRC	GP_BA+0x0E0	R/W	P3 Interrupt Source Flag	0x0000_0000
P4_MODE	GP_BA+0x100	R/W	P4 I/O Mode Control	0x0000_0000
P4_DINOFF	GP_BA+0x104	R/W	P4 Digital Input Path Disable Control	0x003F_00C0
P4_DOUT	GP_BA+0x108	R/W	P4 Data Output Value	0x0000_00FF
P4_DATMSK	GP_BA+0x10C	R/W	P4 Data Output Write Mask	0x0000_0000
P4_PIN	GP_BA+0x110	R	P4 Pin Value	0x0000_00XX
P4_DBEN	GP_BA+0x114	R/W	P4 De-bounce Enable Control	0x0000_0000
P4_INTTYPE	GP_BA+0x118	R/W	P4 Interrupt Mode Control	0x0000_0000
P4_INTEN	GP_BA+0x11C	R/W	P4 Interrupt Enable Control	0x0000_0000
P4_INTSRC	GP_BA+0x120	R/W	P4 Interrupt Source Flag	0x0000_0000
P5_MODE	GP_BA+0x140	R/W	P5 I/O Mode Control	0x0000_0000
P5_DINOFF	GP_BA+0x144	R/W	P5 Digital Input Path Disable Control	0x00FF_0000

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P5_DOUT	GP_BA+0x148	R/W	P5 Data Output Value	0x0000_00FF
P5_DATMSK	GP_BA+0x14C	R/W	P5 Data Output Write Mask	0x0000_0000
P5_PIN	GP_BA+0x150	R	P5 Pin Value	0x0000_00XX
P5_DBEN	GP_BA+0x154	R/W	P5 De-bounce Enable Control	0x0000_0000
P5_INTTYPE	GP_BA+0x158	R/W	P5 Interrupt Mode Control	0x0000_0000
P5_INTEN	GP_BA+0x15C	R/W	P5 Interrupt Enable Control	0x0000_0000
P5_INTSRC	GP_BA+0x160	R/W	P5 Interrupt Source Flag	0x0000_0000
GPIO_DBCTL	GP_BA+0x180	R/W	De-bounce Cycle Control	0x0000_0000
P00_PDIO	GP_BA+0x200	R/W	GPIO P0.0 Pin Data Input/Output	0x0000_0001
P01_PDIO	GP_BA+0x204	R/W	GPIO P0.1 Pin Data Input/Output	0x0000_0001
P02_PDIO	GP_BA+0x208	R/W	Reserved	0x0000_0001
P03_PDIO	GP_BA+0x20C	R/W	Reserved	0x0000_0001
P04_PDIO	GP_BA+0x210	R/W	GPIO P0.4 Pin Data Input/Output	0x0000_0001
P05_PDIO	GP_BA+0x214	R/W	Reserved	0x0000_0001
P06_PDIO	GP_BA+0x218	R/W	Reserved	0x0000_0001
P07_PDIO	GP_BA+0x21C	R/W	Reserved	0x0000_0001
P10_PDIO	GP_BA+0x220	R/W	GPIO P1.0 Pin Data Input/Output	0x0000_0001
P11_PDIO	GP_BA+0x224	R/W	GPIO P1.1 Pin Data Input/Output	0x0000_0001
P12_PDIO	GP_BA+0x228	R/W	GPIO P1.2 Pin Data Input/Output	0x0000_0001
P13_PDIO	GP_BA+0x22C	R/W	GPIO P1.3 Pin Data Input/Output	0x0000_0001
P14_PDIO	GP_BA+0x230	R/W	GPIO P1.4 Pin Data Input/Output	0x0000_0001
P15_PDIO	GP_BA+0x234	R/W	GPIO P1.5 Pin Data Input/Output	0x0000_0001
P16_PDIO	GP_BA+0x238	R/W	Reserved	0x0000_0001
P17_PDIO	GP_BA+0x23C	R/W	Reserved	0x0000_0001
P20_PDIO	GP_BA+0x240	R/W	Reserved	0x0000_0001
P21_PDIO	GP_BA+0x244	R/W	GPIO P2.1 Pin Data Input/Output	0x0000_0001
P22_PDIO	GP_BA+0x248	R/W	GPIO P2.2 Pin Data Input/Output	0x0000_0001
P23_PDIO	GP_BA+0x24C	R/W	GPIO P2.3 Pin Data Input/Output	0x0000_0001
P24_PDIO	GP_BA+0x250	R/W	GPIO P2.4 Pin Data Input/Output	0x0000_0001
P25_PDIO	GP_BA+0x254	R/W	GPIO P2.5 Pin Data Input/Output	0x0000_0001
P26_PDIO	GP_BA+0x258	R/W	GPIO P2.6 Pin Data Input/Output	0x0000_0001
P27_PDIO	GP_BA+0x24C	R/W	Reserved	0x0000_0001
P30_PDIO	GP_BA+0x260	R/W	Reserved	0x0000_0001
P31_PDIO	GP_BA+0x264	R/W	GPIO P3.1 Pin Data Input/Output	0x0000_0001
P32_PDIO	GP_BA+0x268	R/W	GPIO P3.2 Pin Data Input/Output	0x0000_0001
P33_PDIO	GP_BA+0x26C	R/W	Reserved	0x0000_0001
P34_PDIO	GP_BA+0x270	R/W	GPIO P3.4 Pin Data Input/Output	0x0000_0001
P35_PDIO	GP_BA+0x274	R/W	GPIO P3.5 Pin Data Input/Output	0x0000_0001
P36_PDIO	GP_BA+0x278	R/W	GPIO P3.6 Pin Data Input/Output	0x0000_0001
P37_PDIO	GP_BA+0x27C	R/W	Reserved	0x0000_0001
P40_PDIO	GP_BA+0x280	R/W	Reserved	0x0000_0001
P41_PDIO	GP_BA+0x284	R/W	Reserved	0x0000_0001

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P42_PDIO	GP_BA+0x288	R/W	Reserved	0x0000_0001
P43_PDIO	GP_BA+0x28C	R/W	Reserved	0x0000_0001
P44_PDIO	GP_BA+0x290	R/W	Reserved	0x0000_0001
P45_PDIO	GP_BA+0x294	R/W	Reserved	0x0000_0001
P46_PDIO	GP_BA+0x298	R/W	GPIO P4.6 Pin Data Input/Output	0x0000_0001
P47_PDIO	GP_BA+0x29C	R/W	GPIO P4.7 Pin Data Input/Output	0x0000_0001
P50_PDIO	GP_BA+0x2A0	R/W	GPIO P5.0 Pin Data Input/Output	0x0000_0001
P51_PDIO	GP_BA+0x2A4	R/W	GPIO P5.1 Pin Data Input/Output	0x0000_0001
P52_PDIO	GP_BA+0x2A8	R/W	Reserved	0x0000_0001
P53_PDIO	GP_BA+0x2AC	R/W	GPIO P5.3 Pin Data Input/Output	0x0000_0001
P54_PDIO	GP_BA+0x2B0	R/W	GPIO P5.4 Pin Data Input/Output	0x0000_0001
P55_PDIO	GP_BA+0x2B4	R/W	GPIO P5.5 Pin Data Input/Output	0x0000_0001
P56_PDIO	GP_BA+0x2B8	R/W	GPIO P5.6 Pin Data Input/Output	0x0000_0001
P57_PDIO	GP_BA+0x2BC	R/W	GPIO P5.7 Pin Data Input/Output	0x0000_0001

4.6.8 GPIO Register Description

4.6.8.1 Port 0-5 I/O Mode Control (Px_MODE)

Register	Offset	R/W	Description	Reset Value
P0_MODE	GP_BA+0x000	R/W	P0 I/O Mode Control	0x0000_0000
P1_MODE	GP_BA+0x040	R/W	P1 I/O Mode Control	0x0000_0000
P2_MODE	GP_BA+0x080	R/W	P2 I/O Mode Control	0x0000_0000
P3_MODE	GP_BA+0x0C0	R/W	P3 I/O Mode Control	0x0000_0000
P4_MODE	GP_BA+0x100	R/W	P4 I/O Mode Control	0x0000_0000
P5_MODE	GP_BA+0x140	R/W	P5 I/O Mode Control	0x0000_0000

Bits	Descriptions	
[31:16]	Reserved	Reserved.
[2n+1:2n] n=0,1..7	MODEn	Port 0-5 I/O Pin[N] Mode Control Determine each I/O mode of Px.n pins. 00 = Px.n is in Input mode. 01 = Px.n is in Push-pull Output mode. 10 = Px.n is in Open-drain Output mode. 11 = Px.n is in Quasi-bidirectional mode. **Note1**: Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,5 are reserved. Max. n=7 for port 5

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4.6.8.2 Port 0-5 Digital Input Path Disable Control (Px_DINOFF)

Register	Offset	R/W	Description	Reset Value
P0_DINOFF	GP_BA+0x004	R/W	P0 Digital Input Path Disable Control	0x00FF_0000
P1_DINOFF	GP_BA+0x044	R/W	P1 Digital Input Path Disable Control	0x00FF_0000
P2_DINOFF	GP_BA+0x084	R/W	P2 Digital Input Path Disable Control	0x00FF_0000
P3_DINOFF	GP_BA+0x0C4	R/W	P3 Digital Input Path Disable Control	0x00FF_0000
P4_DINOFF	GP_BA+0x104	R/W	P4 Digital Input Path Disable Control	0x003F_00C0
P5_DINOFF	GP_BA+0x144	R/W	P5 Digital Input Path Disable Control	0x00FF_0000

Bits	Descriptions	
[31:24]	Reserved	Reserved.
[n+16] n=0,1..7	DINOFF[n]	Port 0-5 Pin[N] Digital Input Path Disable Control Each of these bits is used to control if the digital input path of corresponding Px.n pin is disabled. If input is analog signal, users can disable Px.n digital input path to avoid input current leakage. 0 = Px.n digital input path enabled. 1 = Px.n digital input path disabled (digital input tied to low). Note1: Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,5 are reserved. Max. n=7 for port 5
[15:8]	Reserved	Reserved.
[n] n=0,1..7	PUEN[n]	Port 0-5 Pin[N] Digital Pull Up Path Enable Control Each of these bits is used to control if the digital pull up path of corresponding Px.n pin is enabled. 0 = Px.n digital pull up path disabled. 1 = Px.n digital pull up path enabled.

4.6.8.3 Port 0-5 Data Output Value (Px_DOUT)

Register	Offset	R/W	Description	Reset Value
P0_DOUT	GP_BA+0x008	R/W	P0 Data Output Value	0x0000_00FF
P1_DOUT	GP_BA+0x048	R/W	P1 Data Output Value	0x0000_00FF
P2_DOUT	GP_BA+0x088	R/W	P2 Data Output Value	0x0000_00FF
P3_DOUT	GP_BA+0x0C8	R/W	P3 Data Output Value	0x0000_00FF
P4_DOUT	GP_BA+0x108	R/W	P4 Data Output Value	0x0000_00FF
P5_DOUT	GP_BA+0x148	R/W	P5 Data Output Value	0x0000_00FF

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Bits	Descriptions	
[31:8]	Reserved	Reserved.
[n] n=0,1..7	DOUT[n]	Port 0-5 Pin[N] Output Value Each of these bits controls the status of a Px.n pin when the Px.n is configured as Push-pull output, Open-drain output or Quasi-bidirectional mode. 0 = Px.n will drive Low if the Px.n pin is configured as Push-pull output, Open-drain output or Quasi-bidirectional mode. 1 = Px.n will drive High if the Px.n pin is configured as Push-pull output or Quasi-bidirectional mode. **Note1**: Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,5 are reserved. Max. n=7 for port 5

4.6.8.4 Port 0-5 Data Output Write Mask (Px_DATMSK)

Register	Offset	R/W	Description	Reset Value
P0_DATMSK	GP_BA+0x00C	R/W	P0 Data Output Write Mask	0x0000_0000
P1_DATMSK	GP_BA+0x04C	R/W	P1 Data Output Write Mask	0x0000_0000
P2_DATMSK	GP_BA+0x08C	R/W	P2 Data Output Write Mask	0x0000_0000
P3_DATMSK	GP_BA+0x0CC	R/W	P3 Data Output Write Mask	0x0000_0000
P4_DATMSK	GP_BA+0x10C	R/W	P4 Data Output Write Mask	0x0000_0000
P5_DATMSK	GP_BA+0x14C	R/W	P5 Data Output Write Mask	0x0000_0000

Bits	Descriptions	
[31:8]	Reserved	Reserved.
[n] n=0,1..7	DATMSK[n]	Port 0-5 Pin[N] Data Output Write Mask These bits are used to protect the corresponding DOUT (Px_DOUT[n]) bit. When the DATMSK (Px_DATMSK[n]) bit is set to 1, the corresponding DOUT (Px_DOUT[n]) bit is protected. If the write signal is masked, writing data to the protect bit is ignore. 0 = Corresponding DOUT (Px_DOUT[n]) bit can be updated. 1 = Corresponding DOUT (Px_DOUT[n]) bit protected. **Note**: This function only protects the corresponding DOUT (Px_DOUT[n]) bit, and will not protect the corresponding PDIO (Pxn_PDIO[0]) bit. **Note**: Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,5 are reserved.

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		Max. n=7 for port 5

4.6.8.5 Port 0-5 Pin Value (Px_PIN)

Register	Offset	R/W	Description	Reset Value
P0_PIN	GP_BA+0x010	R	P0 Pin Value	0x0000_00XX
P1_PIN	GP_BA+0x050	R	P1 Pin Value	0x0000_00XX
P2_PIN	GP_BA+0x090	R	P2 Pin Value	0x0000_00XX
P3_PIN	GP_BA+0x0D0	R	P3 Pin Value	0x0000_00XX
P4_PIN	GP_BA+0x110	R	P4 Pin Value	0x0000_00XX
P5_PIN	GP_BA+0x150	R	P5 Pin Value	0x0000_00XX

Bits	Descriptions	
[31:8]	Reserved	Reserved.
[n] n=0,1..7	PIN[n]	Port 0-5 Pin[N] Pin Value Each bit of the register reflects the actual status of the respective Px.n pin. If the bit is 1, it indicates the corresponding pin status is high; else the pin status is low. **Note1**: Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,5 are reserved. Max. n=7 for port 5

4.6.8.6 Port 0-5 De-bounce Enable Control (Px_DBEN)

Register	Offset	R/W	Description	Reset Value
P0_DBEN	GP_BA+0x014	R/W	P0 De-bounce Enable Control	0x0000_0000
P1_DBEN	GP_BA+0x054	R/W	P1 De-bounce Enable Control	0x0000_0000
P2_DBEN	GP_BA+0x094	R/W	P2 De-bounce Enable Control	0x0000_0000
P3_DBEN	GP_BA+0x0D4	R/W	P3 De-bounce Enable Control	0x0000_0000
P4_DBEN	GP_BA+0x114	R/W	P4 De-bounce Enable Control	0x0000_0000
P5_DBEN	GP_BA+0x154	R/W	P5 De-bounce Enable Control	0x0000_0000

Bits	Descriptions	
[31:8]	Reserved	Reserved.
[n] n=0,1..7	DBEN[n]	Port 0-5 Pin[N] Input Signal De-bounce Enable Bit The DBEN[n] bit is used to enable the de-bounce function for each corresponding bit. If the input signal pulse width cannot be sampled by continuous two de-bounce sample cycle, the input signal transition is seen as the signal bounce and will not trigger the interrupt. The de-bounce clock source is controlled by DBCLKSRC (GPIO_DBCTL [4]), one

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		de-bounce sample cycle period is controlled by DBCLKSEL (GPIO_DBCTL [3:0]). 0 = Px.n de-bounce function disabled. 1 = Px.n de-bounce function enabled. The de-bounce function is valid only for edge triggered interrupt. If the interrupt mode is level triggered, the de-bounce enable bit will be ignored. **Note**: If Px.n pin is chosen as Power-down wake-up source, user should be disable the de-bounce function before entering Power-down mode to avoid the second interrupt event occurred after system woken up which caused by Px.n de-bounce function. **Note1**: Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,5 are reserved. Max. n=7 for port 5

4.6.8.7 Port 0-5 Interrupt Mode Control (Px_ INTTYPE)

Register	Offset	R/W	Description	Reset Value
P0_INTTYPE	GP_BA+0x018	R/W	P0 Interrupt Mode Control	0x0000_0000
P1_INTTYPE	GP_BA+0x058	R/W	P1 Interrupt Mode Control	0x0000_0000
P2_INTTYPE	GP_BA+0x098	R/W	P2 Interrupt Mode Control	0x0000_0000
P3_INTTYPE	GP_BA+0x0D8	R/W	P3 Interrupt Mode Control	0x0000_0000
P4_INTTYPE	GP_BA+0x118	R/W	P4 Interrupt Mode Control	0x0000_0000
P5_INTTYPE	GP_BA+0x158	R/W	P5 Interrupt Mode Control	0x0000_0000

Bits	Descriptions	
[31:8]	Reserved	Reserved.
[n] n=0,1..7	TYPE[n]	Port 0-5 Pin[N] Edge or Level Detection Interrupt Trigger Type Control TYPE (Px_INTTYPE[n]) bit is used to control the triggered interrupt which is by level trigger or by edge trigger. If the interrupt is edge-triggerred, the trigger source can be controlled by de-bounce. If the interrupt is level-triggerred, the input source is sampled by one AHB_CLK clock and generates the interrupt. 0 = Edge trigger interrupt. 1 = Level trigger interrupt. If the pin is set as the level trigger interrupt, only one level can be set on the registers RHIEN (Px_INTEN[n+16])/FLIEN (Px_INTEN[n]). If both levels to trigger interrupt are set, the setting will be ignored and no interrupt will occur. The de-bounce function is valid only for edge-triggered interrupt. If the interrupt mode is level-triggered, the de-bounce enable bit will be ignore. **Note1**:

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		Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,5 are reserved. Max. n=7 for port 5

4.6.8.8 Port 0-5 Interrupt Enable Control (Px_INTEN)

Register	Offset	R/W	Description	Reset Value
P0_INTEN	GP_BA+0x01C	R/W	P0 Interrupt Enable Control	0x0000_0000
P1_INTEN	GP_BA+0x05C	R/W	P1 Interrupt Enable Control	0x0000_0000
P2_INTEN	GP_BA+0x09C	R/W	P2 Interrupt Enable Control	0x0000_0000
P3_INTEN	GP_BA+0x0DC	R/W	P3 Interrupt Enable Control	0x0000_0000
P4_INTEN	GP_BA+0x11C	R/W	P4 Interrupt Enable Control	0x0000_0000
P5_INTEN	GP_BA+0x15C	R/W	P5 Interrupt Enable Control	0x0000_0000

Bits	Descriptions	
[31:24]	Reserved	Reserved.
[n+16] n=0,1..7	RHIEN[n]	Port 0-5 Pin[N] Rising Edge or High Level Interrupt Trigger Type Enable Bit The RHIEN (Px_INTEN[n+16]) bit is used to enable the interrupt for each of the corresponding input Px.n pin. Setting bit to 1 also enables the pin wake-up function. When setting the RHIEN (Px_INTEN[n+16]) bit to 1: If the interrupt is level trigger (TYPE (Px_INTTYPE[n]) bit is set to 1), the input Px.n pin will generate the interrupt while this pin state is at high level. If the interrupt is edge trigger (TYPE (Px_INTTYPE[n]) bit is set to 0), the input Px.n pin will generate the interrupt while this pin state changes from low to high. 0 = Px.n level high or low to high interrupt disabled. 1 = Px.n level high or low to high interrupt enabled. **Note1**: Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,5 are reserved. Max. n=7 for port 5
[15:8]	Reserved	Reserved.
[n] n=0,1..7	FLIEN[n]	Port 0-5 Pin[N] Falling Edge or Low Level Interrupt Trigger Type Enable Bit The FLIEN (Px_INTEN[n]) bit is used to enable the interrupt for each of the corresponding input Px.n pin. Setting bit to 1 also enables the pin wake-up function. When setting the FLIEN (Px_INTEN[n]) bit to 1: If the interrupt is level trigger (TYPE (Px_INTTYPE[n]) bit is set to 1), the input Px.n pin will generate the interrupt while this pin state is at low level. If the interrupt is edge trigger (TYPE (Px_INTTYPE[n]) bit is set to 0), the input Px.n

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		pin will generate the interrupt while this pin state changed from high to low. 0 = Px.n level low or high to low interrupt disabled. 1 = Px.n level low or high to low interrupt enabled. **Note1**: Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,5 are reserved. Max. n=7 for port 5

4.6.8.9 Port 0-5 Interrupt Source Flag (Px_INTSRC)

Register	Offset	R/W	Description	Reset Value
P0_INTSRC	GP_BA+0x020	R/W	P0 Interrupt Source Flag	0x0000_0000
P1_INTSRC	GP_BA+0x060	R/W	P1 Interrupt Source Flag	0x0000_0000
P2_INTSRC	GP_BA+0x0A0	R/W	P2 Interrupt Source Flag	0x0000_0000
P3_INTSRC	GP_BA+0x0E0	R/W	P3 Interrupt Source Flag	0x0000_0000
P4_INTSRC	GP_BA+0x120	R/W	P4 Interrupt Source Flag	0x0000_0000
P5_INTSRC	GP_BA+0x160	R/W	P5 Interrupt Source Flag	0x0000_0000

Bits	Descriptions	
[31:8]	Reserved	Reserved.
[n] n=0,1..7	INTSRC[n]	Port 0-5 Pin[N] Interrupt Source Flag Write Operation: 0 = No action. 1 = Clear the corresponding pending interrupt. Read Operation: 0 = No interrupt at Px.n. 1 = Px.n generates an interrupt. **Note1**: Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,.5 are reserved. Max. n=7 for port 5

4.6.8.10 Interrupt De-bounce Cycle Control (GPIO_DBCTL)

Register	Offset	R/W	Description	Reset Value
GPIO_DBCTL	GP_BA+0x180	R/W	De-bounce Cycle Control	0x0000_0000

Bits	Descriptions

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[31:5]	Reserved	Reserved.
[4]	DBCLKSRC	De-bounce Counter Clock Source Selection 0 = De-bounce counter clock source is AHB_CLK. 1 = De-bounce counter clock source is 32 KHz internal low speed RC oscillator (RCL).
[3:0]	DBCLKSEL	De-bounce Sampling Cycle Selection 0000 = Sample interrupt input once per 1 clock. 0001 = Sample interrupt input once per 2 clocks. 0010 = Sample interrupt input once per 4 clocks. 0011 = Sample interrupt input once per 8 clocks. 0100 = Sample interrupt input once per 16 clocks. 0101 = Sample interrupt input once per 32 clocks. 0110 = Sample interrupt input once per 64 clocks. 0111 = Sample interrupt input once per 128 clocks. 1000 = Sample interrupt input once per 256 clocks. 1001 = Sample interrupt input once per 2*256 clocks. 1010 = Sample interrupt input once per 4*256 clocks. 1011 = Sample interrupt input once per 8*256 clocks. 1100 = Sample interrupt input once per 16*256 clocks. 1101 = Sample interrupt input once per 32*256 clocks. 1110 = Sample interrupt input once per 64*256 clocks. 1111 = Sample interrupt input once per 128*256 clocks.

4.6.8.11 GPIO Px.n Data Input/Output (Pxn_PDIO)

Register	Offset	R/W	Description	Reset Value
P00_PDIO	GP_BA+0x200	R/W	GPIO P0.0 Pin Data Input/Output	0x0000_0001
P01_PDIO	GP_BA+0x204	R/W	GPIO P0.1 Pin Data Input/Output	0x0000_0001
P02_PDIO	GP_BA+0x208	R/W	Reserved	0x0000_0001
P03_PDIO	GP_BA+0x20C	R/W	Reserved	0x0000_0001
P04_PDIO	GP_BA+0x210	R/W	GPIO P0.4 Pin Data Input/Output	0x0000_0001
P05_PDIO	GP_BA+0x214	R/W	Reserved	0x0000_0001
P06_PDIO	GP_BA+0x218	R/W	Reserved	0x0000_0001
P07_PDIO	GP_BA+0x21C	R/W	Reserved	0x0000_0001
P10_PDIO	GP_BA+0x220	R/W	GPIO P1.0 Pin Data Input/Output	0x0000_0001
P11_PDIO	GP_BA+0x224	R/W	GPIO P1.1 Pin Data Input/Output	0x0000_0001
P12_PDIO	GP_BA+0x228	R/W	GPIO P1.2 Pin Data Input/Output	0x0000_0001
P13_PDIO	GP_BA+0x22C	R/W	GPIO P1.3 Pin Data Input/Output	0x0000_0001
P14_PDIO	GP_BA+0x230	R/W	GPIO P1.4 Pin Data Input/Output	0x0000_0001
P15_PDIO	GP_BA+0x234	R/W	GPIO P1.5 Pin Data Input/Output	0x0000_0001
P16_PDIO	GP_BA+0x238	R/W	Reserved	0x0000_0001
P17_PDIO	GP_BA+0x23C	R/W	Reserved	0x0000_0001
P20_PDIO	GP_BA+0x240	R/W	Reserved	0x0000_0001
P21_PDIO	GP_BA+0x244	R/W	GPIO P2.1 Pin Data Input/Output	0x0000_0001

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P22_PDIO	GP_BA+0x248	R/W	GPIO P2.2 Pin Data Input/Output	0x0000_0001
P23_PDIO	GP_BA+0x24C	R/W	GPIO P2.3 Pin Data Input/Output	0x0000_0001
P24_PDIO	GP_BA+0x250	R/W	GPIO P2.4 Pin Data Input/Output	0x0000_0001
P25_PDIO	GP_BA+0x254	R/W	GPIO P2.5 Pin Data Input/Output	0x0000_0001
P26_PDIO	GP_BA+0x258	R/W	GPIO P2.6 Pin Data Input/Output	0x0000_0001
P27_PDIO	GP_BA+0x24C	R/W	Reserved	0x0000_0001
P30_PDIO	GP_BA+0x260	R/W	Reserved	0x0000_0001
P31_PDIO	GP_BA+0x264	R/W	GPIO P3.1 Pin Data Input/Output	0x0000_0001
P32_PDIO	GP_BA+0x268	R/W	GPIO P3.2 Pin Data Input/Output	0x0000_0001
P33_PDIO	GP_BA+0x26C	R/W	Reserved	0x0000_0001
P34_PDIO	GP_BA+0x270	R/W	GPIO P3.4 Pin Data Input/Output	0x0000_0001
P35_PDIO	GP_BA+0x274	R/W	GPIO P3.5 Pin Data Input/Output	0x0000_0001
P36_PDIO	GP_BA+0x278	R/W	GPIO P3.6 Pin Data Input/Output	0x0000_0001
P37_PDIO	GP_BA+0x27C	R/W	Reserved	0x0000_0001
P40_PDIO	GP_BA+0x280	R/W	Reserved	0x0000_0001
P41_PDIO	GP_BA+0x284	R/W	Reserved	0x0000_0001
P42_PDIO	GP_BA+0x288	R/W	Reserved	0x0000_0001
P43_PDIO	GP_BA+0x28C	R/W	Reserved	0x0000_0001
P44_PDIO	GP_BA+0x290	R/W	Reserved	0x0000_0001
P45_PDIO	GP_BA+0x294	R/W	Reserved	0x0000_0001
P46_PDIO	GP_BA+0x298	R/W	GPIO P4.6 Pin Data Input/Output	0x0000_0001
P47_PDIO	GP_BA+0x29C	R/W	GPIO P4.7 Pin Data Input/Output	0x0000_0001
P50_PDIO	GP_BA+0x2A0	R/W	GPIO P5.0 Pin Data Input/Output	0x0000_0001
P51_PDIO	GP_BA+0x2A4	R/W	GPIO P5.1 Pin Data Input/Output	0x0000_0001
P52_PDIO	GP_BA+0x2A8	R/W	Reserved	0x0000_0001
P53_PDIO	GP_BA+0x2AC	R/W	GPIO P5.3 Pin Data Input/Output	0x0000_0001
P54_PDIO	GP_BA+0x2B0	R/W	GPIO P5.4 Pin Data Input/Output	0x0000_0001
P55_PDIO	GP_BA+0x2B4	R/W	GPIO P5.5 Pin Data Input/Output	0x0000_0001
P56_PDIO	GP_BA+0x2B8	R/W	GPIO P5.6 Pin Data Input/Output	0x0000_0001
P57_PDIO	GP_BA+0x2BC	R/W	GPIO P5.7 Pin Data Input/Output	0x0000_0001

Bits	Descriptions	
[31:1]	Reserved	Reserved.
[0]	PDIO	GPIO Px.N Pin Data Input/Output Writing this bit can control one GPIO pin output value. 0 = Corresponding GPIO pin set to low. 1 = Corresponding GPIO pin set to high. Read this register to get GPIO pin status. For example, writing P00_PDIO will reflect the written value to bit DOUT (P0_DOUT[0]), reading P00_PDIO will return the value of PIN (P0_PIN[0]). **Note1**: The writing operation will not be affected by register DATMSK (Px_DATMSK[n]).

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		Note1: Max. n=7 for port 0. Max. n=7 for port 1. Max. n=7 for port 2. Max. n=7 for port 3, n=3, n=7 are reserved. Max. n=7 for port 4, n=0,.5 are reserved. Max. n=7 for port 5

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4.7 Timer Controller (TMR)

4.7.1 Overview

The Timer Controller includes three 32-bit timers, TMR0, TMR1 and TMR2, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, event counting by external input pins, and interval measurement by external capture pins.

4.7.2 Features

- Three sets of 32-bit timer with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMRTx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

4.7.3 Block Diagram

The timer controller block diagram and clock control are shown in Figure 4-30 and Figure 4-31.

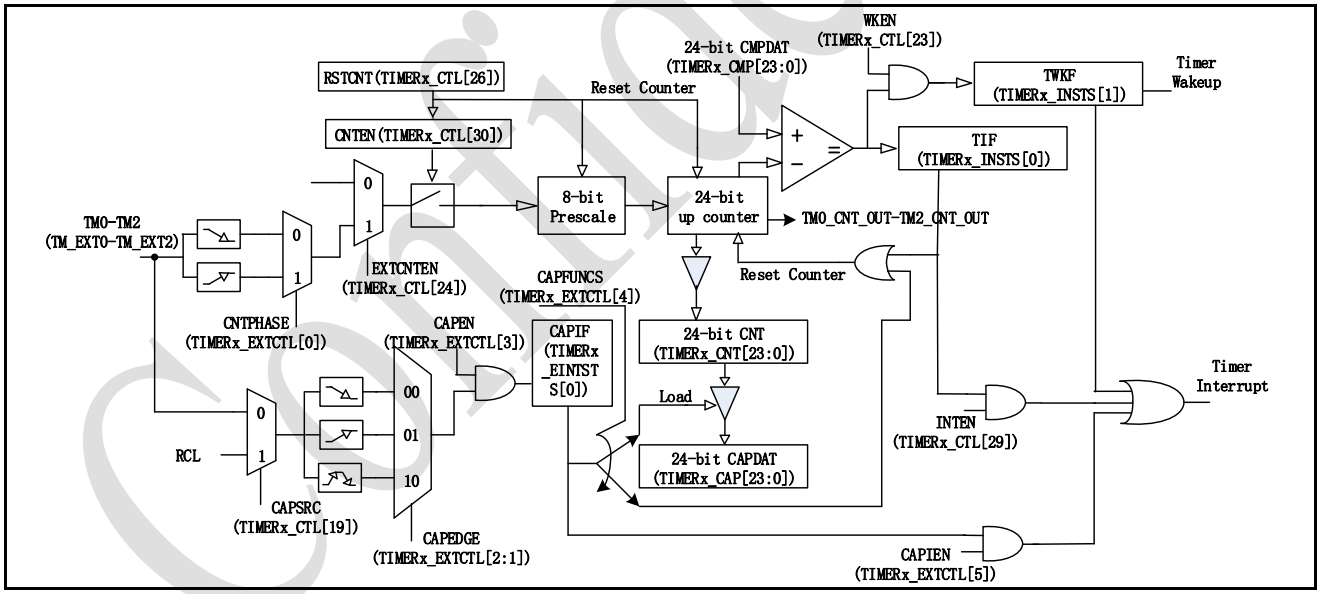

Figure 4-30 Timer Controller Block Diagram (Three TRM)

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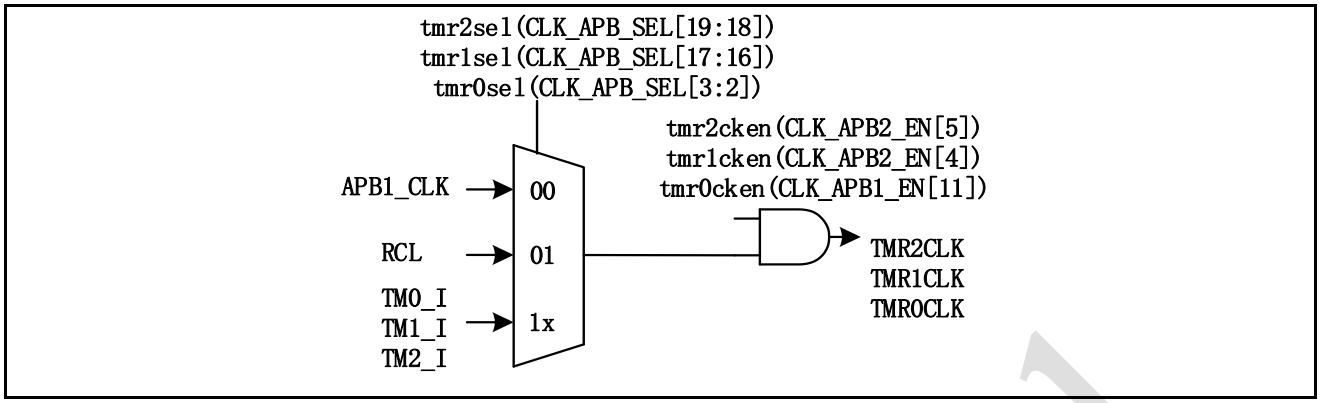

Figure 4-31 Clock Source of Timer Controller (Three TRM)

4.7.4 Basic Configuration

The peripheral clock source of TMR0 , TMR1, and TMR2 can be enabled by tmr0cken(CLK_APB1_EN[11]), tmr1cken(CLK_APB2_EN[4]), tmr2cken(CLK_APB2_EN[5]) respectively and selected as clock source in tmr0sel (CLK_APB_SEL[3:2]) for TMR0, tmr1sel (CLK_APB_SEL[17:16]) for TMR1, and tmr2sel (CLK_APB_SEL[19:18]) for TMR2.

4.7.5 Functional Description

4.7.5.1 Timer Flag

The timer controller supports two interrupt flags; one is TF (TIMERx_INTSTS[2]) which is set while timer counter value CNT (TIMERx_CNT[23:0]) matches the timer compared value CMPDAT (TIMERx_CMP[23:0]), and the other is CAPF (TIMERx_EINTSTS[1]) which is set when the transition on the TMx_EXT pin associated CAPEDGE (TIMERx_EXTCTL[2:1]) setting.

4.7.5.2 Timer Interrupt Flag

The timer controller supports two interrupt flags; one is TIF (TIMERx_INTSTS[0]) which is set while timer counter value CNT (TIMERx_CNT[23:0]) matches the timer compared value CMPDAT (TIMERx_CMP[23:0])and INTEN (TIMERx_CTL[29]) is set to 1.And the other is CAPIF (TIMERx_EINTSTS[0]) which is set when the transition on the TMx_EXT pin associated CAPEDGE (TIMERx_EXTCTL[2:1]) setting, and CAPIEN (TIMERx_EXTCTL[5]) is set to 1.

4.7.5.3 Timer Counting Operation Mode

The Timer controller provides four timer counting modes: One-shot, Periodic, Toggle-output and Continuous Counting operation modes as described below.

4.7.5.3.1. One-shot Mode

If the timer controller is configured in one-shot mode OPMODE (TIMERx_CTL[28:27] is 2’b00) and CNTEN (TIMERx_CTL[30]) is set, the timer counter starts up_counting. Once the CNT (TIMERx_CNT[23:0]) value reaches CMPDAT (TIMERx_CMP[23:0]) value, the TIF (TIMERx_INTSTS[0]) will be set to 1, CNT value and CNTEN bit is cleared automatically by timer controller then timer counting operation stops. In the meantime, if the INTEN (TIMERx_CTL[29]) is enabled, the timer interrupt signal is generated and sent to NVIC to inform CPU.

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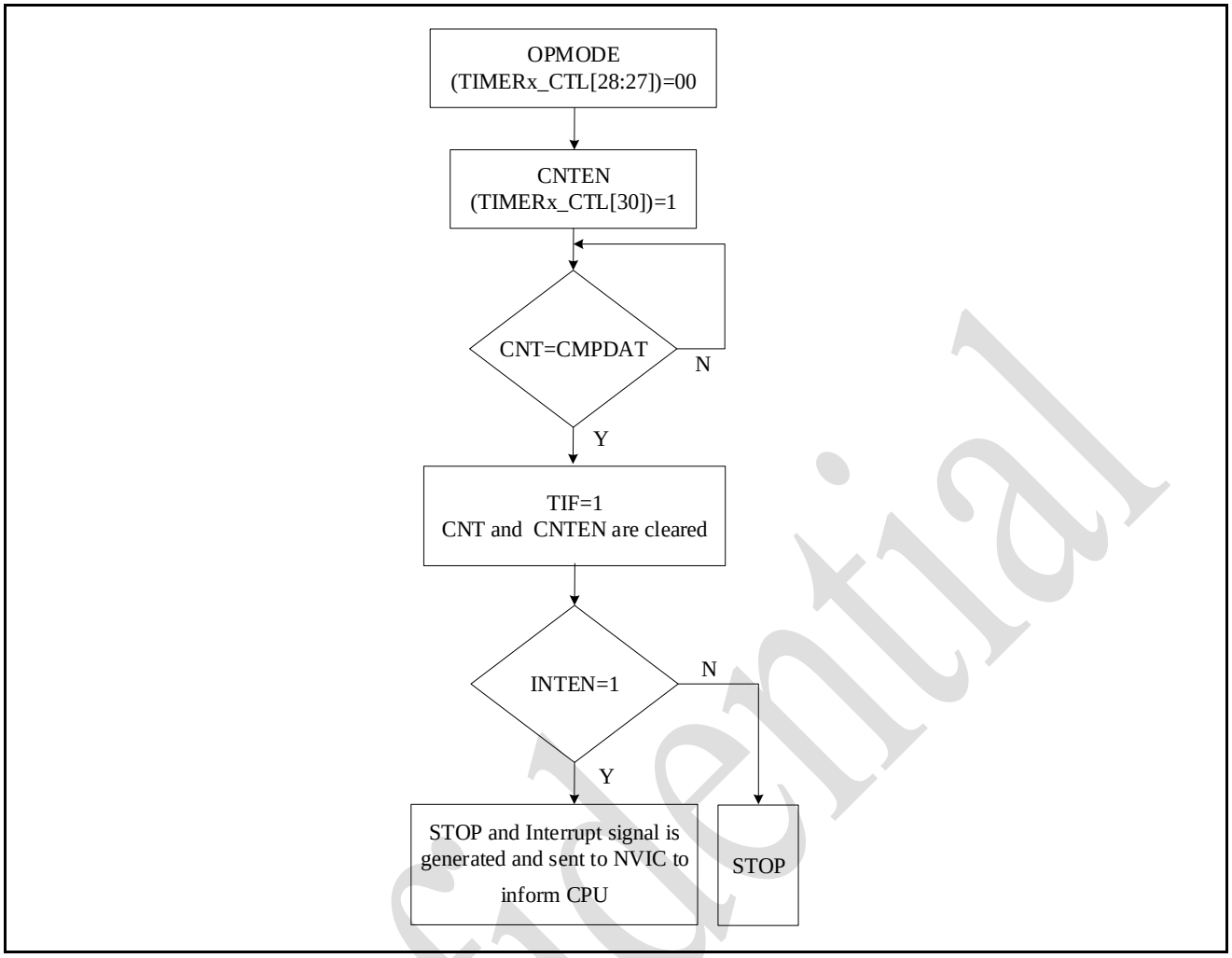

Figure 4-32 One-shot Mode

4.7.5.3.2. Periodic Mode

If the timer controller is configured at periodic mode (TIMERx_CTL[28:27] is 2'b01) and CNTEN (TIMERx_CTL[30]) is set, the timer counter starts up_counting. Once the CNT (TIMERx_CNT[23:0]) value reaches CMPDAT (TIMERx_CMP[23:0]) value, the TIF (TIMERx_INTSTS[0]) will be set to 1, CNT value will be cleared automatically by timer controller and timer counter operates counting again. In the meantime, if the INTEN (TIMERx_CTL[29]) bit is enabled, the timer interrupt signal is generated and sent to NVIC to inform CPU also. In this mode, the timer controller operates counting and compares with CMPDAT value periodically until the CNTEN bit is cleared by user.

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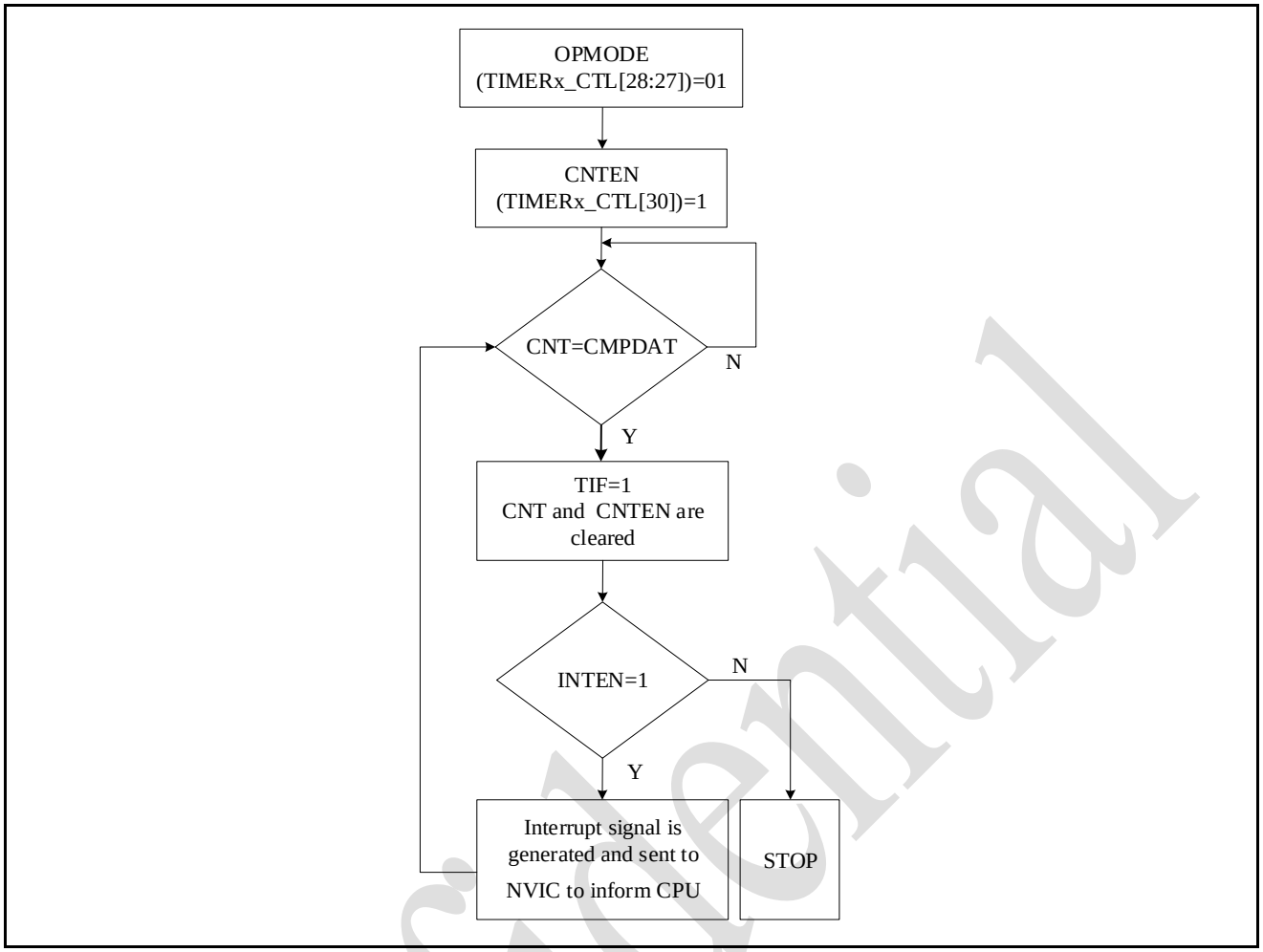

Figure 4-33 Periodic Mode

4.7.5.3.3. Toggle-output Mode

If the timer controller is configured at toggle-output mode (TIMERx_CTL[28:27] is 2'b10) and CNTEN (TIMERx_CTL[30]) is set, the timer counter starts up_counting. The counting operation of toggle-output mode is almost the same as periodic mode, except toggle-output mode has associated TM0 ~ TM2 pin to output signal while specify TIF (TIMERx_INTSTS[0]) is set. Thus, the toggle-output signal on TMx_CNT_OUT（x=0,1,2）pin is high and changing back and forth with 50% duty cycle.

4.7.5.3.4. Continuous Counting Mode

If the timer controller is configured at continuous counting mode (TIMERx_CTL[28:27] is 2'b11) and CNTEN (TIMERx_CTL[30]) is set, the timer counter starts up_counting. Once the CNT (TIMERx_CNT[23:0]) value reaches the CMPDAT (TIMERx_CMP[23:0]) value, the TIF (TIMERx_INTSTS[0]) will be set to 1 and the CNT value keeps up_counting. In the meantime, if the INTEN (TIMERx_CTL[29]) is enabled, the timer interrupt signal is generated and sent to NVIC to inform CPU. User can change different CMPDAT value immediately without disabling timer counting and restarting timer counting in this mode.

For example, CMPDAT value is set as 80, first. The TIF will set to 1 when CNT value is equal to 80, the timer counter is kept counting and CNT value will not go back to 0, it continues to count 81, 82, 83,…to 2^{24}-1, 0, 1, 2, 3, …to 2^{24}-1 again and again. Next, if user programs the CMPDAT value

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as 200 and clears TIF, the TIF will be set to 1 again when CNT value reaches 200. At last, user programs CMPDAT as 500 and clears TIF, the TIF will set to 1 again when CNT value reaches to 500. In this mode, the timer counting is continuous.

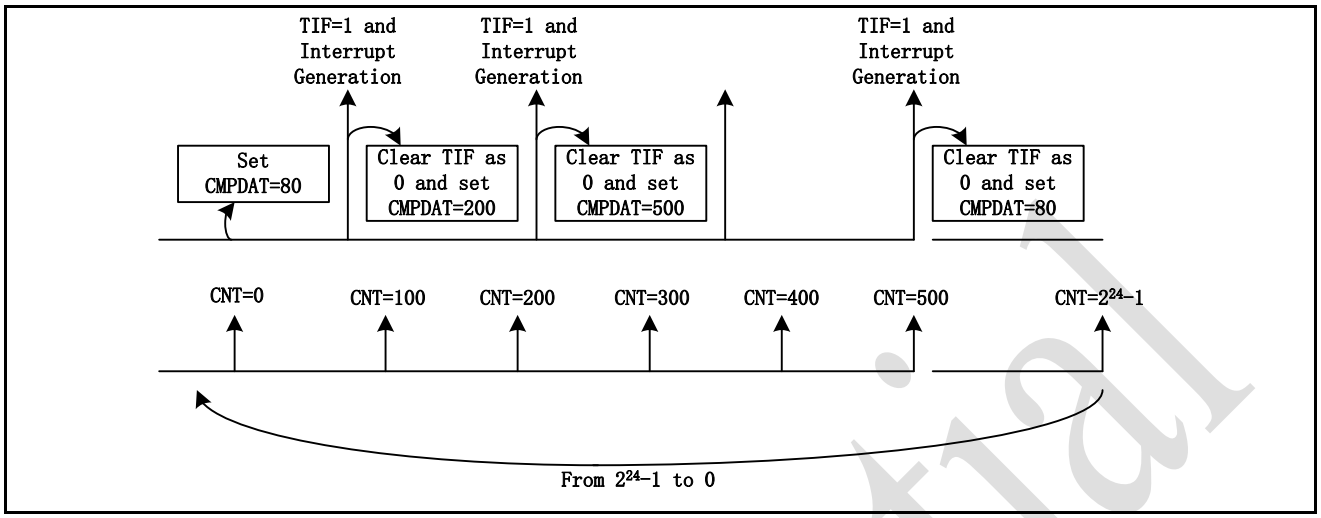

Figure 4-34 Continuous Counting Mode

4.7.5.4 Event Counting Mode

The timer controller also provides an application which can count the input event from TMx (x= 0~2) pin and the number of event will reflect to CNT (TIMERx_CNT[23:0]) value. It is also called as event counting function. In this function, EXTCNTEN (TIMERx_CTL[24]) should be set and the timer peripheral clock source should be set as APB_CLK.

User can enable or disable TMx pin de-bounce circuit by setting CNTDBEN (TIMERx_EXTCTL[7]). The input event frequency should be less than 1/3 AHB_CLK if TMx pin de-bounce disabled or less than 1/8 AHB_CLK if TMx pin de-bounce enabled to assure the returned CNT value is correct, and user can also select edge detection phase of TMx pin by setting CNTPHASE (TIMERx_EXTCTL[0]) bit.

In event counting mode, the timer counting operation mode can be selected as one-shot, periodic and continuous counting mode to counts the counter value CNT (TIMERx_CNT[23:0]) from TMx pin.

4.7.5.5 Input Capture Function

The input capture or reset function is provided to capture or reset timer counter value. The capture function with free-counting capture mode and trigger-counting capture mode are configured by CAPSEL (TIMERx_EXTCTL[8]). The free-counting capture mode, external reset counter mode, trigger-counting capture mode are described as follows.

4.7.5.5.1. Free-Counting Capture Mode

The event capture function is used to load CNT (TIMERx_CNT[23:0]) value to CAPDAT (TIMERx_CAP[23:0]) value while edge transition detected on TMx_EXT (x= 0~2) pin. In this mode, CAPSEL (TIMERx_EXTCTL[8]) and CAPFUNCS (TIMERx_EXTCTL[4]) should be as 0 for select TMx_EXT transition is used to trigger event capture function.

User can enable or disable TMx_EXT pin de-bounce circuit by setting CAPDBEN (TIMERx_EXTCTL[6]). The transition frequency of TMx_EXT pin should be less than 1/3 AHB_CLK if

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TMx_EXT pin de-bounce disabled or less than 1/8 AHB_CLK if TMx_EXT pin de-bounce enabled to assure the capture function can be work normally, and user can also select edge transition detection of TMx_EXT pin by setting CAPEDGE (TIMERx_EXTCTL[2:1]).

In event capture mode, user does not consider what timer counting operation mode is selected, the capture event occurred only if edge transition on TMx_EXT pin is detected.

Users must consider the Timer will keep register TIMERx_CAP unchanged and drop the new capture value, if the CPU does not clear the CAPIF (TIMERx_EINTSTS[0]) status. The operation method is described in Figure 4-35.

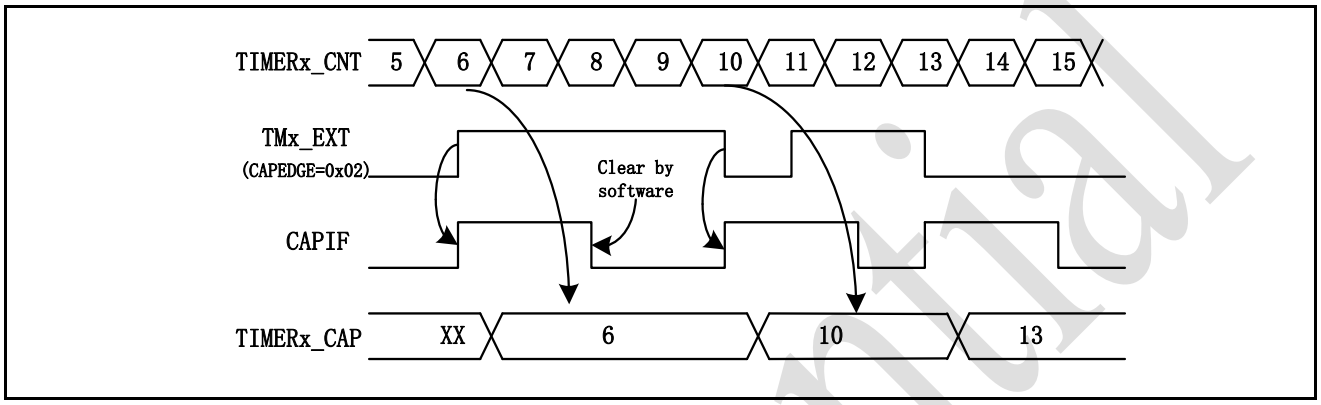

Figure 4-35 Free-Counting Capture Mode

4.7.5.5.2. External Reset Counter Mode

The timer controller also provides reset counter function to reset CNT (TIMERx_CNT[23:0]) value while edge transition detected on TMx_EXT (x= 0~2). In this mode, most the settings are the same as event capture mode except CAPFUNCS (TIMERx_EXTCTL[4]) should be as 1 for select TMx_EXT transition is used to trigger reset counter value. The operation method is also described in Figure 4-36.

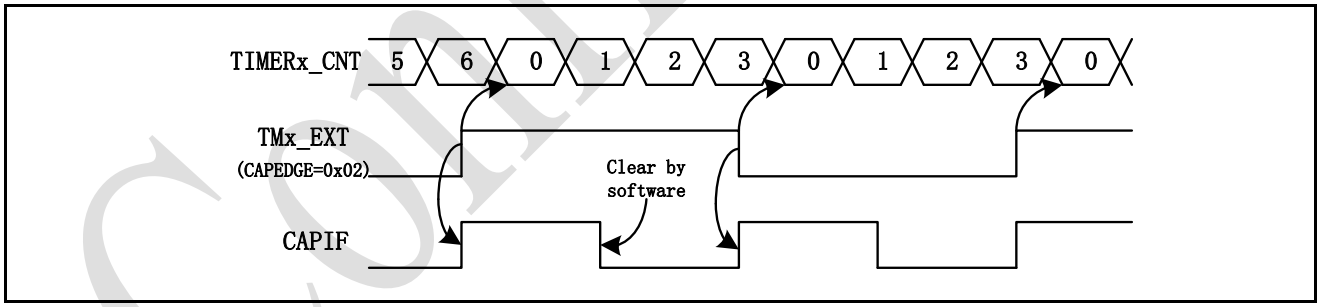

Figure 4-36 External Reset Counter Mode

4.7.5.5.3. Trigger-Counting Capture Mode

If CAPSEL (TIMERx_EXTCTL[8]) is set to 1, CAPEN (TIMERx_EXTCTL[3]) is set to 1 and CAPFUNCS (TIMERx_EXTCTL[4]) is set to 0, the CNT will be reset to 0 then captured into CAPDAT register when TMx_EXT (x= 0~2) pin trigger condition occurred. The TMx_EXT trigger edge can be chosen by CAPEDGE (TIMERx_EXTCTL[2:1]). The detailed operation method is described in

Table 4-8.

When TMx_EXT trigger occurred, CAPIF (TIMERx_EINTSTS[0]) is set to 1, and the interrupt

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signal is generated, then sent to NVIC to inform CPU if CAPIEN (TIMERx_EXTCTL[5]) is 1. And,

If TMx_EXT de-bounce is disabled, the TMx_EXT source operating frequency should be less than 1/3 AHB_CLK frequency. If TMx_EXT de-bounce is enabled, the TMx_EXT source operating frequency should be less than 1/8 AHB_CLK frequency. It also provides TMx_EXT enabled or disabled capture de-bounce function by CAPDBEN (TIMERx_EXTCTL[6]).

Table 4-8 Input Capture Mode Operation

Function	CAPSEL (TIMERx_EXTCTL[8])	CAPFUNCS (TIMERx_EXTCTL[4])	CAPEDGE (TIMERx_EXTCTL[2:1])	Operation Description
Free-counting Capture Mode	0	0	00	A transition(1 to 0) on TMx_EXT (x= 0~2) pin is detected. CNT is captured to CAPDAT.
	0	0	01	A transition(0 to 1) on TMx_EXT (x= 0~2) pin is detected. CNT is captured to CAPDAT.
	0	0	10	Either 1 to 0 or 0 to 1 transition on TMx_EXT (x= 0~2) pin is detected. CNT is captured to CAPDAT.
	0	0	11	Reserved
External Reset Counter Mode	0	1	00	A transition(1 to 0) on TMx_EXT (x= 0~2) pin is detected. CNT is reset to 0.
	0	1	01	A transition(0 to 1) on TMx_EXT (x= 0~2) pin is detected. CNT is reset to 0.
	0	1	10	Either 1 to 0 or 0 to 1 transition on TMx_EXT (x= 0~2) pin is detected. CNT is reset to 0.
	0	1	11	Reserved
Trigger-CountingCapture Mode	1	0	00	Falling Edge Trigger: The 1st 1 to 0 transition on TMx_EXT (x= 0~2) pin is detected to reset CNT as 0 and then starts counting, while the 2nd 1 to 0 transition stops counting.
	1	0	01	Rising Edge Trigger: The first transition(0 to 1) on TMx_EXT (x= 0~2) pin is detected to reset CNT as 0 and then starts counting, while the second transition(0 to 1) stops counting.
	1	0	10	Level Change Trigger: A transition(1 to 0) on TMx_EXT (x= 0~2) pin is detected to reset CNT as 0 and then starts counting, while 0 to 1 transition stops counting.
	1	0	11	Level Change Trigger: A transition(0 to 1) on TMx_EXT (x= 0~2) pin is detected to reset CNT as 0 and then starts counting, while 1 to 0 transition stops counting.

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4.7.6 TMR Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
TRM Base Address: **TMR0_BA = 0x4000_8000** **TMR1_BA = 0x4001_4000** **TMR2_BA = 0x4001_5000**				
TIMER0_CTL	TMR0_BA+0x00	R/W	Timer0 Control and Status Register	0x0000_0005
TIMER0_CMP	TMR0_BA+0x04	R/W	Timer0 Compare Register	0x0000_0000
TIMER0_INTSTS	TMR0_BA+0x08	R/W	Timer0 Interrupt Status Register	0x0000_0000
TIMER0_CNT	TMR0_BA+0x0C	R	Timer0 Data Register	0x0000_0000
TIMER0_CAP	TMR0_BA+0x10	R	Timer0 Capture Data Register	0x0000_0000
TIMER0_EXTCTL	TMR0_BA+0x14	R/W	Timer0 External Control Register	0x0000_0000
TIMER0_EINTSTS	TMR0_BA+0x18	R/W	Timer0 External Interrupt Status Register	0x0000_0000
TIMER1_CTL	TMR1_BA+0x00	R/W	Timer1 Control and Status Register	0x0000_0005
TIMER1_CMP	TMR1_BA+0x04	R/W	Timer1 Compare Register	0x0000_0000
TIMER1_INTSTS	TMR1_BA+0x08	R/W	Timer1 Interrupt Status Register	0x0000_0000
TIMER1_CNT	TMR1_BA+0x0C	R	Timer1 Data Register	0x0000_0000
TIMER1_CAP	TMR1_BA+0x10	R	Timer1 Capture Data Register	0x0000_0000
TIMER1_EXTCTL	TMR1_BA+0x14	R/W	Timer1 External Control Register	0x0000_0000
TIMER1_EINTSTS	TMR1_BA+0x18	R/W	Timer1 External Interrupt Status Register	0x0000_0000
TIMER2_CTL	TMR2_BA+0x00	R/W	Timer2 Control and Status Register	0x0000_0005
TIMER2_CMP	TMR2_BA+0x04	R/W	Timer2 Compare Register	0x0000_0000
TIMER2_INTSTS	TMR2_BA+0x08	R/W	Timer2 Interrupt Status Register	0x0000_0000
TIMER2_CNT	TMR2_BA+0x0C	R	Timer2 Data Register	0x0000_0000
TIMER2_CAP	TMR2_BA+0x10	R	Timer2 Capture Data Register	0x0000_0000
TIMER2_EXTCTL	TMR2_BA+0x14	R/W	Timer2 External Control Register	0x0000_0000
TIMER2_EINTSTS	TMR2_BA+0x18	R/W	Timer2 External Interrupt Status Register	0x0000_0000

4.7.7 TMR Register Description

4.7.7.1 Timer Control Register (TIMERx_CTL)

Register	Offset	R/W	Description	Reset Value
TIMER0_CTL	TMR0_BA+0x00	R/W	Timer0 Control and Status Register	0x0000_0005
TIMER1_CTL	TMR1_BA+0x00	R/W	Timer1 Control and Status Register	0x0000_0005
TIMER2_CTL	TMR2_BA+0x00	R/W	Timer2 Control and Status Register	0x0000_0005

Bits	Descriptions	
[31]	ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect) 0 = ICE debug mode acknowledgement effects TIMER counting. TIMER counter will be held while CPU is held by ICE.

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		1 = ICE debug mode acknowledgement disabled. TIMER counter will keep going no matter CPU is held by ICE or not. **Note**: This bit is write protected. Refer to the SYS_REGLCTL register.
[30]	CNTEN	Timer Counting Enable Bit 0 = Stops/Suspends counting. 1 = Starts counting. **Note1**: In stop status, and then setting CNTEN to 1 will enable the 24-bit up counter to keep counting from the last stop counting value. **Note2**: This bit is auto-cleared by hardware in one-shot mode (TIMERx_CTL[28:27] = 2'b00) when the timer interrupt flag TIF (TIMERx_INTSTS[0]) is generated.
[29]	INTEN	Timer Interrupt Enable Bit 0 = Timer interrupt disabled. 1 = Timer interrupt enabled. **Note**: If this bit is enabled, when the timer interrupt flag TIF is set to 1, the timer interrupt signal will be generated and inform CPU.
[28:27]	OPMODE	Timer Counting Mode Selection 00 = The timer controller is operated in one-shot mode. 01 = The timer controller is operated in periodic mode. 10 = The timer controller is operated in toggle-output mode. 11 = The timer controller is operated in continuous counting mode.
[26]	RSTCNT	Timer Counter Reset Setting this bit will reset the 24-bit up counter value CNT (TIMERx_CNT[23:0]) and also force CNTEN (TIMERx_CTL[30]) to 0 if ACTSTS (TIMERx_CTL[25]) is 1. 0 = No effect. 1 = Reset internal 8-bit prescale counter, 24-bit up counter value and CNTEN bit.
[25]	ACTSTS	Timer Active Status (Read Only) This bit indicates the 24-bit up counter status. 0 = 24-bit up counter is not active. 1 = 24-bit up counter is active.
[24]	EXTCNTEN	Event Counter Mode Enable Bit This bit is for external counting pin function enabled. 0 = Event counter mode disabled. 1 = Event counter mode enabled. **Note**: When timer is used as an event counter, this bit should be set to 1 and select AHB_CLK as timer clock source
[23]	WKEN	Wake-up Function Enable Bit If this bit is set to 1, while the timer interrupt flag TIF (TIMERx_INTSTS[0]) is 1 and INTEN (TIMERx_CTL[29]) is enabled, the timer interrupt signal will generate a wake-up trigger event to CPU. 0 = Wake-up function disabled if timer interrupt signal generated. 1 = Wake-up function enabled if timer interrupt signal generated.
[22:20]	Reserved	Reserved.
[19]	CAPSRC	Capture Pin Source Select Bit

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		0 = Capture function source is from TMx_EXT (x= 0~2) pin. 1 = Capture function source is from internal RCL.
[18:8]	Reserved	Reserved.
[7:0]	PSC	Prescale Counter Timer input clock or event source is divided by (PSC+1) before it is fed to the timer up counter. If this field is 0 (PSC = 0), then there is no scaling.

4.7.7.2 Timer Compare Register (TIMERx_CMP)

Register	Offset	R/W	Description	Reset Value
TIMER0_CMP	TMR0_BA+0x04	R/W	Timer0 Compare Register	0x0000_0000
TIMER1_CMP	TMR1_BA+0x04	R/W	Timer1 Compare Register	0x0000_0000
TIMER2_CMP	TMR2_BA+0x04	R/W	Timer2 Compare Register	0x0000_0000

Bits	Descriptions	
[31:24]	Reserved	Reserved.
[23:0]	CMPDAT	Timer Compared Value CMPDAT is a 24-bit compared value register. When the internal 24-bit up counter value is equal to CMPDAT value, the TIF (TIMERx_INTSTS[0] Timer Interrupt Flag) will set to . Time-out period = (Period of timer clock input) * (8-bit PSC + 1) * (24-bit CMPDAT). **Note1**: Never write 0x0 or 0x1 in CMPDAT field, or the core will run into unknown state. **Note2**: When timer is operating at continuous counting mode, the 24-bit up counter will keep counting continuously even if user writes a new value into CMPDAT field. But if timer is operating at other modes, the 24-bit up counter will restart counting from 0 and using newest CMPDAT value to be the timer compared value while user writes a new value into the CMPDAT field.

4.7.7.3 Timer Interrupt Status Register (TIMERx_INTSTS)

Register	Offset	R/W	Description	Reset Value
TIMER0_INTSTS	TMR0_BA+0x08	R/W	Timer0 Interrupt Status Register	0x0000_0000
TIMER1_INTSTS	TMR1_BA+0x08	R/W	Timer1 Interrupt Status Register	0x0000_0000
TIMER2_INTSTS	TMR2_BA+0x08	R/W	Timer2 Interrupt Status Register	0x0000_0000

Bits	Descriptions	
[31:3]	Reserved	Reserved.
[2]	TF	Timer Flag This bit indicates the interrupt flag status of timer while 24-bit timer up counter CNT (TIMERx_CNT[23:0]) value reaches to CMPDAT (TIMERx_CMP[23:0]) value. 0 = No effect. 1 = CNT value matches the CMPDAT value.

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		Note: This bit is cleared by writing 1 to it.
[1]	TWKF	Timer Wake-up Flag This bit indicates the interrupt wake-up flag status of timer. 0 = Timer does not cause CPU wake-up. 1 = CPU wake-up from idle or power-down mode if timer time-out interrupt signal generated. **Note**: This bit is cleared by writing 1 to it.
[0]	TIF	Timer Interrupt Flag This bit indicates the interrupt flag status of Timer while 24-bit timer up counter CNT (TIMERx_CNT[23:0]) value reaches to CMPDAT (TIMERx_CMP[23:0]) value. 0 = No effect. 1 = CNT value matches the CMPDAT value. **Note**: This bit is cleared by writing 1 to it.

4.7.7.4 Timer Data Register (TIMERx_CNT)

Register	Offset	R/W	Description	Reset Value
TIMER0_CNT	TMR0_BA+0x0C	R	Timer0 Data Register	0x0000_0000
TIMER1_CNT	TMR1_BA+0x0C	R	Timer1 Data Register	0x0000_0000
TIMER2_CNT	TMR2_BA+0x0C	R	Timer2 Data Register	0x0000_0000

Bits	Descriptions	
[31:24]	Reserved	Reserved.
[23:0]	CNT	Timer Data Register This field can be reflected the internal 24-bit timer counter value or external event input counter value from TMx (x=0~2) pin. If EXTCNTEN (TIMERx_CTL[24]) is 0, user can read CNT value for getting current 24- bit counter value. If EXTCNTEN (TIMERx_CTL[24]) is 1, user can read CNT value for getting current 24- bit event input counter value.

4.7.7.5 Timer Capture Data Register (TIMERx_CAP)

Register	Offset	R/W	Description	Reset Value
TIMER0_CAP	TMR0_BA+0x10	R	Timer0 Capture Data Register	0x0000_0000
TIMER1_CAP	TMR1_BA+0x10	R	Timer1 Capture Data Register	0x0000_0000
TIMER2_CAP	TMR2_BA+0x10	R	Timer2 Capture Data Register	0x0000_0000

Bits	Descriptions	
[31:24]	Reserved	Reserved.
[23:0]	CAPDAT	Timer Capture Data Register When CAPEN (TIMERx_EXTCTL[3]) bit is set, CAPFUNCS (TIMERx_EXTCTL[4]) bit is 0, and a transition on TMx_EXT pin matched the CAPEDGE (TIMERx_EXTCTL[2:1]) setting, CAPIF (TIMERx_EINTSTS[0]) will set to 1 and the

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		current timer counter value CNT (TIMERx_CNT[23:0]) will be auto-loaded into this CAPDAT field.

4.7.7.6 Timer External Control Register (TIMERx_EXTCTL)

Register	Offset	R/W	Description	Reset Value
TIMER0_EXTCTL	TMR0_BA+0x14	R/W	Timer0 External Control Register	0x0000_0000
TIMER1_EXTCTL	TMR1_BA+0x14	R/W	Timer1 External Control Register	0x0000_0000
TIMER2_EXTCTL	TMR2_BA+0x14	R/W	Timer2 External Control Register	0x0000_0000

Bits	Descriptions	
[31:9]	Reserved	Reserved.
[8]	CAPSEL	Capture Mode Select Bit 0 = Timer counter reset function or free-counting mode of timer capture function. 1 = Trigger-counting mode of timer capture function.
[7]	CNTDBEN	Timer Counter Pin De-bounce Enable Bit 0 = TMx (x= 0~2) pin de-bounce disabled. 1 = TMx (x= 0~2) pin de-bounce enabled. **Note**: If this bit is enabled, the edge detection of TMx pin is detected with de-bounce circuit.
[6]	CAPDBEN	Timer External Capture Pin De-bounce Enable Bit 0 = TMx_EXT (x= 0~2) pin de-bounce disabled. 1 = TMx_EXT (x= 0~2) pin de-bounce enabled. **Note1**: If this bit is enabled, the edge detection of TMx_EXT pin is detected with de-bounce circuit.
[5]	CAPIEN	Timer External Capture Interrupt Enable Bit 0 = TMx_EXT (x= 0~2) pin detection Interrupt disabled. 1 = TMx_EXT (x= 0~2) pin detection Interrupt enabled. **Note**: CAPIEN is used to enable timer external interrupt. If CAPIEN enabled, timer will generate an interrupt when CAPIF (TIMERx_EINTSTS[0]) is 1. For example, while CAPIEN = 1, CAPEN = 1, and CAPEDGE = 00, an 1 to 0 transition on the TMx_EXT pin will cause the CAPIF to be set then the interrupt signal is generated and sent to NVIC to inform CPU.
[4]	CAPFUNCS	Capture Function Select Bit 0 = External Capture Mode enabled. 1 = External Reset Mode enabled. **Note1**: When CAPFUNCS is 0, transition on TMx_EXT (x= 0~2) pin is used to save the 24-bit timer counter value to CAPDAT register. **Note2**: When CAPFUNCS is 1, transition on TMx_EXT (x= 0~2) pin is used to reset the 24-bit timer counter value.
[3]	CAPEN	Timer External Capture Pin Enable Bit This bit enables the TMx_EXT pin. 0 = TMx_EXT (x= 0~2) pin Disabled. 1 = TMx_EXT (x= 0~2) pin Enabled.

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[2:1]	CAPEDGE	Timer External Capture Pin Edge Detection 00 = A falling edge on TMx_EXT (x= 0~2) pin will be detected. 01 = A rising edge on TMx_EXT (x= 0~2) pin will be detected. 10 = Either rising or falling edge on TMx_EXT (x= 0~2) pin will be detected. 11 = Reserved.
[0]	CNTPHASE	Timer External Count Phase This bit indicates the detection phase of external counting pin TMx (x= 0~2). 0 = A falling edge of external counting pin will be counted. 1 = A rising edge of external counting pin will be counted.

4.7.7.7 Timer External Interrupt Status Register (TIMERx_EINTSTS)

Register	Offset	R/W	Description	Reset Value
TIMER0_EINTSTS	TMR0_BA+0x18	R/W	Timer0 External Interrupt Status Register	0x0000_0000
TIMER1_EINTSTS	TMR1_BA+0x18	R/W	Timer1 External Interrupt Status Register	0x0000_0000
TIMER2_EINTSTS	TMR2_BA+0x18	R/W	Timer2 External Interrupt Status Register	0x0000_0000

Bits	Descriptions	
[31:2]	Reserved	Reserved.
[1]	CAPF	Timer External Capture Flag This bit indicates the timer external capture interrupt flag status. 0 = TMx_EXT (x= 0~2) pin interrupt does not occur. 1 = TMx_EXT (x= 0~2) pin interrupt occurs. **Note1**: This bit is cleared by writing 1 to it. **Note2**: When CAPEN (TIMERx_EXTCTL[3]) bit is set, CAPFUNCS (TIMERx_EXTCTL[4]) bit is 0, and a transition on TMx_EXT (x= 0~2) pin matches the CAPEDGE (TIMERx_EXTCTL[2:1]) setting, this bit will be set to 1 by hardware. **Note3**: There is a new incoming capture event detected before CPU clearing the CAPIF status. If the above condition occurred, the Timer will keep register TIMERx_CAP unchanged and drop the new capture value.
[0]	CAPIF	Timer External Capture Interrupt Flag This bit indicates the timer external capture interrupt flag status. 0 = TMx_EXT (x= 0~2) pin interrupt does not occur. 1 = TMx_EXT (x= 0~2) pin interrupt occurs. **Note1**: This bit is cleared by writing 1 to it. **Note2**: When CAPEN (TIMERx_EXTCTL[3]) bit is set, CAPFUNCS (TIMERx_EXTCTL[4]) bit is 0, and a transition on TMx_EXT (x= 0~2) pin matches the CAPEDGE (TIMERx_EXTCTL[2:1]) setting, this bit will be set to 1 by hardware. **Note3**: There is a new incoming capture event detected before CPU clearing the CAPIF status. If the above condition occurred, the Timer will keep register TIMERx_CAP unchanged and drop the new capture value.

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4.8 Enhanced PWM Generator (PWM)

4.8.1 Overview

The PAN2025 series have a built-in PWM unit (PWM0) which is specially designed for motor driving control applications. The PWM0 supports eight PWM generators which can be configured as eight independent PWM outputs, PWM0_CH0~PWM0_CH7, or as four complementary PWM pairs, (PWM0_CH0, PWM0_CH1), (PWM0_CH2, PWM0_CH3), (PWM0_CH4, PWM0_CH5) and (PWM0_CH6, PWM0_CH7) with four programmable dead-time generators, or as four synchronous PWM pairs, with each pin in a pair in-phase – (PWM0_CH0, PWM0_CH1), (PWM0_CH2, PWM0_CH3), (PWM0_CH4, PWM0_CH5) and (PWM0_CH6, PWM0_CH7).

Every complementary PWM pairs share one 8-bit prescaler. There are eight clock dividers providing five divided frequencies (1, 1/2, 1/4, 1/8, 1/16) for each channel. Each PWM output has independent 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The eight PWM generators provide sixteen independent PWM interrupt flags which are set by hardware when the corresponding PWM period counter comparison matched period and duty. Each PWM interrupt source with its corresponding enable bit can request PWM interrupt. The PWM generators can be configured as Auto-reload mode to output PWM waveform continuously.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit down counter/comparator at the end of current period. The double buffering feature avoids glitch at PWM outputs.

Besides PWM, Motor controlling also need Timer and ADC to work together. In order to control motor more precisely, we provide some registers that not only configure PWM but also Timer and ADC, by doing so, it can save more CPU time and control motor with ease especially in BLDC.

4.8.2 Features

- Eight independent 16-bit PWM duty control units with maximum eight port pins:
  - Eight independent PWM outputs – PWM0_CH0, PWM0_CH1, PWM0_CH2, PWM0_CH3, PWM0_CH4, PWM0_CH5, PWM0_CH6, and PWM0_CH7
  - Four complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-time insertion – (PWM0_CH0, PWM0_CH1), (PWM0_CH2, PWM0_CH3), (PWM0_CH4, PWM0_CH5) and (PWM0_CH6, PWM0_CH7)
  - Four synchronous PWM pairs, with each pin in a pair in-phase – (PWM0_CH0, PWM0_CH1), (PWM0_CH2, PWM0_CH3), (PWM0_CH4, PWM0_CH5)and (PWM0_CH6, PWM0_CH7)
- Group control bit – PWM0_CH2, PWM0_CH4 and PWM0_CH6 are synchronized with PWM0_CH0, PWM0_CH3, PWM0_CH5 and PWM0_CH7 are synchronized with PWM0_CH1
- Auto-reload mode PWM
- Up to 16-bit resolution
- Supports edge-aligned, center-aligned and precise center-aligned mode
- Supports asymmetric PWM generating in center-aligned and precise center-aligned mode
- Supports center loading in center-aligned and precise center-aligned mode
- Programmable dead-time insertion between complementary paired PWMs
- Each pin of PWM0_CH0 to PWM0_CH7 has independent polarity setting control
- The PWM signals before polarity control stage are defined in the view of low logic. The PWM ports is active high or active low are controlled by polarity control register

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- Supports mask aligned function
- Supports independently rising CMP matching, PERIOD matching, falling CMP matching (in Center-aligned type), PERIOD matching to trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change in BLDC application
- Provides interrupt accumulation function

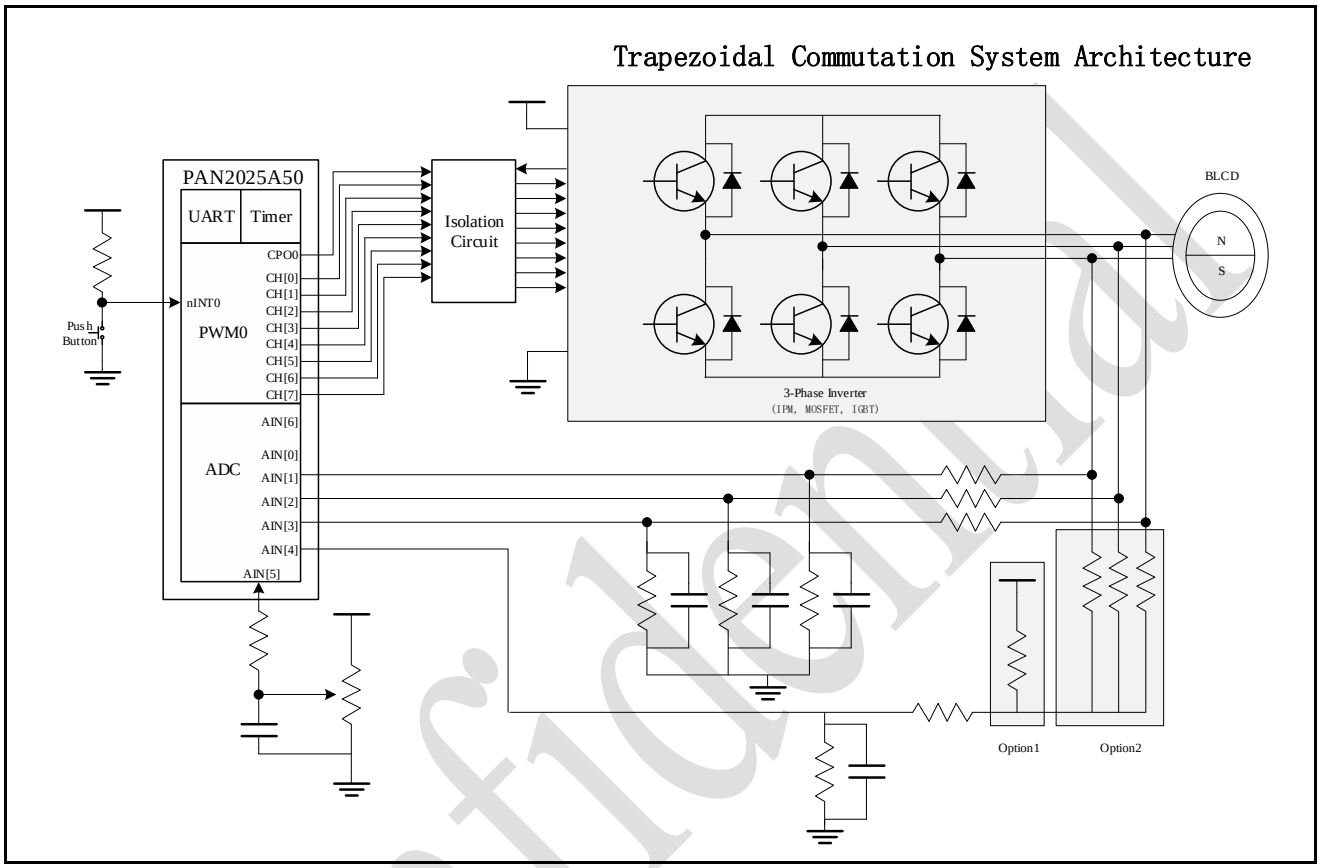

Figure 4-37 Application Circuit Diagram

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4.8.3 Block Diagram

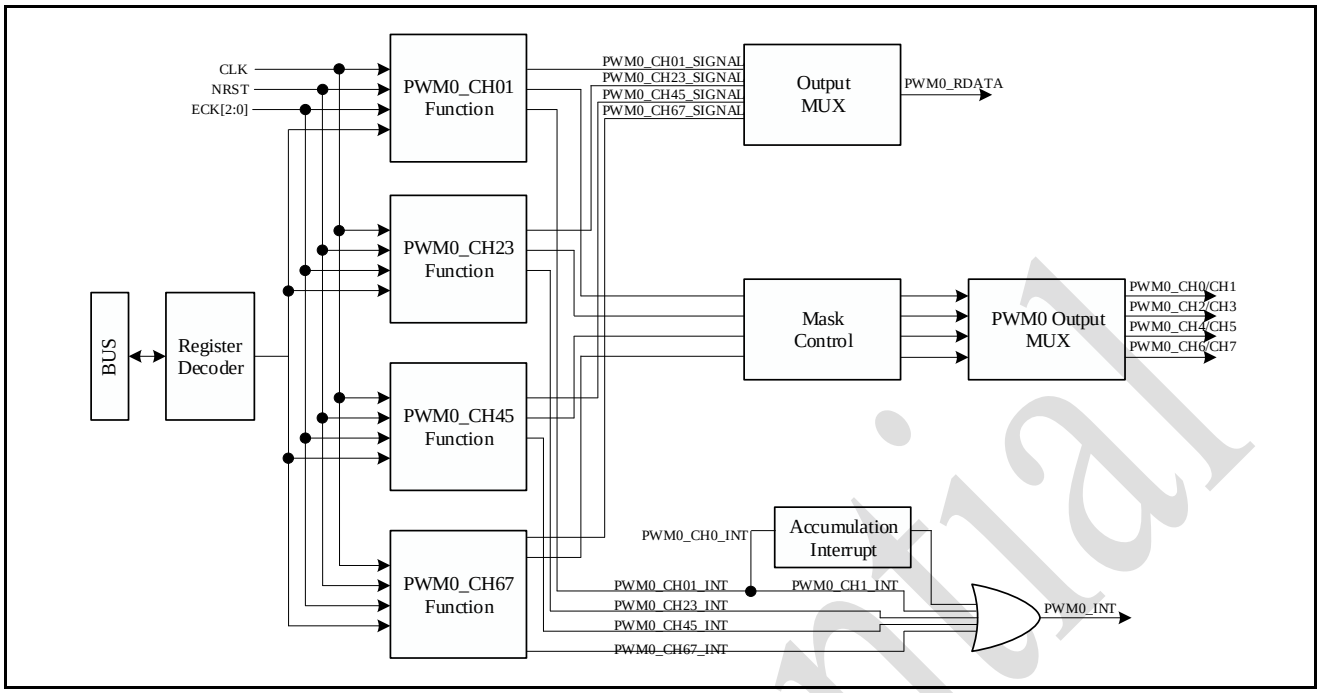

Figure 4-38 PWM Block Diagram

Figure 4-39 shows the architecture of PWM0 in pair (e.g. PWM Counter 0/1 are in one pair and PWM Counter 2/3 are in another one, and so on).

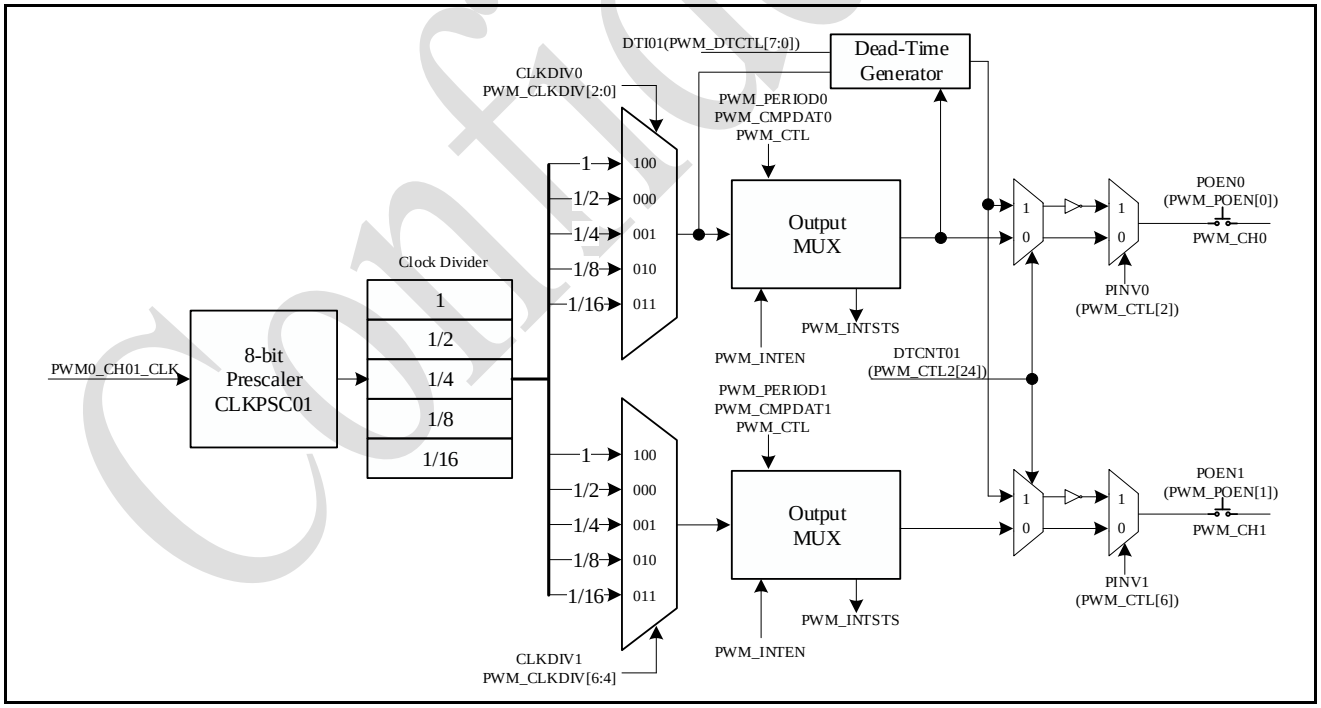

Figure 4-39 PWM Generator 0 Architecture Diagram

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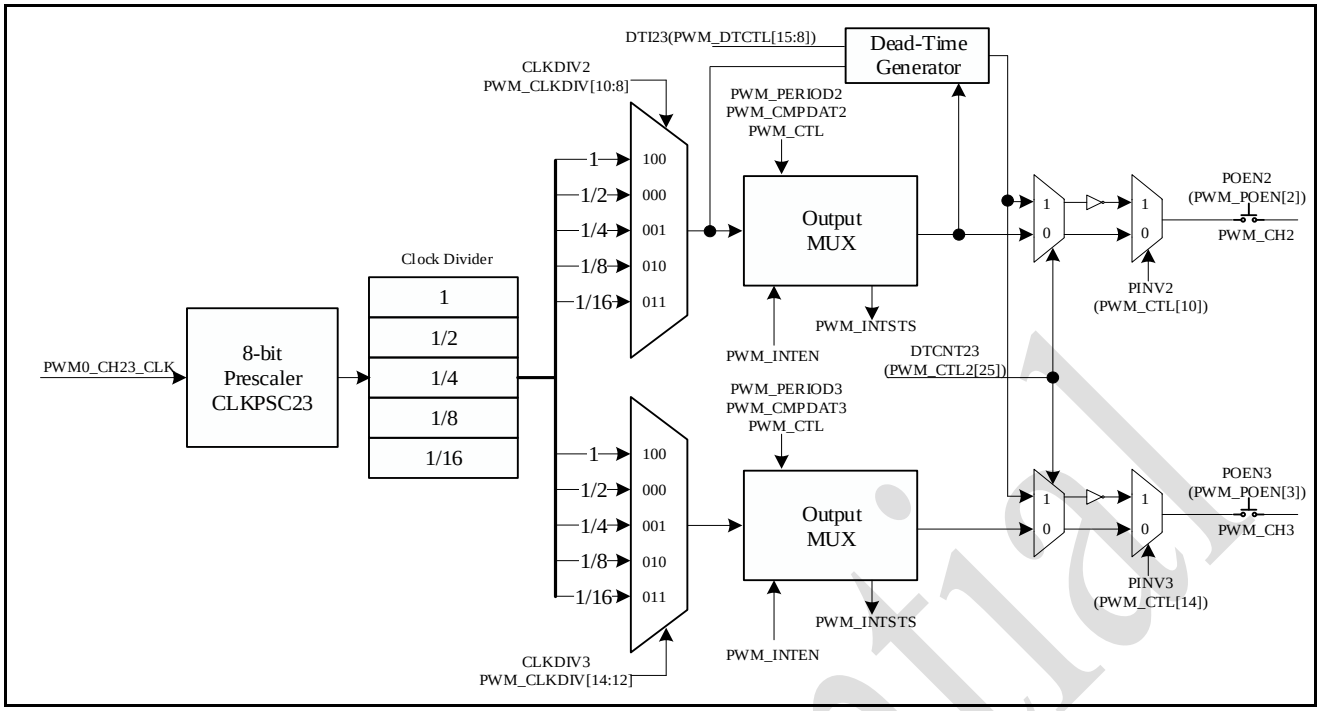

Figure 4-40 PWM Generator 2 Architecture Diagram

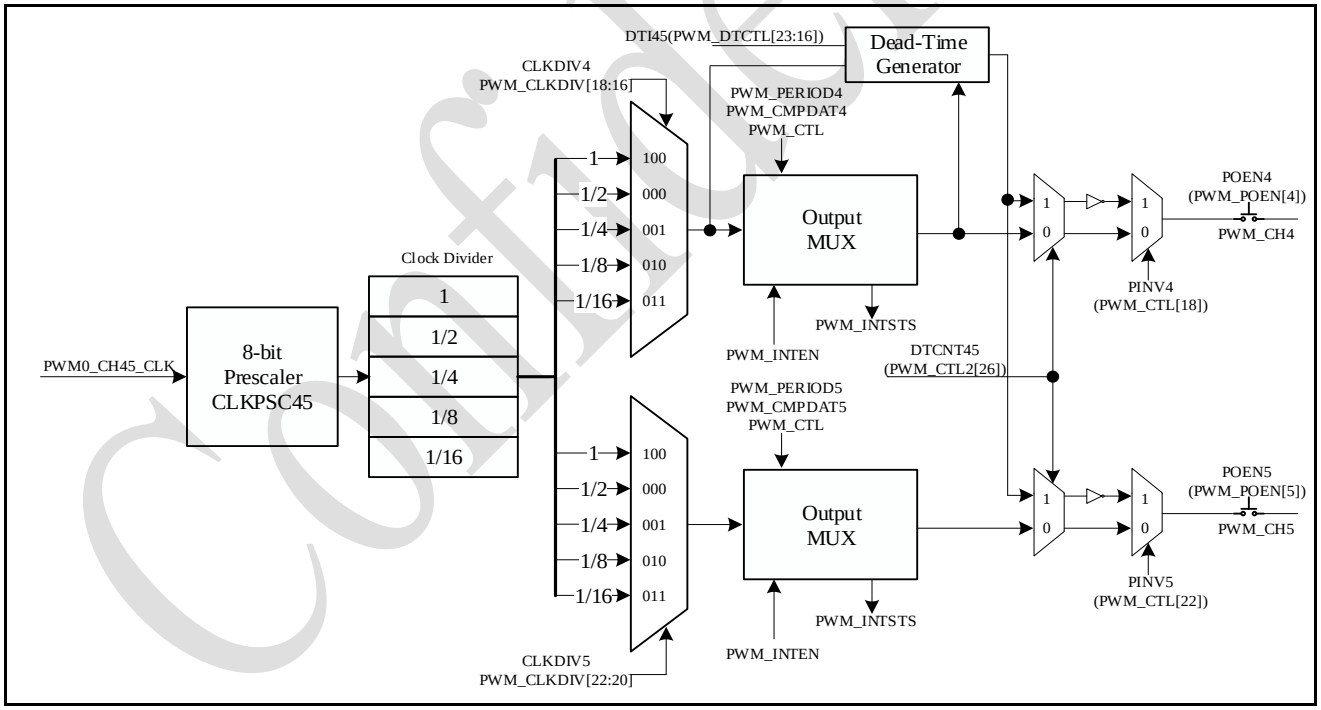

Figure 4-41 PWM Generator 4 Architecture Diagram

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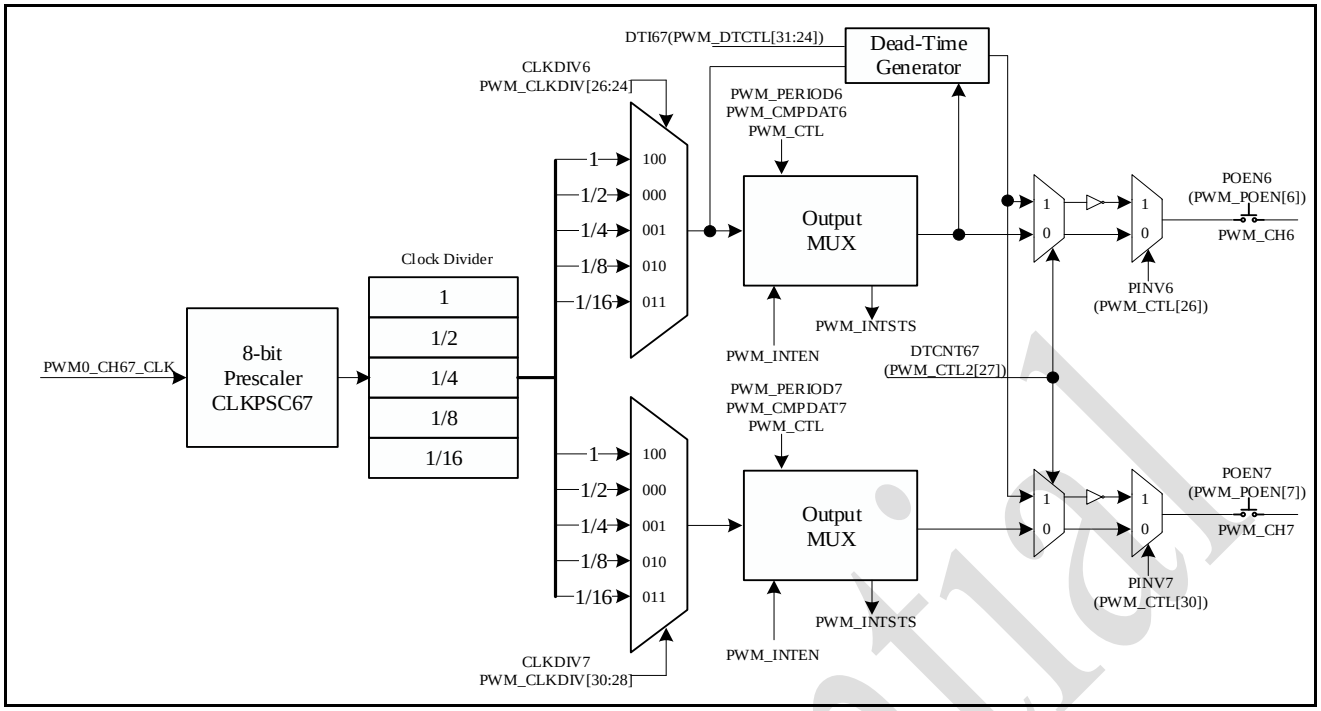

Figure 4-42 PWM Generator 6 Architecture Diagram

4.8.4 Basic Configuration

The PWM0 pin functions are configured in SYS_P0_MFP, SYS_P1_MFP, SYS_P2_MFP and SYS_P5_MFP registers. The PWM0 clock can be enabled by CLK_APB1_EN[7:4].

4.8.5 Functional Description

4.8.5.1 PWM Counter Operation

This device supports three operation types: Edge-aligned, Center-aligned and Precise center-aligned type.

Following equations show the formula for period and duty for each PWM counter operation type:

Edge-aligned (Down counter):

Duty ratio = (CMP + 1) / (PERIOD + 1)

*Duty = (CMP + 1) * (clock period)*

*Period = (PERIOD + 1) * (clock period)*

Center-aligned (Up and Down Counter):

Duty ratio = (PERIOD - CMP) / (PERIOD + 1)

*Duty = (PERIOD - CMP) * 2 * (clock period)*

*Period = (PERIOD + 1) * 2 * (clock period)*

Precise Center-aligned (Up and Down Counter):

*Duty ratio = (PERIOD - (CMP + 1) * 2) / PERIOD*

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*Duty = (PERIOD - (CMP + 1) * 2) * (clock period)*

*Period = (PERIOD) * (clock period)*

4.8.5.1.1. Edge-aligned PWM (Down-counter)

In Edge-aligned PWM Output type, the 16-bit PWM counter will start counting-down from PERIODn to match with the value of the duty cycle CMPn (old); when this happens it will toggle the PWM0_CHn output to high and set up CMPDIF compare down match interrupt flag. The counter will continue counting-down to zero; at this moment, it toggles the PWM0_CHn output to low and CMPn (new) and PERIODn (new) are updated with CNTMODEn=1 and set PIF period interrupt flag.

Figure 4-43, Figure 4-44 and Figure 4-45 show the Edge-aligned PWM timing and operation flow.

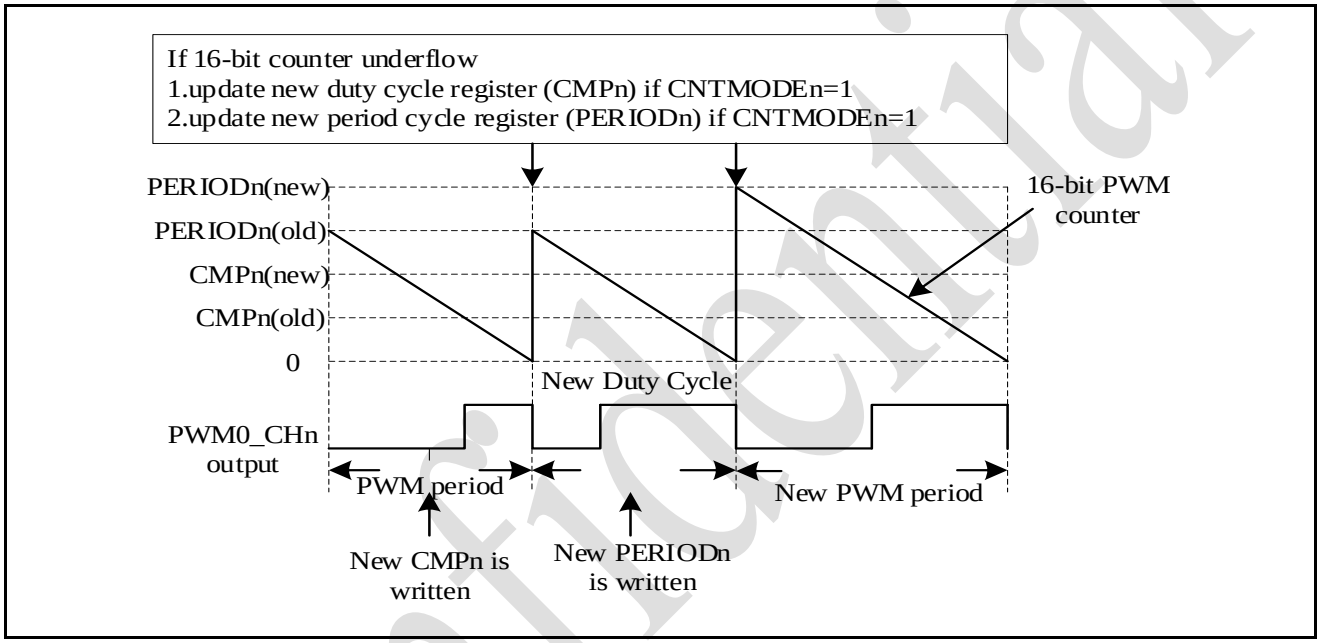

Figure 4-43 Edge-aligned Type PWM

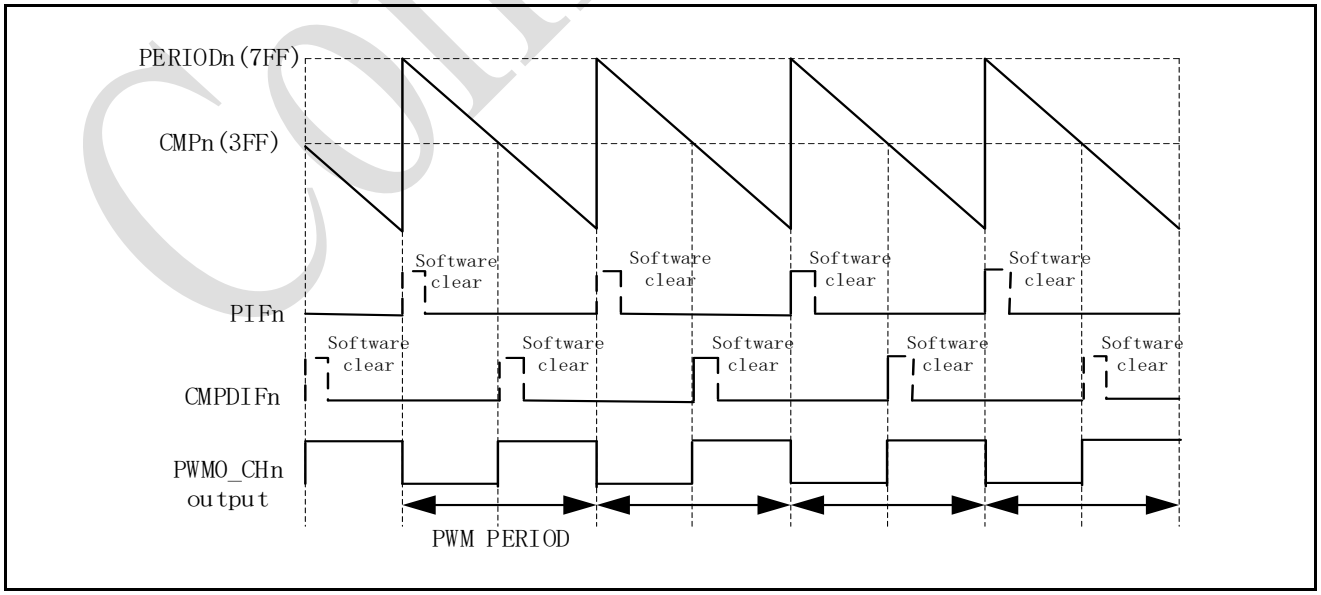

Figure 4-44 PWM Edge-aligned Waveform Timing Diagram

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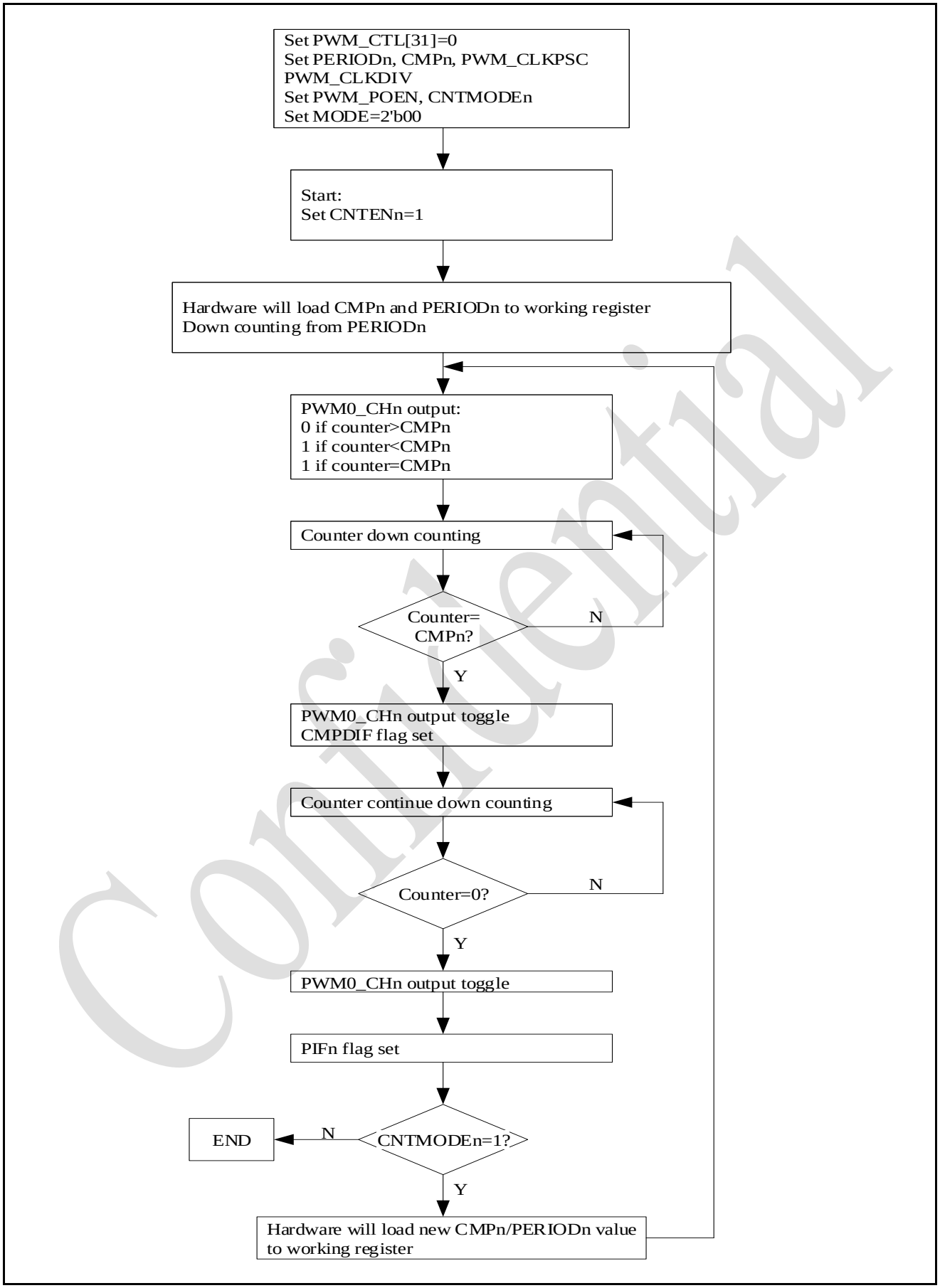

Figure 4-45 Edge-aligned Flow Diagram

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The PWM period and duty control are decided by PWM down-counter period register (PERIODn) and PWM comparator register (CMPn). The PWM counter timing operation is shown in Figure 4-47. The pulse width modulation follows the formula below and the legend of PWM counter Comparator is shown in Figure 4-46. Note that the corresponding GPIO pins must be configured as PWM function (enable PWM_POEN) for the corresponding PWM channel.

*PWM frequency = APB1_CLK / ((CLKPSCnm + 1) * (clock divider)) / (PERIOD + 1)*; where nm, could be 01, 23, 45 or 67 depending on the selected PWM channel

Duty ratio = (CMP + 1) / (PERIOD + 1)

PERIOD =0: PWM output is always low

When PERIOD!=0, PWM output is as follow:

CMP ≥ PERIOD: PWM output is always high

CMP < PERIOD: PWM low width = (PERIOD - CMP) unit[1]; PWM high width = (CMP+1) unit

CMP = 0: PWM is always low

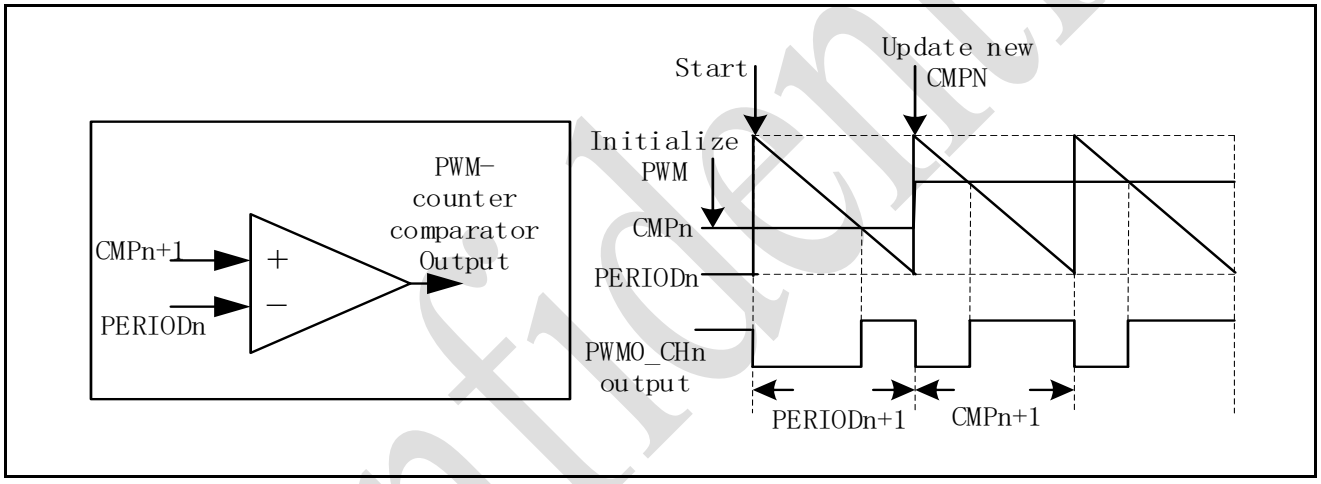

Figure 4-46 Legend of Internal Comparator Output of PWM Counter

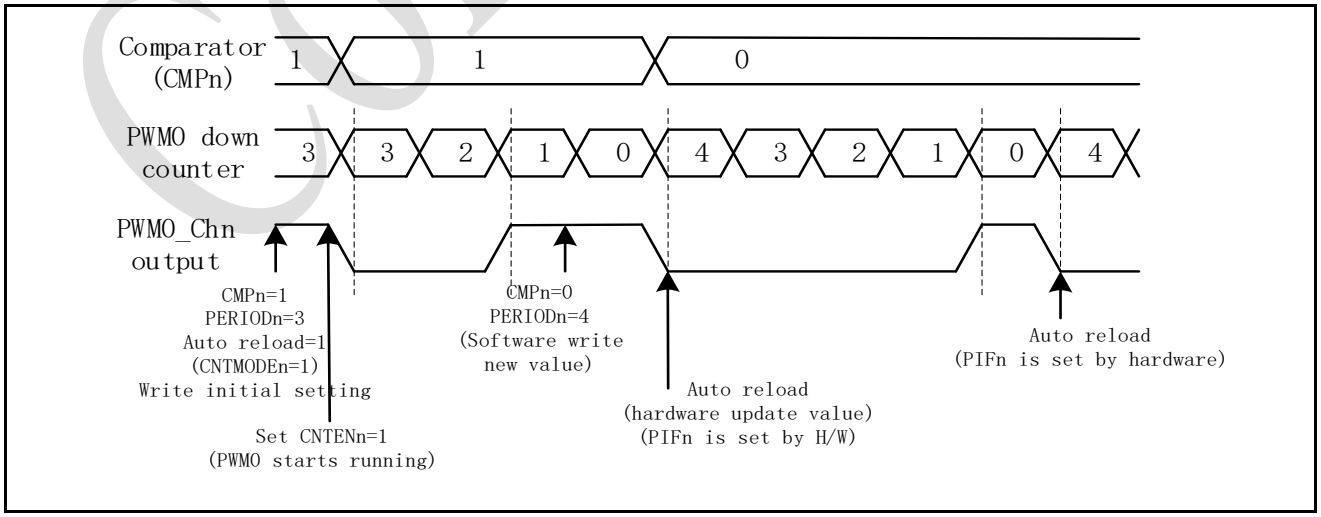

Figure 4-47 PWM Counter Operation Timing

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4.8.5.1.2. Center-Aligned PWM (up/down counter)

The center-aligned PWM signals are produced by the module when the PWM time base is configured in an Up/Down Counting type. The PWM counter will start counting-up from 0 to match the value of CMPn (old); this will cause the toggling of the PWM0_CHn generator output to high and set up CMPUIF compare up match interrupt flag. The counter will continue counting to match with the PERIODn (old). Upon reaching this state counter is configured automatically to down counting and set up PIF period interrupt flag, when PWM counter matches the CMPn (old) value again the PWM0_CHn generator output toggles to low and set up CMPDIF compare down match interrupt flag. Once the PWM counter underflows it will update the PWM period register PERIODn (new) and duty cycle register CMPn (new) with CNTMODEn = 1.

In Center-aligned type, the PWM period interrupt can also be requested at down-counter underflow if PINTTYPE (PWM_CTL2[17]) =0, i.e. at start (end) of each PWM cycle or at up-counter matching with PERIODn if PINTTYPE (PWM_CTL2[17]) =1, i.e. at center point of PWM cycle.

*PWM frequency = APB1_CLK / ((CLKPSCnm + 1) * (clock divider)) / (PERIOD + 1)*; where nm, could be 01, 23, 45 or 67 depending on the selected PWM channel

Duty ratio = (PERIOD - CMP) / (PERIOD + 1)

PERIOD =0: PWM output is always low

When PERIOD!=0, PWM output is as follow:

CMP ≥ PERIOD: PWM output is always low

CMP < PERIOD: PWM low width = (CMP + 1) * 2 units; PWM high width= (PERIOD - CMP) * 2 units[1]

CMP = 0: PWM is always high

Note: 1. Unit = one PWM clock cycle.

Figure 4-48, Figure 4-49, Figure 4-50 and Figure 4-51 show the Center-aligned PWM timing and operation flow.

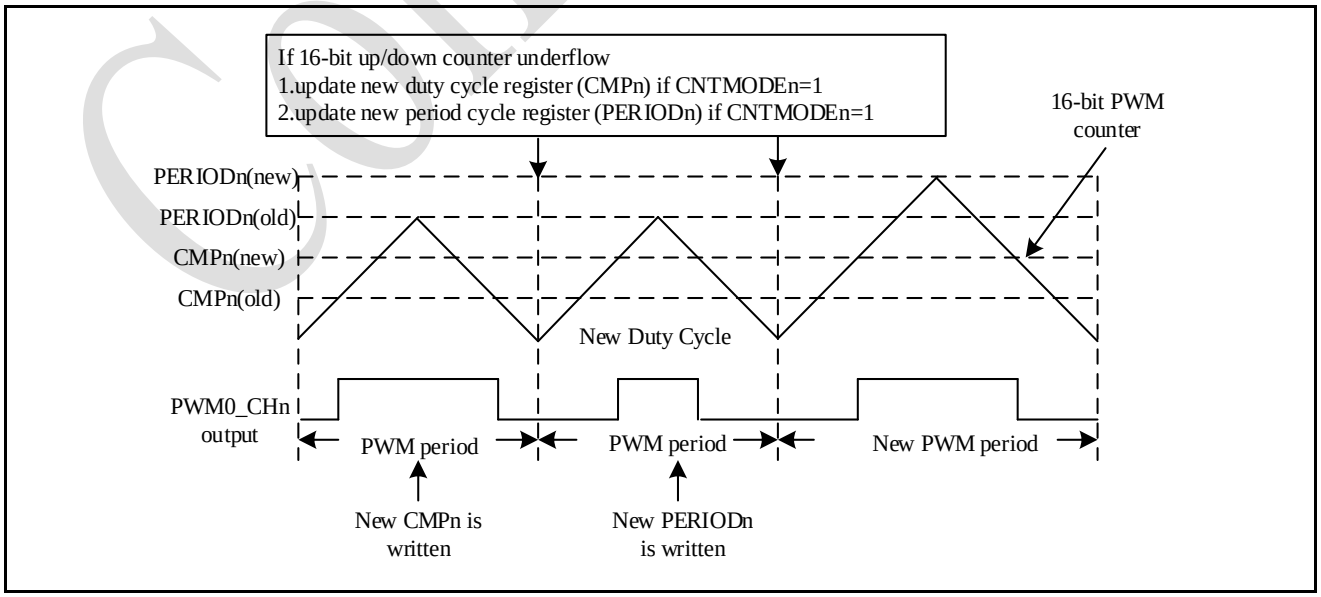

Figure 4-48 Center-aligned Type PWM

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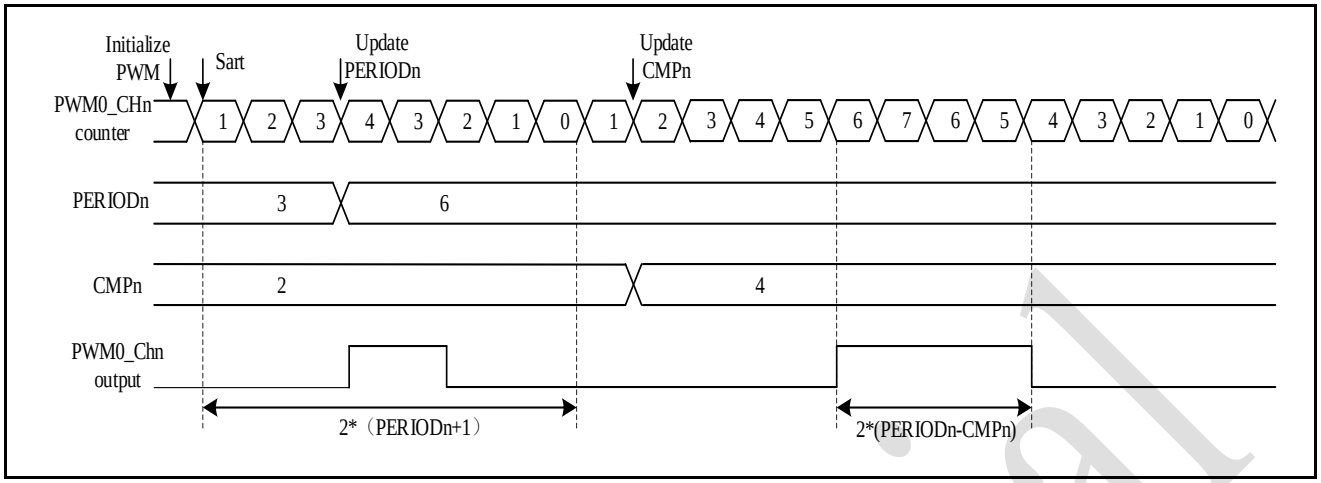

Figure 4-49 Center-aligned Type Operation Timing

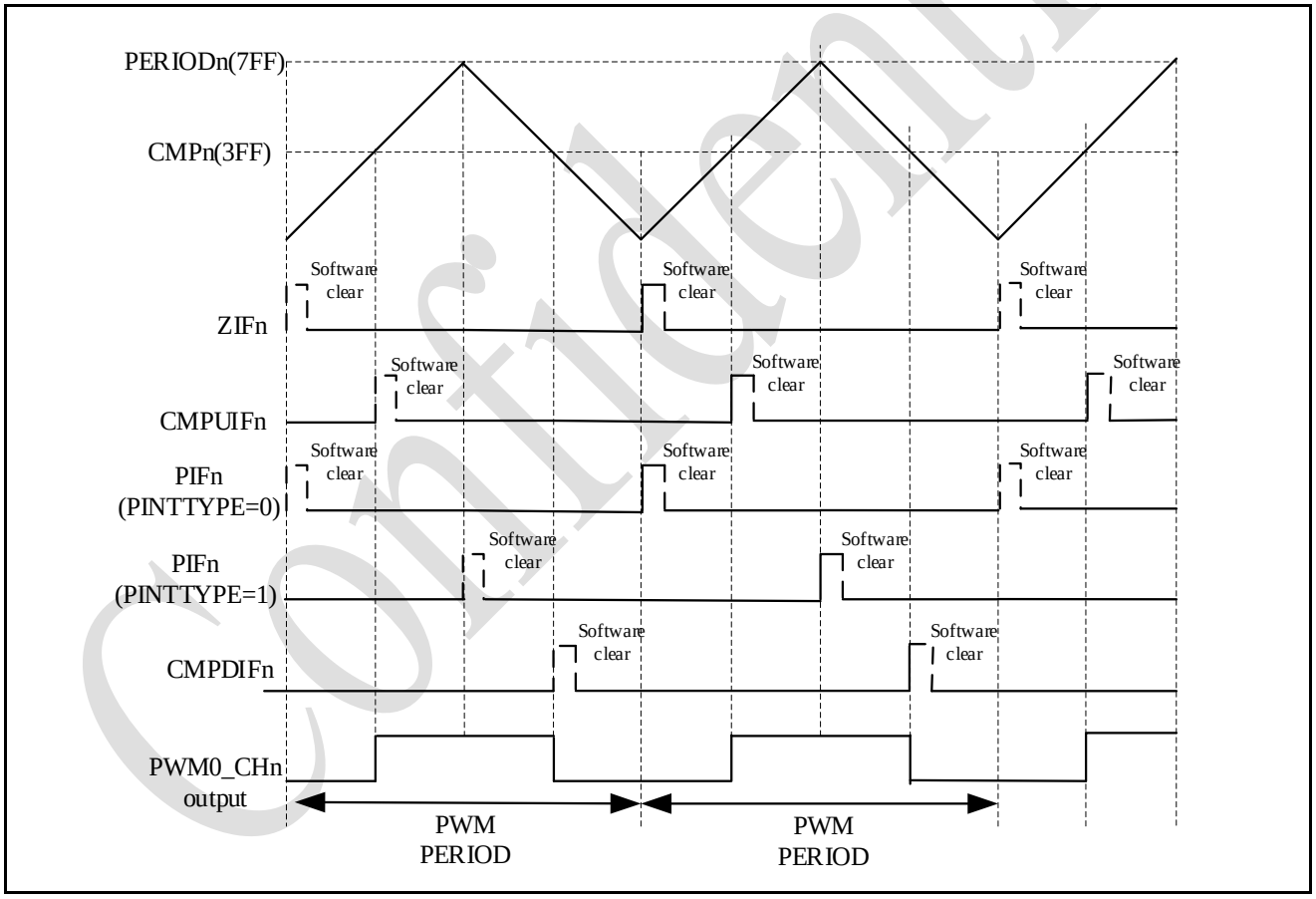

Figure 4-50 PWM Center-aligned Waveform Timing Diagram

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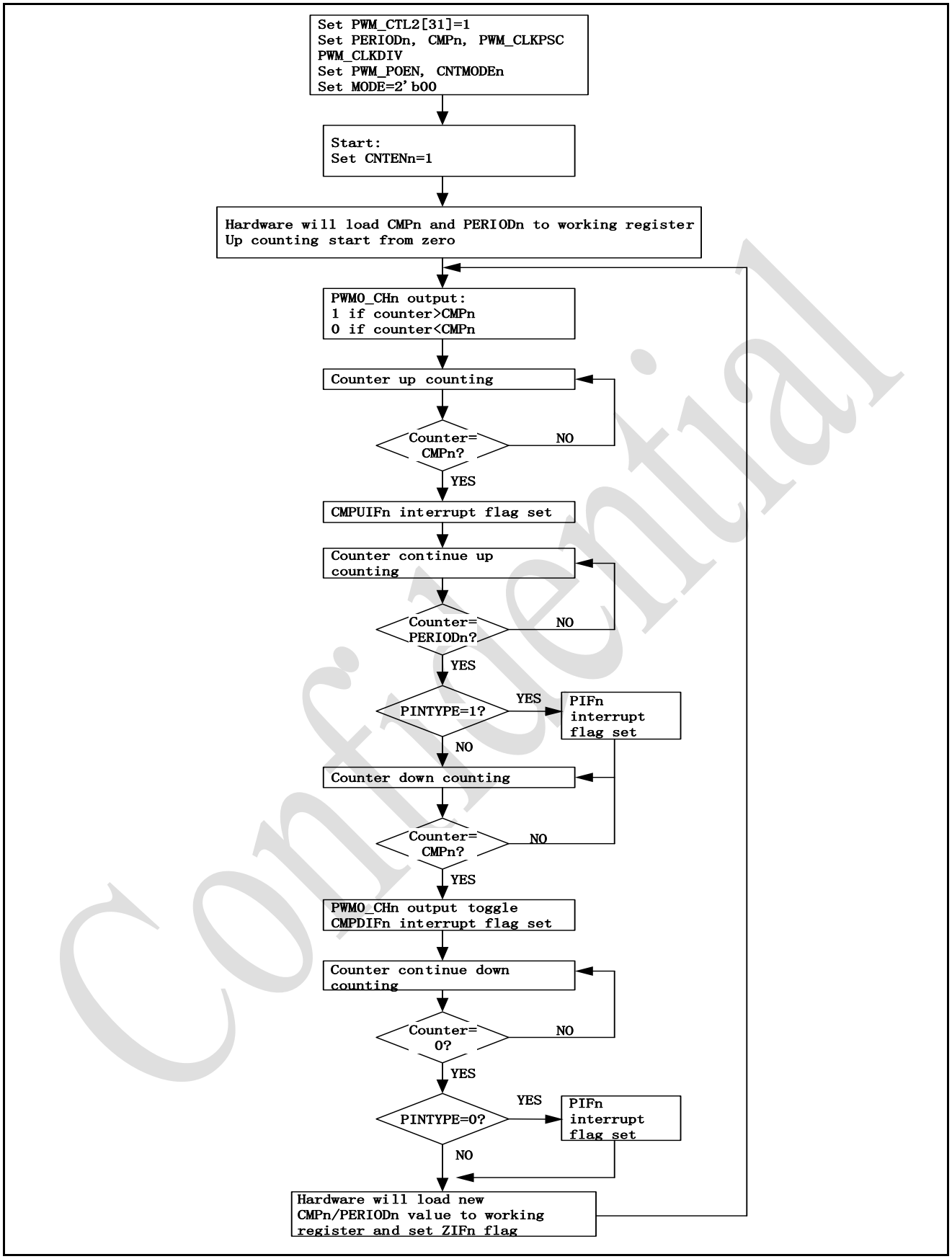

Figure 4-51 Center-aligned Flow Diagram

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4.8.5.1.3. Precise Center-Aligned PWM (Up/Down Counter)

The precise center-aligned PWM signals are produced by the module when the PWM time base is configured in an Up/Down Counting type and enable PCAEN (PWM_PCACTL[0]). The PWM counter will start counting-up from 0 to match the value of CMPn (old); this will cause the toggling of the PWM0_CHn output to high. The counter will continue counting to match with the half of the PERIODn (old). If PERIODn is an odd number, the counter will continue counting to match the integer of lower boundary of the half of the PERIODn (old) and keep the counter value for two clock cycles. Upon reaching this state counter is configured automatically to down counting, when PWM counter matches the CMPn (old) value again the PWM0_CHn output toggles to low. Once the PWM counter underflows it will update the PWM period register PERIODn (new) and duty cycle register CMPn (new) with CNTMODEn = 1.

In Precise Center-aligned type, the PWM period interrupt can also be requested at down-counter underflow if PINTTYPE (PWM_CTL2[17]) =0, i.e. at start (end) of each PWM cycle or at up-counter matching with PERIODn if PINTTYPE (PWM_CTL2[17]) =1, i.e. at center point of PWM cycle.

*PWM frequency = APB1_CLK / ((CLKPSCnm + 1) * (clock divider)) / (PERIOD + 1)*; where nm, could be 01, 23, 45 or 67 depending on the selected PWM channel

*Duty ratio = (PERIOD – (CMP+1)*2) / PERIOD*

PERIOD =0: PWM output is always low

When PERIOD!=0, PWM output is as follow:

CMP ≥ PERIOD: PWM output is always low

CMP < PERIOD: PWM low width = (CMP + 1) * 2 units; PWM high width= (PERIOD – (CMP+1)*2) units[1]

CMP = 0: PWM is always high

Note: 1. Unit = one PWM clock cycle.

Figure 4-52, Figure 4-53, Figure 4-54 show the Precise Center-aligned PWM timing and operation flow.

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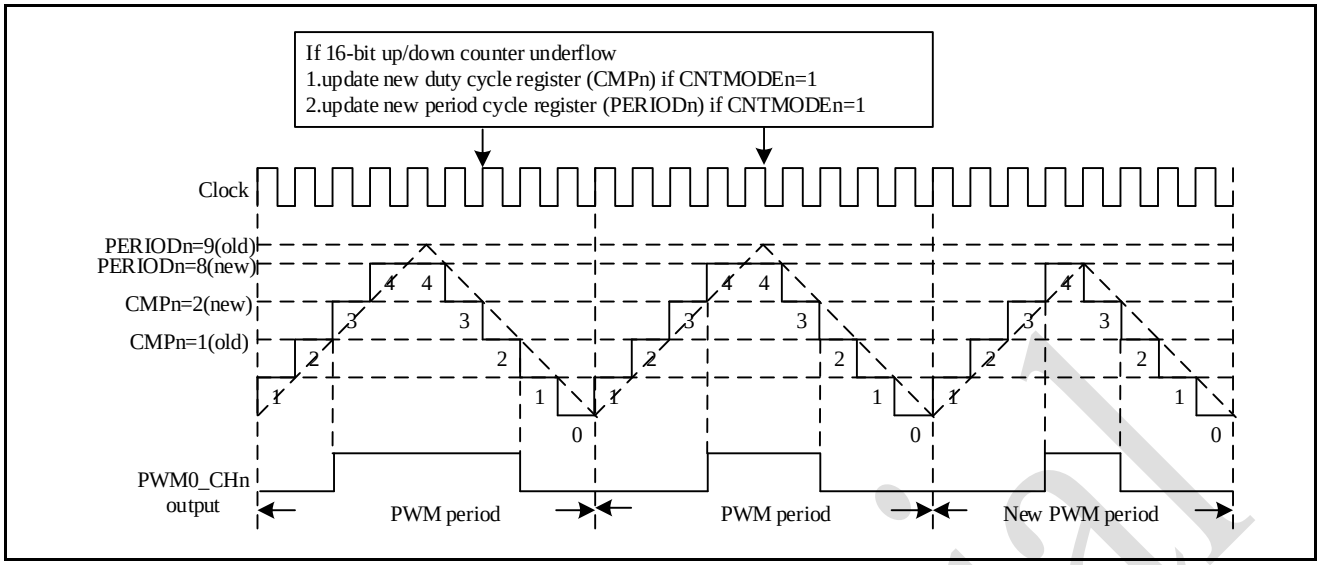

Figure 4-52 Precise Center-aligned Type PWM

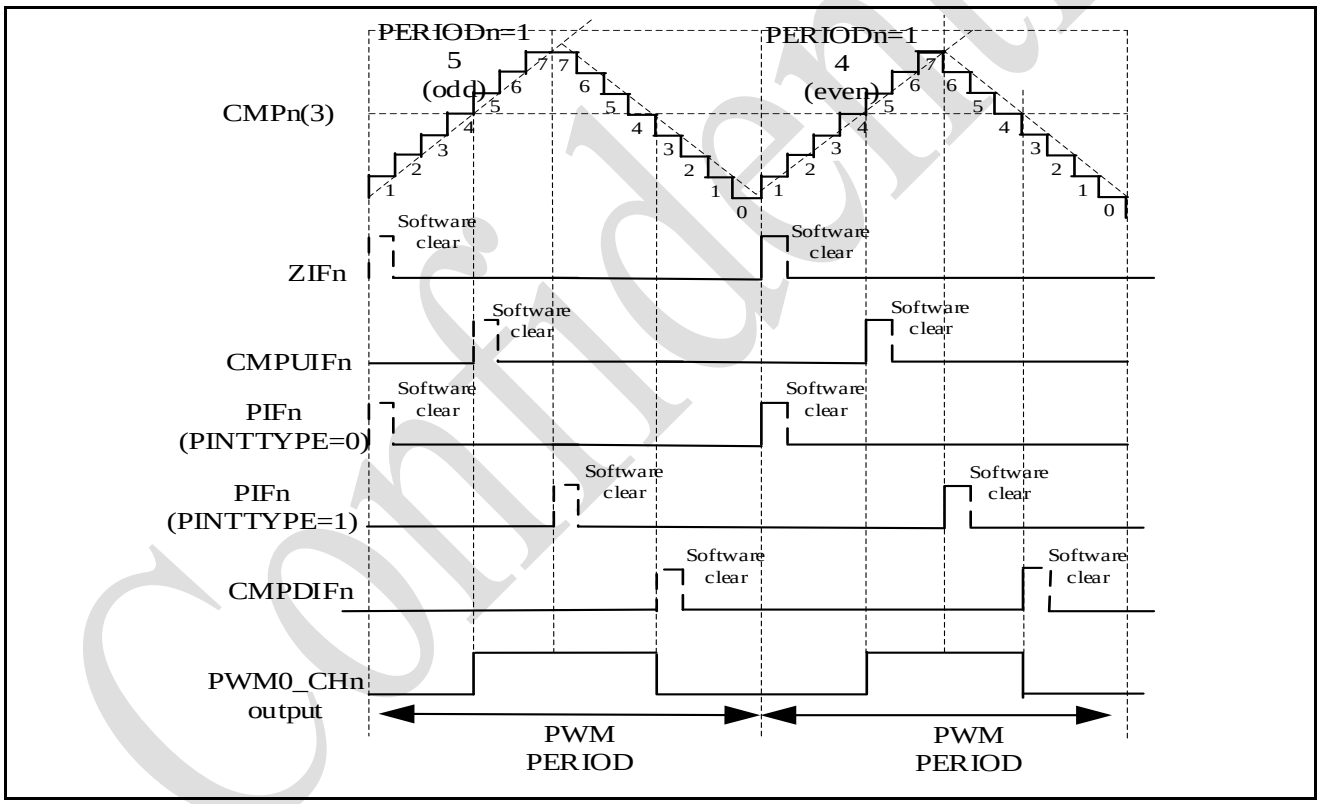

Figure 4-53 PWM Precise Center-aligned Waveform Timing Diagram

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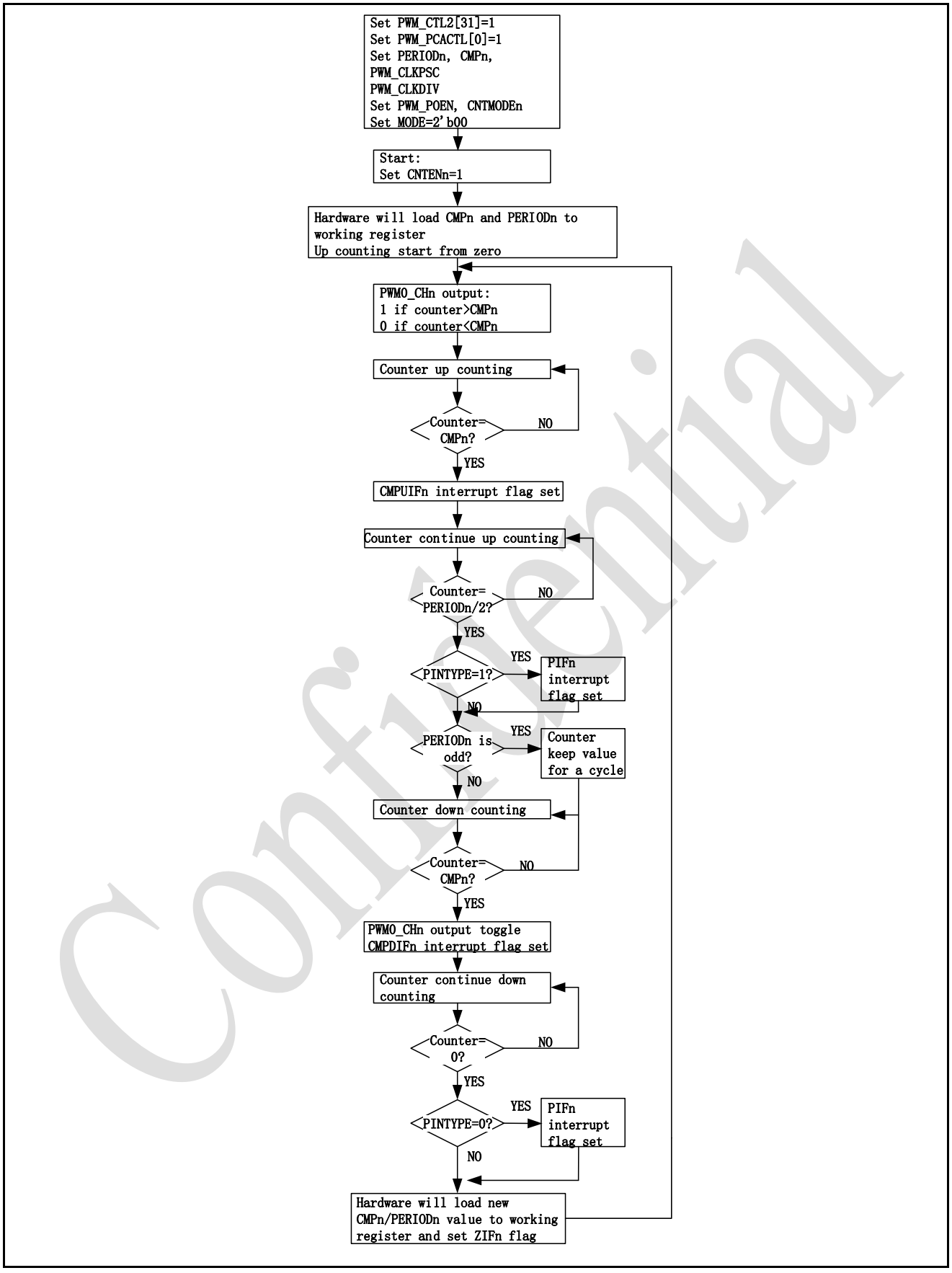

Figure 4-54 Precise Center-aligned Flow Diagram

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4.8.5.2 PWM Center Loading Operation

In center-aligned or precise center-aligned type, PWM also supports loading new PERIODn, CMPn. If operating in asymmetric mode, CMPDn will also supports center loading operation.When counter counts to center of PWM period. This function is enabled by setting HCUPDT (PWM_CTL[5]). Figure 4-55 shows an example of center loading operation, when counter counts to original center 4; it updates its value to PERIODn 6 then continues counting down.

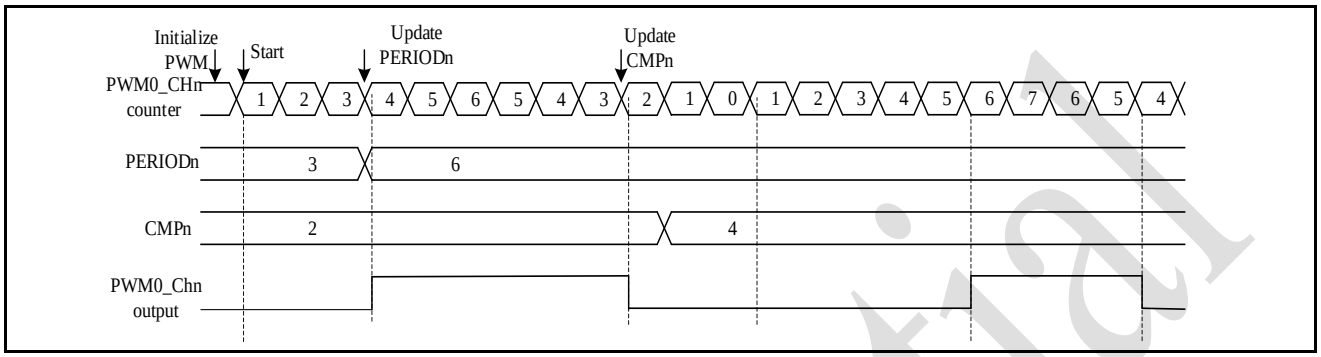

Figure 4-55 PWM Center Loading Timing Diagram

4.8.5.3 PWM Double Buffering and Auto-reload Operation

The PAN2025 series PWM has double buffering function, the reload value is updated at the start of next period without affecting current counter operation. The PWM counter value can be written into PERIODn.

PWM0_CH0 will operate in Auto-reload mode if CNTMODE0 bit is set to 1. It is recommended that switch PWM0_CH0 operating mode before setting CNTEN0 bit to 1 to enable PWM0_CH0 counter to start running because the content of PERIOD0 and CMP0 will be cleared to 0 to reset the PWM0_CH0 period and duty setting when PWM0_CH0 operating mode is changed. As PWM0_CH0 operates at auto-reload mode, CMP0 and PERIOD0 should be written first and then set CNTEN0 bit to 1 to enable PWM0_CH0 counter to start running. The PERIOD0 value will be reloaded to PWM0_CH0 counter when the down counting reaches 0. If the PERIOD0 is set to 0, PWM0_CH0 counter will be held. PWM0_CH1~PWM0_CH7 performs the same function as PWM0_CH0

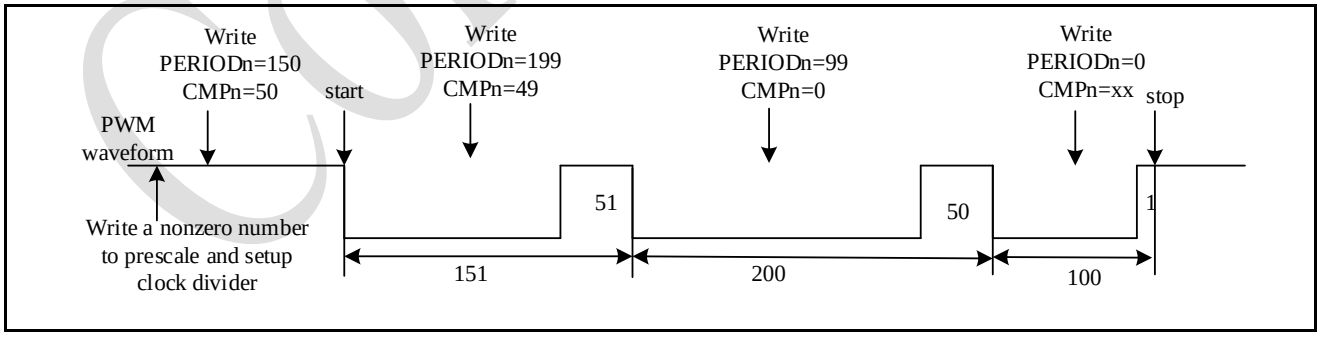

Figure 4-56 PWM Double Buffering Illustration

4.8.5.4 Modulate Duty Ratio

The double buffering function allows CMPn to be written at any point in the current cycle. The loaded value will take effect from the next cycle

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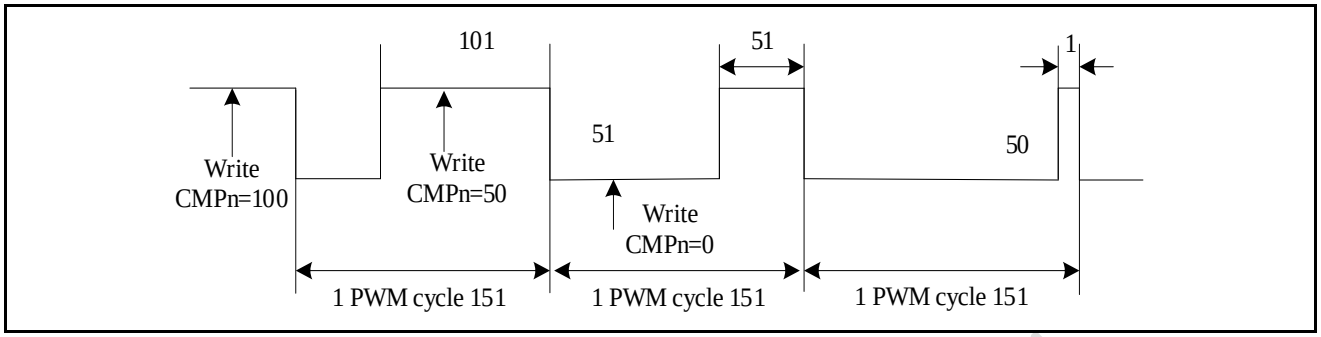

Figure 4-57 PWM Controller Output Duty Ratio

4.8.5.5 PWM Operation Modes

This powerful PWM unit supports independent mode which may be applied to DC or BLDC motor system, Complementary mode with dead-time insertion which may be used in the application of AC induction motor and synchronous motor, and Synchronous mode that makes both pins of each pair are in phase. Besides, the Group mode, which forces the PWM0_CH2, PWM0_CH4 and PWM0_CH6 synchronous with PWM0_CH0 generator, may simplify updating duty control in DC and BLDC motor applications and Asymmetric mode, to generate asymmetric PWM waveform and interrupt timing.

4.8.5.6 Independent Mode

Independent mode is enabled when MODE (PWM_CTL2[29:28]) = 00.

By default, the PWM is operated in independent mode, with eight PWM channels outputs. Each channel is running off its own duty-cycle generator module.

4.8.5.7 Complementary Mode

Complementary mode is enabled when MODE (PWM_CTL2[29:28]) = 01.

In this module there are four duty-cycle generators utilized for complementary mode, with total of four PWM output pairs of pins in this module. The total eight PWM outputs are grouped into output pairs of even and odd numbered outputs. In complimentary modes, the internal odd PWM signal PWM0_CHn, always be the complement of the corresponding even PWM signal. For example, PWM0_CH1 will be the complement of PWM0_CH0. PWM0_CH3 will be the complement of PWM0_CH2, PWM0_CH5 will be the complement of PWM0_CH4, and PWM0_CH7 will be the complement of PWM0_CH6. The time base for the PWM module is provided by its own 16-bit counter, which also incorporates selectable pre-scalar options.

4.8.5.8 Dead-time Insertion

The dead-time generator inserts an “off” period called “dead-time” between the turning off of one pin to the turning on of the complementary pin of the paired pins. This is to prevent damage to the power switching devices that will be connected to the PWM output pins. The complementary output pair mode has an 8-bit down counter used to produce the dead-time insertion. The complementary outputs are delayed until the counter counts down to zero.

The dead-time can be calculated by the following formula:

*dead-time = PWM_CLK * (DTInm+1)*, where nm, could be 01, 23, 45,67

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The timing diagram as shown below indicates the dead-time insertion for one pair of PWM signals.

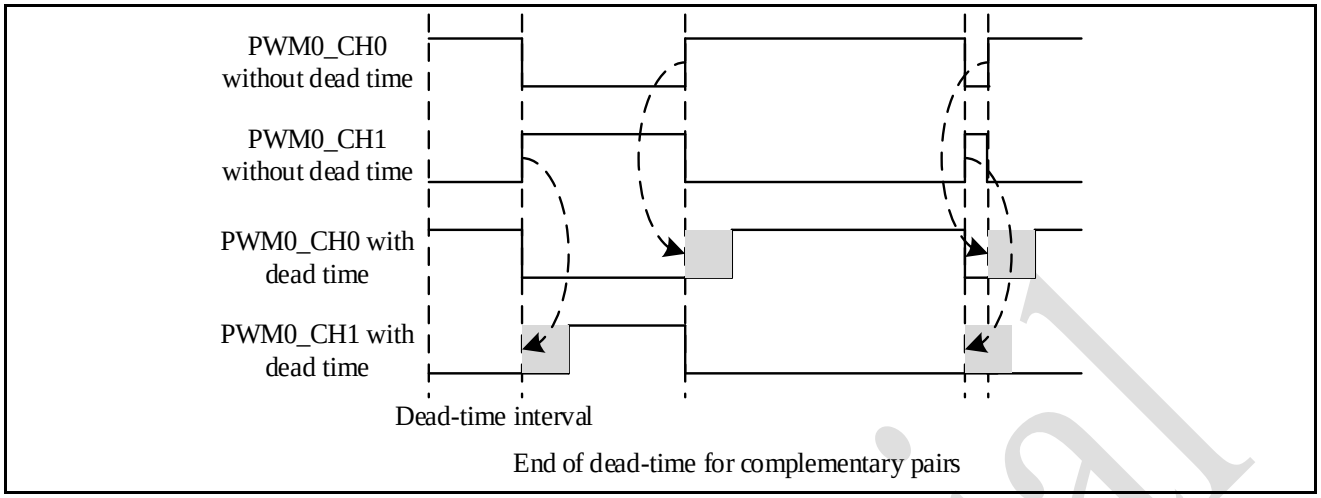

Figure 4-58 Dead-time Insertion

In power inverter applications, a dead-time insertion avoids the upper and lower switches of the half bridge from being active at the same time. Hence the dead-time control is crucial to proper operation of a system. Some amount of time must be provided between turning off of one PWM output in a complementary pair and turning on the other transistor as the power output devices cannot switch instantaneously.

4.8.5.9 Synchronous Mode

Synchronous mode is enabled when MODE (PWM_CTL2[29:28]) = 10.

In the synchronization mode the PWM pair signals from PWM Generator are in-phase.

PWM0_CH1=PWM0_CH0, PWM0_CH3=PWM0_CH2, PWM0_CH5=PWM0_CH4, and PWM0_CH7=PWM0_CH6.

4.8.5.10 Group Mode

Group mode is enabled when GROUPEN (PWM_CTL2[30]) = 1.

This device supports Group mode control which allows all even PWM channel output to be duty controllable by PWM0_CH0 duty register.

If GROUPEN = 1, all (PWM0_CH2, PWM0_CH3), (PWM0_CH4, PWM0_CH5) and (PWM0_CH6, PWM0_CH7) pairs will follow (PWM0_CH0, PWM0_CH1), which imply;

PWM0_CH6 = PWM0_CH4 = PWM0_CH2 = PWM0_CH0;

PWM0_CH7= PWM0_CH5 = PWM0_CH3 = PWM0_CH1 = invert (PWM0_CH0) if Complementary mode is enabled when MODE (PWM_CTL2[29:28]) = 01.

Note: For applications, please do not use Group and Synchronous mode simultaneously because the Synchronous mode will be inactive.

4.8.5.11 Asymmetric Mode

Asymmetric mode only works under Center-aligned type. Asymmetric mode is enabled when ASYMEN (PWM_CTL[21]) = 1. In this mode PWM counter will be compared with another value

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CMPDn (PWM_CMPDATn[31:16]) when counting down. If CMRDn is not equal to the CMRn, the PWM will generate asymmetric waveform and set CMPDIFn (PWM_INTSTS[13:8]) of the corresponding channel n.

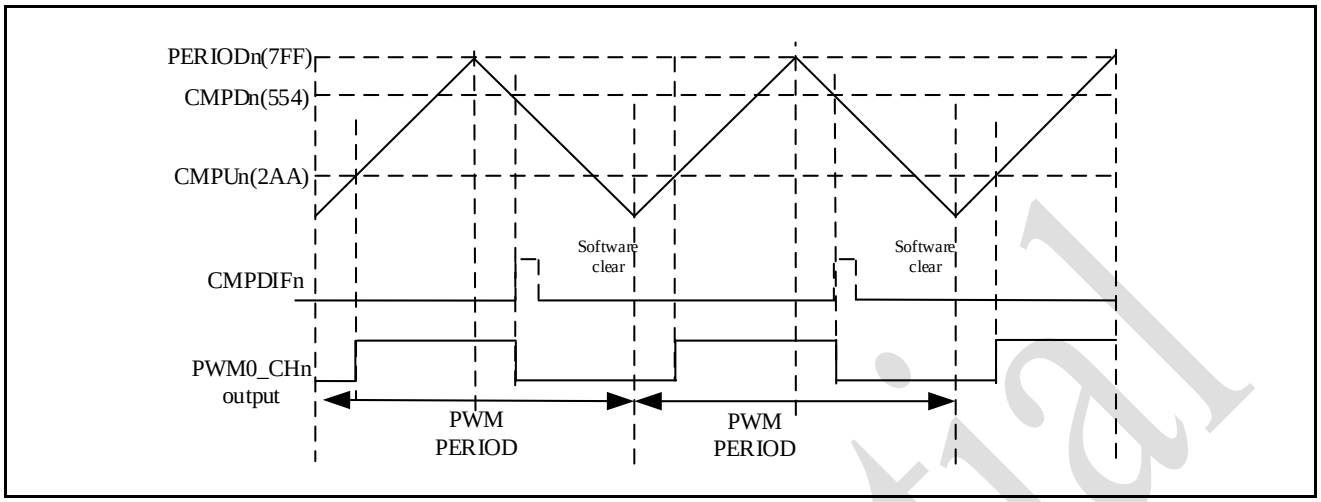

Figure 4-59 Asymmetric Mode Timing Diagram

4.8.5.12 Polarity Control

Each PWM port from PWM0_CH0 to PWM0_CH7 has independent polarity control (PINV0~7) to configure the polarity of active state of PWM output which are described in the PINVn in PWM Control Register (PWM_CTL). By default, the PWM output is active high.

Figure 4-60 shows the initial state before PWM starts with different polarity settings.

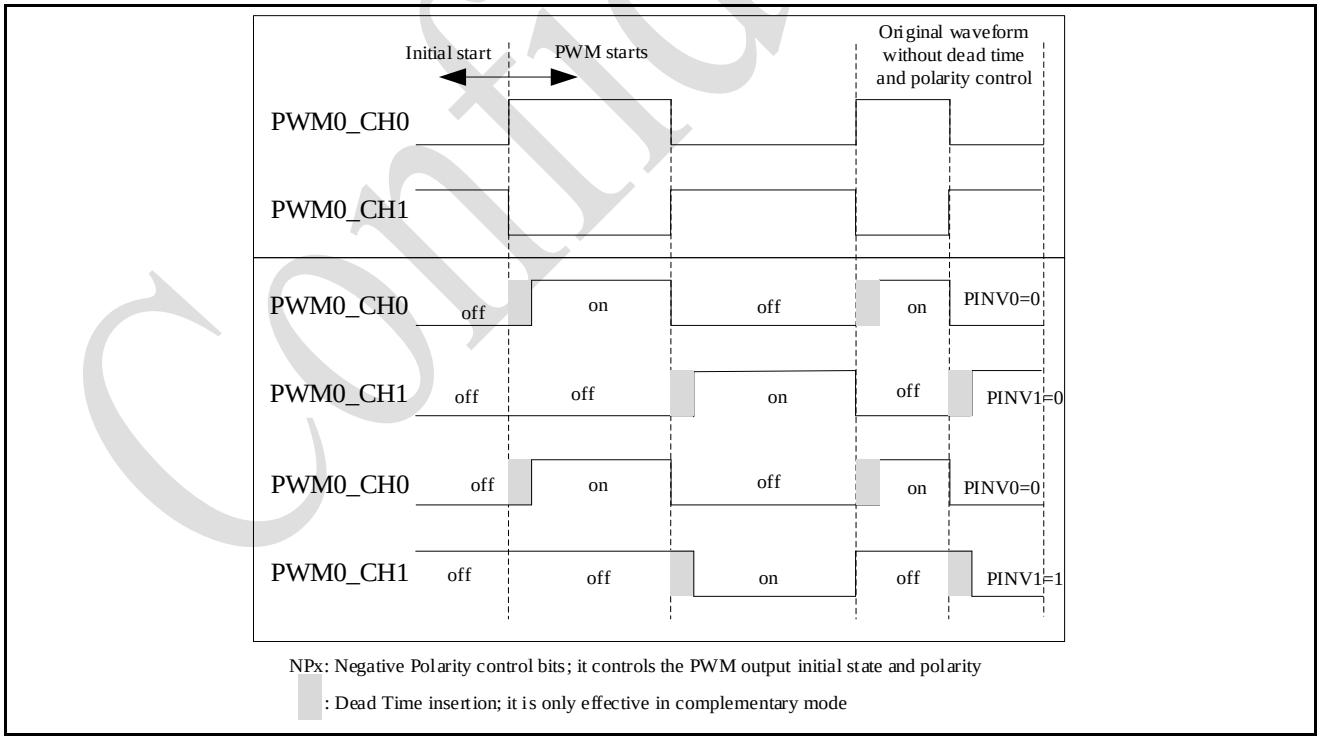

Figure 4-60 Initial State and Polarity Control with Rising Edge Dead-time Insertion

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4.8.5.13 PWM for Motor Control Interrupt Architecture

There are four interrupt sources for PWM unit, which are

- ZIFn (PWM_INTSTS[7:0]) PWM counter count to zero interrupt flag;
- CMPUIFn (PWM_INTSTS[31:24]) PWM counter up-counts to CMPn (PWM_CMPDATn[15:0]) interrupt flag;
- PIFn (PWM_INTSTS[23:16]) PWM counter counts to period of edge-aligned type or counts to center of center-aligned type interrupt flag;
- CMPDIFn (PWM_INTSTS[15:8]) PWM counter down-counts to CMPn (PWM_CMPDATn[15:0]) interrupt flag, if operating in asymmetric type it down count to CMPDn (PWM_CMPDATn[31:16]).

The bits ZIENn (PWM_INTEN[7:0]) control the ZIFn interrupt enable; the bits CMPUIENn (PWM_INTEN[31:24]) control the CMPUIFn interrupt enable; the bits PIENn (PWM_INTEN[23:16]) control the PIFn interrupt enable; and the bits CMPDIENn (PWM_INTEN[15:8]) control the CMPDIFn interrupt enable. Note that all the interrupt flags are set by hardware and must be cleared by software.

Figure 6.7-24 shows the architecture of Motor Control PWM interrupts.

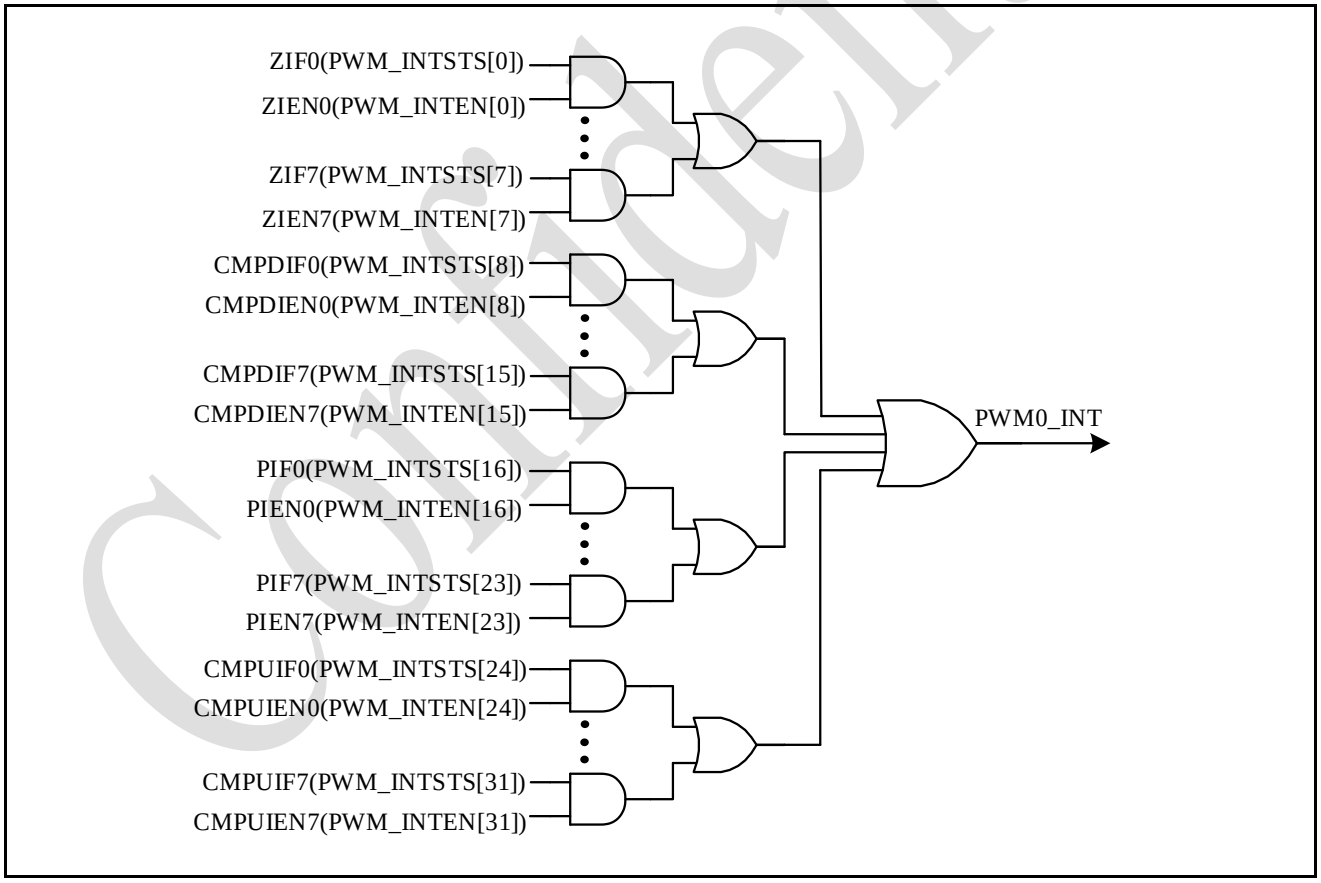

Figure 4-61 Motor Control PWM Interrupt Architecture

4.8.5.14 PWM Counter Start Procedure

The following procedure is recommended for PWM counter start

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1. Configure prescaler register (PWM_CLKPSC) for setting clock prescaler (CLKPSCnm).

2. Configure clock select register (PWM_CLKDIV) for setting clock source select (CLKDIVn).

3. Configure PWM control register (PWM_CTL) for setting auto-reload mode (CNTMODEn = 1), PWM counter aligned type (CNTTYPE) and DISABLE PWM counter (CNTENn = 0).

4. Configure PWM control register (PWM_CTL) for setting inverter on/off (PINVn), and Dead-time generator on/off (DTCNTnm). (Optional)

5. Configure PWM_DTCTL register to set dead-time interval. (Optional)

6. Configure comparator register (PWM_CMPDATn) for setting PWM duty (CMPn).

7. Configure PWM counter register (PWM_PERIODn) for setting PWM counter loaded value (PERIODn).

8. Configure PWM interrupt enable register (PWM_INTEN) for setting PWM period interrupt type (INTTYPE), PWM zero interrupt enable bit (ZIENn), PWM compare up match interrupt enable bit (CMPUIENn), PWM period interrupt enable bit (PIENn), PWM compare down match interrupt enable bit (CMPDIENn). (Optional)

9. Configure PWM output enable register (PWM_POEN) to enable PWM output channel

10. Configure PWM control register (PWM_CTL) to enable PWM counter (CNTENn = 1)

4.8.5.15 PWM Counter Stop Procedure

Method 1:

Set 16-bit counter register (PERIODn) to 0. When interrupt request happens, disable PWM counter (CNTENn in PWM_CTL). (Recommended)

Method 2:

Disable PWM Counter directly (CNTENn in PWM_CTL) (Not recommended)

The reason why this method is not recommended is that disabling CNTENn will immediately stop PWM output signal and lead to change the duty of the PWM output, this may cause damage to the motor control circuit.

4.8.6 PWM Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
PWM0 Base Address: **PWM0_BA = 0x4000_4000**				
PWM_CLKPSC	PWM0_BA+0x00	R/W	PWM Clock Pre-scale Register	0x0000_0000
PWM_CLKDIV	PWM0_BA+0x04	R/W	PWM Clock Select Register	0x0000_0000
PWM_CTL	PWM0_BA+0x08	R/W	PWM Control Register	0x0000_0000
PWM_PERIOD0	PWM0_BA+0x0C	R/W	PWM Counter Period Register 0	0x0000_0000
PWM_PERIOD1	PWM0_BA+0x10	R/W	PWM Counter Period Register 1	0x0000_0000
PWM_PERIOD2	PWM0_BA+0x14	R/W	PWM Counter Period Register 2	0x0000_0000

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PWM_PERIOD3	PWM0_BA+0x18	R/W	PWM Counter Period Register 3	0x0000_0000
PWM_PERIOD4	PWM0_BA+0x1C	R/W	PWM Counter Period Register 4	0x0000_0000
PWM_PERIOD5	PWM0_BA+0x20	R/W	PWM Counter Period Register 5	0x0000_0000
PWM_PERIOD6	PWM0_BA+0x24	R/W	PWM Counter Period Register 6	0x0000_0000
PWM_PERIOD7	PWM0_BA+0x28	R/W	PWM Counter Period Register 7	0x0000_0000
PWM_CMPDAT0	PWM0_BA+0x2C	R/W	PWM Comparator Register 0	0x0000_0000
PWM_CMPDAT1	PWM0_BA+0x30	R/W	PWM Comparator Register 1	0x0000_0000
PWM_CMPDAT2	PWM0_BA+0x34	R/W	PWM Comparator Register 2	0x0000_0000
PWM_CMPDAT3	PWM0_BA+0x38	R/W	PWM Comparator Register 3	0x0000_0000
PWM_CMPDAT4	PWM0_BA+0x3C	R/W	PWM Comparator Register 4	0x0000_0000
PWM_CMPDAT5	PWM0_BA+0x40	R/W	PWM Comparator Register 5	0x0000_0000
PWM_CMPDAT6	PWM0_BA+0x44	R/W	PWM Comparator Register 6	0x0000_0000
PWM_CMPDAT7	PWM0_BA+0x48	R/W	PWM Comparator Register 7	0x0000_0000
PWM_CTL2	PWM0_BA+0x4C	R/W	PWM Control Register	0x0000_0000
PWM_FLAG	PWM0_BA+0x50	R/W	PWM Status Register	0x0000_0000
PWM_INTEN	PWM0_BA+0x54	R/W	PWM Interrupt Enable Register	0x0000_0000
PWM_INTSTS	PWM0_BA+0x58	R/W	PWM Interrupt Status Register	0x0000_0000
PWM_POEN	PWM0_BA+0x5C	R/W	PWM Output Enable Register	0x0000_0000
PWM_DTCTL	PWM0_BA+0x64	R/W	PWM Dead-time Control Register	0x0000_0000
PWM_ADCTCTL0	PWM0_BA+0x68	R/W	PWM Trigger Control Register 0	0x0000_0000
PWM_ADCTCTL1	PWM0_BA+0x6C	R/W	PWM Trigger Control Register 1	0x0000_0000
PWM_ADCTSTS0	PWM0_BA+0x70	R/W	PWM Trigger Status Register 0	0x0000_0000
PWM_ADCTSTS1	PWM0_BA+0x74	R/W	PWM Trigger Status Register 1	0x0000_0000
PWM_PCACTL	PWM0_BA+0x88	R/W	PWM Precise Center-Aligned Type Control Register	0x0000_0000

4.8.7 PWM Register Description

4.8.7.1 PWM Pre-Scale Register (PWM_CLKPSC)

Register	Offset	R/W	Description	Reset Value
PWM_CLKPSC	PWM0_BA+0x00	R/W	PWM Clock Pre-scale Register	0x0000_0000

Bits	Descriptions	
[31:24]	CLKPSC67	Clock Prescaler 6 for PWM Counter 6 and 7 Clock input is divided by (CLKPSC67 + 1) before it is sent to the corresponding PWM counter. If CLKPSC67 = 0, the clock prescaler 6 output clock will be stopped. So the corresponding PWM counter will also be stopped.
[23:16]	CLKPSC45	Clock Prescaler 4 for PWM Counter 4 and 5 Clock input is divided by (CLKPSC45 + 1) before it is sent to the corresponding PWM counter.

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		If CLKPSC45 = 0, the clock prescaler 4 output clock will be stopped. So the corresponding PWM counter will also be stopped.
[15:8]	CLKPSC23	Clock Prescaler 2 for PWM Counter 2 and 3 Clock input is divided by (CLKPSC23 + 1) before it is sent to the corresponding PWM counter. If CLKPSC23 = 0, the clock prescaler 2 output clock will be stopped. So the corresponding PWM counter will also be stopped.
[7:0]	CLKPSC01	Clock Prescaler 0 for PWM Counter 0 and 1 Clock input is divided by (CLKPSC01 + 1) before it is sent to the corresponding PWM counter. If CLKPSC01 = 0, the clock prescaler 0 output clock will be stopped. So the corresponding PWM counter will also be stopped.

4.8.7.2 PWM Clock Selector Register (PWM_CLKDIV)

Register	Offset	R/W	Description	Reset Value
PWM_CLKDIV	PWM0_BA+0x04	R/W	PWM Clock Select Register	0x0000_0000

Bits	Descriptions	
[31]	Reserved	Reserved
[30:28]	CLKDIV7	Counter 7 Clock Divider Selection Select clock input for PWM counter. 000 = Clock input / (CLKPSC67*2). 001 = Clock input / (CLKPSC67*4). 010 = Clock input / (CLKPSC67*8). 011 = Clock input / (CLKPSC67*16). 100 = Clock input / CLKPSC67. Others = Clock input.
[27]	Reserved	Reserved
[26:24]	CLKDIV6	Counter 6 Clock Divider Selection Select clock input for PWM counter. 000 = Clock input / (CLKPSC67*2). 001 = Clock input / (CLKPSC67*4). 010 = Clock input / (CLKPSC67*8). 011 = Clock input / (CLKPSC67*16). 100 = Clock input / CLKPSC67. Others = Clock input.
[23]	Reserved	Reserved
[22:20]	CLKDIV5	Counter 5 Clock Divider Selection Select clock input for PWM counter. 000 = Clock input / (CLKPSC45*2). 001 = Clock input / (CLKPSC45*4). 010 = Clock input / (CLKPSC45*8). 011 = Clock input / (CLKPSC45*16).

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		100 = Clock input / CLKPSC45. Others = Clock input.
[19]	Reserved	Reserved
[18:16]	CLKDIV4	Counter 4 Clock Divider Selection Select clock input for PWM counter. 000 = Clock input / (CLKPSC45*2). 001 = Clock input / (CLKPSC45*4). 010 = Clock input / (CLKPSC45*8). 011 = Clock input / (CLKPSC45*16). 100 = Clock input / CLKPSC45. Others = Clock input.
[15]	Reserved	Reserved
[14:12]	CLKDIV3	Counter 3 Clock Divider Selection Select clock input for PWM counter. 000 = Clock input / (CLKPSC23*2). 001 = Clock input / (CLKPSC23*4). 010 = Clock input / (CLKPSC23*8). 011 = Clock input / (CLKPSC23*16). 100 = Clock input / CLKPSC23. Others = Clock input.
[11]	Reserved	Reserved
[10:8]	CLKDIV2	Counter 2 Clock Divider Selection Select clock input for PWM counter. 000 = Clock input / (CLKPSC23*2). 001 = Clock input / (CLKPSC23*4). 010 = Clock input / (CLKPSC23*8). 011 = Clock input / (CLKPSC23*16). 100 = Clock input / CLKPSC23. Others = Clock input.
[7]	Reserved	Reserved
[6:4]	CLKDIV1	Counter 1 Clock Divider Selection Select clock input for PWM counter. 000 = Clock input / (CLKPSC01*2). 001 = Clock input / (CLKPSC01*4). 010 = Clock input / (CLKPSC01*8). 011 = Clock input / (CLKPSC01*16). 100 = Clock input / CLKPSC01. Others = Clock input.
[3]	Reserved	Reserved
[2:0]	CLKDIV0	Counter 0 Clock Divider Selection Select clock input for PWM counter. 000 = Clock input / (CLKPSC01*2). 001 = Clock input / (CLKPSC01*4).

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		010 = Clock input / (CLKPSC01*8). 011 = Clock input / (CLKPSC01*16). 100 = Clock input / CLKPSC01. Others = Clock input.

4.8.7.3 PWM Control Register (PWM_CTL)

Register	Offset	R/W	Description	Reset Value
PWM_CTL	PWM0_BA+0x08	R/W	PWM Control Register	0x0000_0000

Bits	Descriptions	
[31]	Reserved	Reserved
[30]	PINV7	PWM0_CH7 Output Inverter Enable Bit 0 = PWM0_CH7 output inverter disabled. 1 = PWM0_CH7 output inverter enabled.
[29]	Reserved	Reserved
[28]	CNTEN7	PWM Counter 7 Enable Start Run 0 = Corresponding PWM counter running stopped. 1 = Corresponding PWM counter start run enabled.
[27]	Reserved	Reserved
[26]	PINV6	PWM0_CH6 Output Inverter Enable Bit 0 = PWM0_CH6 output inverter disabled. 1 = PWM0_CH6 output inverter enabled.
[25]	Reserved	Reserved
[24]	CNTEN6	PWM Counter 6 Enable Start Run 0 = Corresponding PWM counter running stopped. 1 = Corresponding PWM counter start run enabled.
[23]	Reserved	Reserved
[22]	PINV5	PWM0_CH5 Output Inverter Enable Bit 0 = PWM0_CH5 output inverter disabled. 1 = PWM0_CH5 output inverter enabled.
[21]	ASYMEN	Asymmetric Mode In Center-aligned Type 0 = Symmetric mode in center-aligned type. 1 = Asymmetric mode in center-aligned type.
[20]	CNTEN5	PWM Counter 5 Enable Start Run 0 = Corresponding PWM counter running stopped. 1 = Corresponding PWM counter start run enabled.
[19]	Reserved	Reserved
[18]	PINV4	PWM0_CH4 Output Inverter Enable Bit 0 = PWM0_CH4 output inverter disabled. 1 = PWM0_CH4 output inverter enabled.
[17]	Reserved	Reserved
[16]	CNTEN4	PWM Counter 4 Enable Start Run 0 = Corresponding PWM counter running stopped.

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		1 = Corresponding PWM counter start run enabled.
[15]	Reserved	Reserved
[14]	PINV3	PWM0_CH 3 Output Inverter Enable Bit 0 = PWM0_CH3 output inverter disabled. 1 = PWM0_CH3 output inverter enabled.
[13]	Reserved	Reserved
[12]	CNTEN3	PWM Counter 3 Enable Start Run 0 = Corresponding PWM counter running stopped. 1 = Corresponding PWM counter start run enabled.
[11]	Reserved	Reserved
[10]	PINV2	PWM0_CH2 Output Inverter Enable Bit 0 = PWM0_CH2 output inverter disabled. 1 = PWM0_CH2 output inverter enabled.
[9]	Reserved	Reserved
[8]	CNTEN2	PWM Counter 2 Enable Start Run 0 = Corresponding PWM counter running stopped. 1 = Corresponding PWM counter start run enabled.
[7]	Reserved	Reserved
[6]	PINV1	PWM0_CH1 Output Inverter Enable Bit 0 = PWM0_CH1 output inverter disabled. 1 = PWM0_CH1 output inverter enable.
[5]	HCUPDT	Half Cycle Update Enable for Center-aligned Type 0 = Disable half cycle update PERIOD & CMP. 1 = Enable half cycle update PERIOD & CMP.
[4]	CNTEN1	PWM Counter 1 Enable/Disable Start Run 0 = Corresponding PWM counter running stopped. 1 = Corresponding PWM counter start run enabled.
[3]	Reserved	Reserved
[2]	PINV0	PWM0_CH0 Output Inverter Enable Bit 0 = PWM0_CH0 output inverter disabled. 1 = PWM0_CH0 output inverter enabled.
[1]	Reserved	Reserved
[0]	CNTEN0	PWM Counter 0 Enable Start Run 0 = Corresponding PWM counter running stopped. 1 = Corresponding PWM counter start run enabled.

4.8.7.4 PWM Counter Register 0-7 (PWM_PERIOD0-7)

Register	Offset	R/W	Description	Reset Value
PWM_PERIOD0	PWM0_BA+0x0C	R/W	PWM Counter Period Register 0	0x0000_0000
PWM_PERIOD1	PWM0_BA+0x10	R/W	PWM Counter Period Register 1	0x0000_0000
PWM_PERIOD2	PWM0_BA+0x14	R/W	PWM Counter Period Register 2	0x0000_0000
PWM_PERIOD3	PWM0_BA+0x18	R/W	PWM Counter Period Register 3	0x0000_0000
PWM_PERIOD4	PWM0_BA+0x1C	R/W	PWM Counter Period Register 4	0x0000_0000

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PWM_PERIOD5	PWM0_BA+0x20	R/W	PWM Counter Period Register 5	0x0000_0000
PWM_PERIOD6	PWM0_BA+0x24	R/W	PWM Counter Period Register 6	0x0000_0000
PWM_PERIOD7	PWM0_BA+0x28	R/W	PWM Counter Period Register 7	0x0000_0000

Bits	Descriptions	
[31:16]	Reserved	Reserved
[15:0] n=0,1..7	PERIODn	PWM Counter Period Value PERIODn determines the PWM counter period. **Edge-aligned type**: *PWM frequency = APB1_CLK/((prescale+1)*(clock divider))/(PERIODn+1)*; where xy, could be 01, 23, 45, 67 depending on the selected PWM channel. *Duty ratio = (CMPn+1)/(PERIODn+1).* PERIOD = 0: PWM is always low. When PERIOD!=0, PWM output is as follow: CMPn ≥ PERIODn: PWM output is always high. CMPn < PERIODn: PWM low width = (PERIODn-CMPn) unit; PWM high width = (CMP+1) unit. CMPn = 0: PWM is always low. **Center-aligned type**: PWM frequency = APB1_CLK/((prescale+1)*(clock divider))/ (2*PERIODn+1); where xy, could be 01, 23, 45, 67 depending on the selected PWM channel. *Duty ratio = (PERIODn - CMPn)/(PERIODn+1).* *PERIOD = 0: PWM is always low.* When PERIOD!=0, PWM output is as follow: CMPn ≥ PERIODn: PWM output is always low. CMPn < PERIODn: PWM low width = (CMPn + 1) * 2 unit; PWM high width = (PERIODn - CMPn) * 2 unit. CMPn = 0: PWM is always high. (Unit = One PWM clock cycle). **Note**: Any write to PERIODn will take effect in the next PWM cycle.

4.8.7.5 PWM Comparator Register 0-7 (PWM_CMPDAT0-7)

Register	Offset	R/W	Description	Reset Value
PWM_CMPDAT0	PWM0_BA+0x2C	R/W	PWM Comparator Register 0	0x0000_0000
PWM_CMPDAT1	PWM0_BA+0x30	R/W	PWM Comparator Register 1	0x0000_0000
PWM_CMPDAT2	PWM0_BA+0x34	R/W	PWM Comparator Register 2	0x0000_0000
PWM_CMPDAT3	PWM0_BA+0x38	R/W	PWM Comparator Register 3	0x0000_0000
PWM_CMPDAT4	PWM0_BA+0x3C	R/W	PWM Comparator Register 4	0x0000_0000
PWM_CMPDAT5	PWM0_BA+0x40	R/W	PWM Comparator Register 5	0x0000_0000
PWM_CMPDAT6	PWM0_BA+0x44	R/W	PWM Comparator Register 6	0x0000_0000
PWM_CMPDAT7	PWM0_BA+0x48	R/W	PWM Comparator Register 7	0x0000_0000

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Bits	Descriptions	
[31:16] n=0,1..7	CMPDn	PWM Comparator Register for Down Counter In Asymmetric Mode CMPn ≥ PERIODn: up counter PWM output is always low. CMPDn ≥ PERIODn: down counter PWM output is always low. Others: PWM output is always high.
[15:0] n=0,1..7	CMPn	PWM Comparator Register CMP determines the PWM duty. Edge-aligned type: PWM frequency = APB1_CLK/(((CLKPSCnm+1)*(clock divider))/(PERIODn+1); where nm, could be 01, 23, 45, 67 depending on the selected PWM channel. *Duty ratio = (CMPn+1)/(PERIODn+1).* PERIOD = 0: PWM is always low. When PERIOD!=0, PWM output is as follow: CMPn ≥ PERIODn: PWM output is always high. CMPn < PERIODn: PWM low width = (PERIODn-CMPn) unit; PWM high width = (CMP+1) unit. CMPn = 0: PWM is always low. Center-aligned type: PWM frequency = APB1_CLK/((prescale+1)*(clock divider))/ (2*PERIODn+1); where xy, could be 01, 23, 45, 67 depending on the selected PWM channel. *Duty ratio = (PERIODn - CMPn)/(PERIODn+1).* *PERIOD = 0: PWM is always low.* When PERIOD!=0, PWM output is as follow: CMPn ≥ PERIODn: PWM output is always low. CMPn < PERIODn: PWM low width = (CMPn + 1) * 2 unit; PWM high width = (PERIODn - CMPn) * 2 unit. CMPn = 0: PWM is always high. (Unit = One PWM clock cycle). **Note**: Any write to CMPn will take effect in the next PWM cycle.

4.8.7.6 PWM Control Register2 (PWM_CTL2)

Register	Offset	R/W	Description	Reset Value
PWM_CTL2	PWM0_BA+0x4C	R/W	PWM Control Register	0x0000_0000

Bits	Descriptions	
[31]	CNTTYPE	PWM Counter-aligned Type Select Bit 0 = Edge-aligned type. 1 = Center-aligned type.
[30]	GROUPEN	Group Function Enable Bit 0 = The signals timing of all PWM channels are independent. 1 = Unify the signals timing of PWM0_CH0, PWM0_CH2, PWM0_CH4 and PWM0_CH6 in the same phase which is controlled by PWM0_CH0 and also unify the signals timing of PWM0_CH1, PWM0_CH3, PWM0_CH5 and PWM0_CH7

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		in the same phase which is controlled by PWM0_CH1.
[29:28]	MODE	PWM Operating Mode Select Bit 00 = Independent mode. 01 = Complementary mode. 10 = Synchronized mode. 11 = Reserved.
[27]	DTCNT67	Dead-time 6 Counter Enable Bit (PWM0_CH6 and PWM0_CH7 Pair for PWMC Group) 0 = Dead-time 6 generator disabled. 1 = Dead-time 6 generator enabled. **Note**: When the dead-time generator is enabled, the pair of PWM0_CH6 and PWM0_CH7 becomes a complementary pair for PWMC group.
[26]	DTCNT45	Dead-time 4 Counter Enable Bit (PWM0_CH4 and PWM0_CH5 Pair for PWMC Group) 0 = Dead-time 4 generator disabled. 1 = Dead-time 4 generator enabled. **Note**: When the dead-time generator is enabled, the pair of PWM0_CH4 and PWM0_CH5 becomes a complementary pair for PWMC group.
[25]	DTCNT23	Dead-time 2 Counter Enable Bit (PWM0_CH2 and PWM0_CH3 Pair for PWMB Group) 0 = Dead-time 2 generator disabled. 1 = Dead-time 2 generator enabled. **Note**: When the dead-time generator is enabled, the pair of PWM0_CH2 and PWM0_CH3 becomes a complementary pair for PWMB group.
[24]	DTCNT01	Dead-time 0 Counter Enable Bit (PWM0_CH0 and PWM0_CH1 Pair for PWMA Group) 0 = Dead-time 0 generator disabled. 1 = Dead-time 0 generator enabled. **Note**: When the dead-time generator is enabled, the pair of PWM0_CH0 and PWM0_CH1 becomes a complementary pair for PWMA group.
[23:18]	Reserved	Reserved
[17]	PINTTYPE	PWM Interrupt Type Selection 0 = ZIFn will be set if PWM counter underflows. 1 = ZIFn will be set if PWM counter matches PERIODn register. **Note**: This bit is effective when PWM is in center-aligned type only.
[16:0]	Reserved	Reserved

4.8.7.7 PWM Flag Indication Register (PWM_FLAG)

Register	Offset	R/W	Description	Reset Value
PWM_FLAG	PWM0_BA+0x50	R/W	PWM Status Flag Register	0x0000_0000

Bits	Descriptions	
[31:24]	CMPUFn	PWM Compare Up Flag

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n=0,1..7		Flag is set by hardware when PWM0_CHn up_counter reaches CMPn. **Note**: This bit can be cleared by software writing 1.
[23:16] n=0,1..7	PFn	PWM Period Flag Flag is set by hardware when PWM0_CHn counter reaches PERIODn. **Note**: This bit can be cleared by software writing 1.
[15:8] n=0,1..7	CMPDFn	PWM Compare Down Flag Flag is set by hardware when PWMn down_counter reaches CMPn. **Note**: This bit can be cleared by software writing 1.
[7:0] n=0,1..7	ZFn	PWM Zero Point Flag Flag is set by hardware when PWMn down_counter reaches zero point. **Note**: This bit can be cleared by software writing 1.

4.8.7.8 PWM Interrupt Enable Register (PWM_INTEN)

Register	Offset	R/W	Description	Reset Value
PWM_INTEN	PWM0_BA+0x54	R/W	PWM Interrupt Enable Register	0x0000_0000

Bits	Descriptions	
[31:24] n=0,1..7	CMPUIENn	PWM Compare Up Interrupt Enable Bit 0 = PWM0_CHn compare up interrupt disabled. 1 = PWM0_CHn compare up interrupt enabled.
[23:16] n=0,1..7	PIENn	PWM Period Interrupt Enable Bit 0 = PWM0_CHn period interrupt disabled. 1 = PWM0_CHn period interrupt enabled.
[15:8] n=0,1..7	CMPDIENn	PWM Compare Down Interrupt Enable Bit 0 = PWM0_CHn compare down interrupt disabled. 1 = PWM0_CHn compare down interrupt enabled.
[7:0] n=0,1..7	ZIENn	PWM Zero Point Interrupt Enable Bit 0 = PWM0_CHn zero point interrupt disabled. 1 = PWM0_CHn zero point interrupt enabled.

4.8.7.9 PWM Interrupt Indication Register (PWM_INTSTS)

Register	Offset	R/W	Description	Reset Value
PWM_INTSTS	PWM0_BA+0x58	R/W	PWM Interrupt Status Register	0x0000_0000

Bits	Descriptions	
[31:24] n=0,1..7	CMPUIFn	PWM Compare Up Interrupt Flag Flag is set by hardware when PWM0_CHn counter up count reaches CMPn. **Note**: This bit can be cleared by software writing 1.
[23:16] n=0,1..7	PIFn	PWM Period Interrupt Flag Flag is set by hardware when PWM0_CHn counter reaches PERIODn. **Note**: This bit can be cleared by software writing 1.
[15:8]	CMPDIFn	PWM Compare Down Interrupt Flag

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n=0,1..7		Flag is set by hardware when PWMn counter down count reaches CMPn. **Note**: This bit can be cleared by software writing 1.
[7:0] n=0,1..7	ZIFn	PWM Zero Point Interrupt Flag Flag is set by hardware when PWMn counter down count reaches zero point. **Note**: This bit can be cleared by software writing 1.

4.8.7.10 PWM Output Control Register (PWM_POEN)

Register	Offset	R/W	Description	Reset Value
PWM_POEN	PWM0_BA+0x5C	R/W	PWM Output Enable Register	0x0000_0000

Bits	Descriptions	
[31:8]	Reserved	Reserved
[7:0] n=0,1..7	POENn	PWM Output Enable Bits 0 = PWM channel n output to pin disabled. 1 = PWM channel n output to pin enabled. **Note**: The corresponding GPIO pin must be switched to PWM function.

4.8.7.11 PWM Dead-time Interval Register (PWM_DTCTL)

Register	Offset	R/W	Description	Reset Value
PWM_DTCTL	PWM0_BA+0x64	R/W	PWM Dead-time Control Register	0x0000_0000

Bits	Descriptions	
[31:24]	DTI67	Dead-time Interval Register for Pair of Channel6 and Channel7 (PWM0_CH6 and PWM0_CH7 Pair) These 8 bits determine dead-time length. The unit time of dead-time length is received from corresponding PWM_CLKDIV bits.
[23:16]	DTI45	Dead-time Interval Register for Pair of Channel4 and Channel5 (PWM0_CH4 and PWM0_CH5 Pair) These 8 bits determine dead-time length. The unit time of dead-time length is received from corresponding PWM_CLKDIV bits.
[15:8]	DTI23	Dead-time Interval Register for Pair of Channel2 and Channel3 (PWM0_CH2 and PWM0_CH3 Pair) These 8 bits determine dead-time length. The unit time of dead-time length is received from corresponding PWM_CLKDIV bits.
[7:0]	DTI01	Dead-time Interval Register for Pair of Channel0 and Channel1 (PWM0_CH0 and PWM0_CH1 Pair) These 8 bits determine dead-time length. The unit time of dead-time length is received from corresponding PWM_CLKDIV bits.

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4.8.7.12 PWM Trigger ADC Control Register (PWM_ADCTCTL0)

Register	Offset	R/W	Description	Reset Value
PWM_ADCTCTL0	PWM0_BA+0x68	R/W	PWM Trigger Control Register 0	0x0000_0000

Bits	Descriptions	
[31:28]	Reserved	Reserved
[27]	ZPTRGEN3	Channel 3 Zero Point Trigger ADC Enable Bit Enable PWM trigger ADC function while channel3's counter matching 0 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[26]	CDTRGEN3	Channel 3 Compare Down Trigger ADC Enable Bit Enable PWM trigger ADC function while channel3's counter matching CMP3 in down-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[25]	CPTRGEN3	Channel 3 Center Point Trigger ADC Enable Bit Enable PWM Trigger ADC Function While channel3's Counter Matching PE-RIOD3 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[24]	CUTRGEN3	Channel 3 Compare Up Trigger ADC Enable Bit Enable PWM trigger ADC function while channel3's counter matching CMP3 in up-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[23:20]	Reserved	Reserved
[19]	ZPTRGEN2	Channel 2 Zero Point Trigger ADC Enable Bit Enable PWM trigger ADC function while channel2's counter matching 0 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[18]	CDTRGEN2	Channel 2 Compare Down Trigger ADC Enable Bit Enable PWM trigger ADC function while channel2's counter matching CMP2 in down-count direction

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		0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[17]	CPTRGEN2	Channel 2 Center Point Trigger ADC Enable Bit Enable PWM Trigger ADC Function While channel2's Counter Matching PERIOD2 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[16]	CUTRGEN2	Channel 2 Compare Up Trigger ADC Enable Bit Enable PWM trigger ADC function while channel2's counter matching CMP2 in up-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[15:12]	Reserved	Reserved
[11]	ZPTRGEN1	Channel 1 Zero Point Trigger ADC Enable Bit Enable PWM trigger ADC function while channel1's counter matching 0 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[10]	CDTRGEN1	Channel 1 Compare Down Trigger ADC Enable Bit Enable PWM trigger ADC function while channel1's counter matching CMP1 in down-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[9]	CPTRGEN1	Channel 1 Center Point Trigger ADC Enable Bit Enable PWM Trigger ADC Function While channel0's Counter Matching PERIOD1 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[8]	CUTRGEN1	Channel 1 Compare Up Trigger ADC Enable Bit Enable PWM trigger ADC function while channel1's counter matching CMP1 in up-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled.

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		Note: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[7:4]	Reserved	Reserved
[3]	ZPTRGEN0	Channel 0 Zero Point Trigger ADC Enable Bit Enable PWM trigger ADC function while channel0's counter matching 0 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[2]	CDTRGEN0	Channel 0 Compare Down Trigger ADC Enable Bit Enable PWM trigger ADC function while channel0's counter matching CMP0 in down-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[1]	CPTRGEN0	Channel 0 Center Point Trigger ADC Enable Bit Enable PWM Trigger ADC Function While channel0's Counter Matching PE-RIOD0 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. Note: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[0]	CUTRGEN0	Channel 0 Compare Up Trigger ADC Enable Bit Enable PWM trigger ADC function while channel0's counter matching CMP0 in up-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. Note: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.

4.8.7.13 PWM Trigger ADC Control Register (PWM_ADCTCTL1)

Register	Offset	R/W	Description	Reset Value
PWM_ADCTCTL1	PWM0_BA+0x6C	R/W	PWM Trigger Control Register 0	0x0000_0000

Bits	Descriptions	
[31:28]	Reserved	Reserved
[27]	ZPTRGEN7	Channel 7 Zero Point Trigger ADC Enable Bit Enable PWM trigger ADC function while channel7's counter matching 0 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.

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[26]	CDTRGEN7	Channel 7 Compare Down Trigger ADC Enable Bit Enable PWM trigger ADC function while channel7's counter matching CMP7 in down-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[25]	CPTRGEN7	Channel 7 Center Point Trigger ADC Enable Bit Enable PWM Trigger ADC Function While channel7's Counter Matching PERIOD7 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[24]	CUTRGEN7	Channel 7 Compare Up Trigger ADC Enable Bit Enable PWM trigger ADC function while channel7's counter matching CMP7 in up-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[23:20]	Reserved	Reserved
[19]	ZPTRGEN6	Channel 6 Zero Point Trigger ADC Enable Bit Enable PWM trigger ADC function while channel6's counter matching 0 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[18]	CDTRGEN6	Channel 6 Compare Down Trigger ADC Enable Bit Enable PWM trigger ADC function while channel6's counter matching CMP6 in down-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[17]	CPTRGEN6	Channel 6 Center Point Trigger ADC Enable Bit Enable PWM Trigger ADC Function While channel6's Counter Matching PERIOD6 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[16]	CUTRGEN6	Channel 6 Compare Up Trigger ADC Enable Bit Enable PWM trigger ADC function while channel6's counter matching CMP6 in

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		up-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[15:12]	Reserved	Reserved
[11]	ZPTRGEN5	Channel 5 Zero Point Trigger ADC Enable Bit Enable PWM trigger ADC function while channel5's counter matching 0 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[10]	CDTRGEN5	Channel 5 Compare Down Trigger ADC Enable Bit Enable PWM trigger ADC function while channel5's counter matching CMP5 in down-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[9]	CPTRGEN5	Channel 5 Center Point Trigger ADC Enable Bit Enable PWM Trigger ADC Function While channel5's Counter Matching PE-RIOD5 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[8]	CUTRGEN5	Channel 5 Compare Up Trigger ADC Enable Bit Enable PWM trigger ADC function while channel5's counter matching CMP5 in up-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[7:4]	Reserved	Reserved
[3]	ZPTRGEN4	Channel 4 Zero Point Trigger ADC Enable Bit Enable PWM trigger ADC function while channel4's counter matching 0 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[2]	CDTRGEN4	Channel 4 Compare Down Trigger ADC Enable Bit Enable PWM trigger ADC function while channel4's counter matching CMP4 in down-count direction 0 = PWM condition trigger ADC function disabled.

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		1 = PWM condition trigger ADC function enabled. **Note**: This bit is valid for both center-aligned type and edged-aligned type.
[1]	CPTRGEN4	Channel 4 Center Point Trigger ADC Enable Bit Enable PWM Trigger ADC Function While channel4's Counter Matching PERIOD4 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.
[0]	CUTRGEN4	Channel 4 Compare Up Trigger ADC Enable Bit Enable PWM trigger ADC function while channel4's counter matching CMP4 in up-count direction 0 = PWM condition trigger ADC function disabled. 1 = PWM condition trigger ADC function enabled. **Note**: This bit is only valid for PWM in center-aligned type. When PWM is in edged-aligned type, setting this bit is meaningless and will not take any effect.

4.8.7.14 PWM Trigger Status Register (PWM_ADCTSTS0)

Register	Offset	R/W	Description	Reset Value
PWM_ADCTSTS0	PWM0_BA+0x70	R/W	PWM Trigger Status Register 0	0x0000_0000

Bits	Descriptions	
[31:28]	Reserved	Reserved
[27]	ZPTRGF3	Channel 3 Zero Point Trigger ADC Flag When the channel3's counter counts to zero point, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[26]	CDTRGF3	Channel 3 Compare Down Trigger ADC Flag When the channel3's counter counts down to CMP3, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[25]	CPTRGF3	Channel 3 Center Point Trigger ADC Flag When the channel3's counter counts to PERIOD3, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[24]	CUTRGF3	Channel 3 Compare Up Trigger ADC Flag When the channel3's counter counts up to CMP3, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[23:20]	Reserved	Reserved
[19]	ZPTRGF2	Channel 2 Zero Point Trigger ADC Flag When the channel2's counter counts to zero point, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[18]	CDTRGF2	Channel 2 Compare Down Trigger ADC Flag When the channel2's counter counts down to CMP2, this bit will be set for trigger ADC.

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		Note: This bit can be cleared by software writing 1.
[17]	CPTRGF2	Channel 2 Center Point Trigger ADC Flag When the channel2's counter counts to PERIOD2, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[16]	CUTRGF2	Channel 2 Compare Up Trigger ADC Flag When the channel2's counter counts up to CMP2, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[15:12]	Reserved	Reserved
[11]	ZPTRGF1	Channel 1 Zero Point Trigger ADC Flag When the channel1's counter counts to zero point, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[10]	CDTRGF1	Channel 1 Compare Down Trigger ADC Flag When the channel1's counter counts down to CMP1, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[9]	CPTRGF1	Channel 1 Center Point Trigger ADC Flag When the channel1's counter counts to PERIOD1, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[8]	CUTRGF1	Channel 1 Compare Up Trigger ADC Flag When the channel1's counter counts up to CMP1, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[7:4]	Reserved	Reserved
[3]	ZPTRGF0	Channel 0 Zero Point Trigger ADC Flag When the channel0's counter counts to zero point, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[2]	CDTRGF0	Channel 0 Compare Down Trigger ADC Flag When the channel0's counter counts down to CMP0, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[1]	CPTRGF0	Channel 0 Center Point Trigger ADC Flag When the channel0's counter counts to PERIOD0, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[0]	CUTRGF0	Channel 0 Compare Up Trigger ADC Flag When the channel0's counter counts up to CMP0, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.

4.8.7.15 PWM Trigger Status Register (PWM_ADCTSTS1)

Register	Offset	R/W	Description	Reset Value
PWM_ADCTSTS1	PWM0_BA+0x74	R/W	PWM Trigger Status Register 1	0x0000_0000

Bits	Descriptions	
[31:28]	Reserved	Reserved
[27]	ZPTRGF7	Channel 7 Zero Point Trigger ADC Flag When the channel7's counter counts to zero point, this bit will be set for trigger ADC.

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		Note: This bit can be cleared by software writing 1.
[26]	CDTRGF7	Channel 7 Compare Down Trigger ADC Flag When the channel7's counter counts down to CMP7, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[25]	CPTRGF7	Channel 7 Center Point Trigger ADC Flag When the channel7's counter counts to PERIOD7, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[24]	CUTRGF7	Channel 7 Compare Up Trigger ADC Flag When the channel7's counter counts up to CMP7, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[23:20]	Reserved	Reserved
[19]	ZPTRGF6	Channel 6 Zero Point Trigger ADC Flag When the channel6's counter counts to zero point, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[18]	CDTRGF6	Channel 6 Compare Down Trigger ADC Flag When the channel6's counter counts down to CMP6, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[17]	CPTRGF6	Channel 6 Center Point Trigger ADC Flag When the channel6's counter counts to PERIOD6, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[16]	CUTRGF6	Channel 6 Compare Up Trigger ADC Flag When the channel6's counter counts up to CMP6, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[15:12]	Reserved	Reserved
[11]	ZPTRGF5	Channel 5 Zero Point Trigger ADC Flag When the channel5's counter counts to zero point, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[10]	CDTRGF5	Channel 5 Compare Down Trigger ADC Flag When the channel5's counter counts down to CMP5, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[9]	CPTRGF5	Channel 5 Center Point Trigger ADC Flag When the channel5's counter counts to PERIOD5, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[8]	CUTRGF5	Channel 5 Compare Up Trigger ADC Flag When the channel5's counter counts up to CMP5, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[7:4]	Reserved	Reserved
[3]	ZPTRGF4	Channel 4 Zero Point Trigger ADC Flag When the channel4's counter counts to zero point, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[2]	CDTRGF4	Channel 4 Compare Down Trigger ADC Flag When the channel4's counter counts down to CMP4, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.

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[1]	CPTRGF4	Channel 4 Center Point Trigger ADC Flag When the channel4's counter counts to PERIOD4, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.
[0]	CUTRGF4	Channel 4 Compare Up Trigger ADC Flag When the channel4's counter counts up to CMP4, this bit will be set for trigger ADC. **Note**: This bit can be cleared by software writing 1.

4.8.7.16 Precise PWM Center-Aligned Type Control Register (PWM_PCACTL)

Register	Offset	R/W	Description	Reset Value
PWM_PCACTL	PWM0_BA+0x88	R/W	PWM Precise Center-Aligned Type Control Register	0x0000_0000

Bits	Descriptions	
[31:1]	Reserved	Reserved
[0]	PCAEN	PWM Precise Center-aligned Type Enable Bit 0 = Precise center-aligned type disabled. 1 = Precise center-aligned type enabled.

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4.9 Watchdog Timer (WDT)

4.9.1 Overview

The Watchdog Timer is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

4.9.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycles and the time-out interval is 0.5ms ~ 8.192s if WDT_CLK = 32 KHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports WDT time-out wake-up function only if WDT clock source is selected as RCL.

4.9.3 Block Diagram

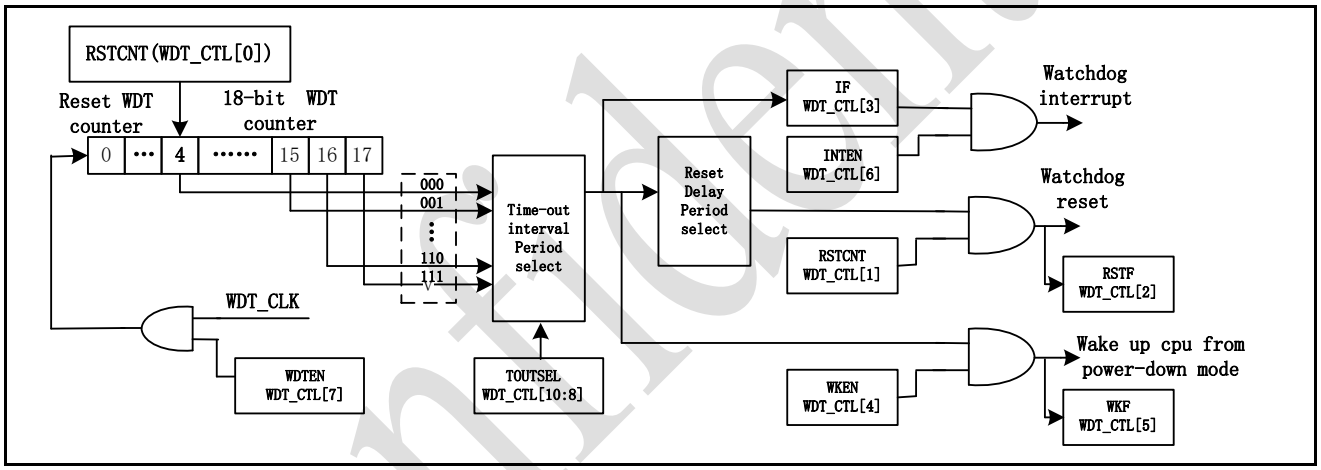

Figure 4-62 Watchdog Timer Block Diagram

4.9.4 Clock Control

The WDT clock control is shown in Figure 4-63.

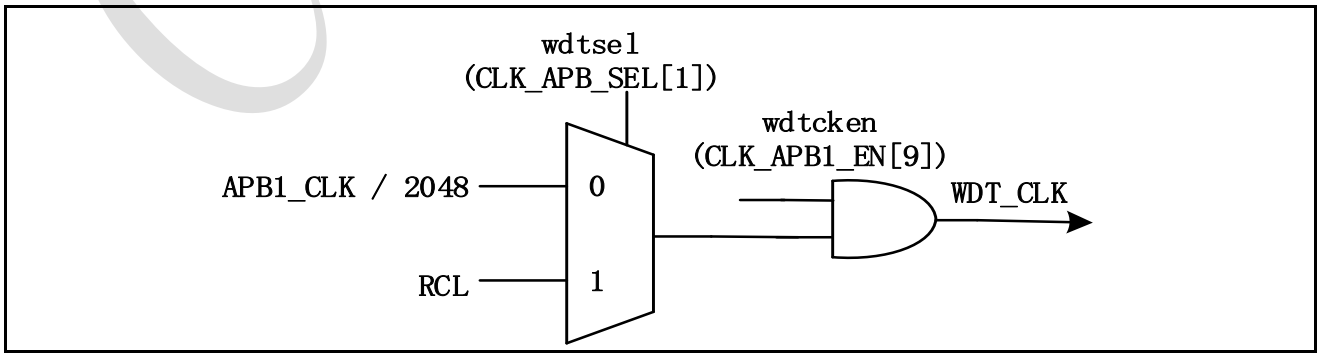

Figure 4-63 Watchdog Timer Clock Control

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4.9.5 Basic Configuration

The WDT peripheral clock is enabled in wdtcken(CLK_APB1_EN[9]) and clock source can be selected in wdtsel (CLK_APB_SEL[1]).

4.9.6 Functional Description

The WDT includes an 18-bit free running up counter with programmable time-out intervals.Table 4-9 shows the WDT time-out interval period selection and Figure 4-64 shows the WDT time-out interval and reset period timing.

4.9.6.1 WDT Time-out Flag

Setting WDTEN (WDT_CTL[7]) to 1 will enable the WDT function and the WDT counter to start counting up. There are eight time-out interval periods can be selected by setting TOUTSEL (WDT_CTL[10:8]). When the WDT up counter reaches the TOUTSEL (WDT_CTL[10:8]) setting, the WDT time-out interrupt will occur and then WDT time-out flag TOF (WDT_CTL[16]) will be set to 1 immediately.

4.9.6.2 WDT Time-out Interrupt Flag

Setting WDTEN (WDT_CTL[7]) to 1 will enable the WDT function and the WDT counter to start counting up. There are eight time-out interval period can be selected by setting TOUTSEL (WDT_CTL[10:8]). When the WDT up counter reaches the TOUTSEL (WDT_CTL[10:8]) setting, the WDT time-out interrupt will occur and then WDT time-out interrupt flag IF (WDT_CTL[3]) will be set to 1 immediatelywhen INTEN (WDT_CTL[6]) is set to 1.

4.9.6.3 WDT Reset Delay Period and Reset System

A specified T_{RSTD} reset delay period occurs when the IF (WDT_CTL[3]) is set to 1. User should set RSTCNT (WDT_CTL[0]) to reset the 18-bit WDT up counter value to avoid generating the WDT time-out reset signal before the T_{RSTD} reset delay period expires. Moreover, user should set RSTDSEL (WDT_ALTCTL [1:0]) to select reset delay period to clear WDT counter. If the WDT up counter value has not been cleared after the specified T_{RSTD} delay period expires, the WDT control will set RSTF (WDT_CTL[2]) to 1 if RSTEN (WDT_CTL[1]) bit is enabled, and then chip enters reset state immediately. Refer to Figure 4-64Watchdog Timer Time-out Interval and Reset Period Timing. The T_{RST} reset period will keep the last 63 WDT clocks and then chip restart executing program from reset vector (0x0000_0000). The RSTF (WDT_CTL[2]) will keep 1 after WDT time-out resets the chip. User can check RSTF (WDT_CTL[2]) via software to recognize if the system has been reset by WDT time-out reset or not.

Table 4-9 Watchdog Timer Time-out Interval Period Selection

TOUTSEL	Time-Out Interval Period TTIS	Reset Delay Period TRSTD
000	$2^4 * T_{WDT}$	(3/18/130/1026) * T_{WDT}
001	$2^6 * T_{WDT}$	(3/18/130/1026) * T_{WDT}
010	$2^8 * T_{WDT}$	(3/18/130/1026) * T_{WDT}
011	$2^{10} * T_{WDT}$	(3/18/130/1026) * T_{WDT}
100	$2^{12} * T_{WDT}$	(3/18/130/1026) * T_{WDT}

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101	$2^{14} * T_{WDT}$	(3/18/130/1026) * T_{WDT}
110	$2^{16} * T_{WDT}$	(3/18/130/1026) * T_{WDT}
111	$2^{18} * T_{WDT}$	(3/18/130/1026) * T_{WDT}

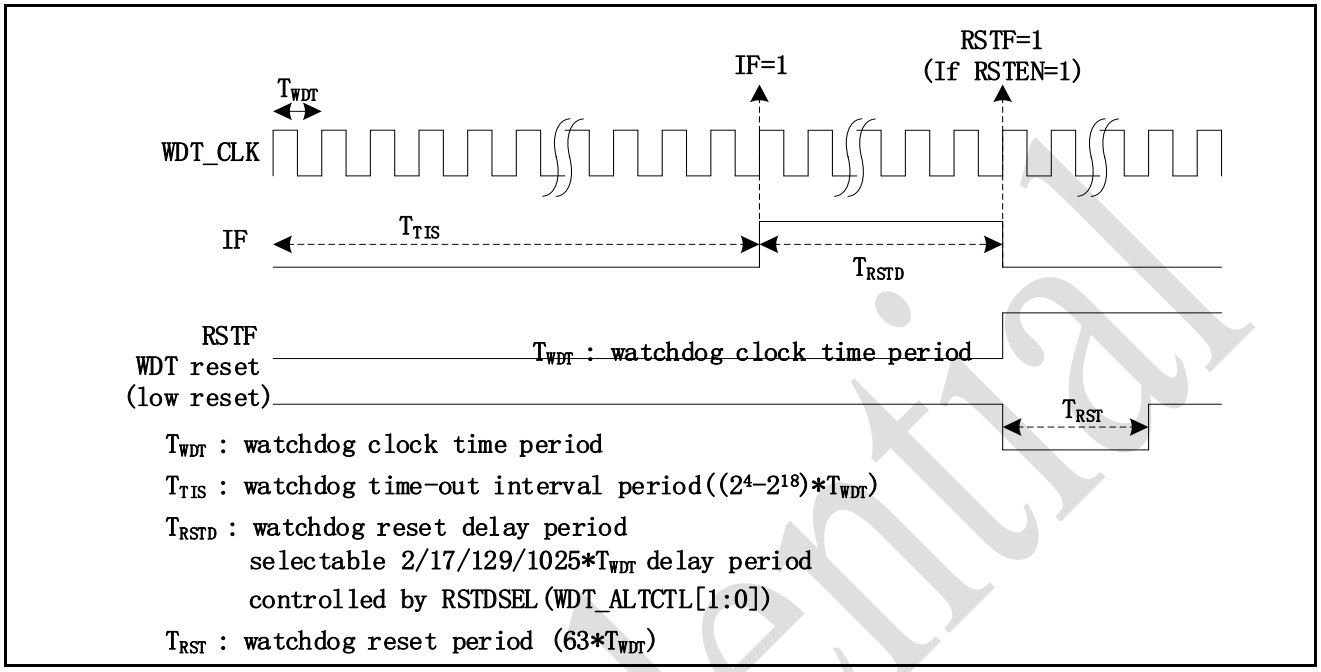

Figure 4-64 Watchdog Timer Time-out Interval and Reset Period Timing

4.9.6.4 WDT Wake-up

If WDT clock source is selected to be RCL or APB1_CLK / 2048, system can be woken up from Power-down mode while WDT time-out interrupt signal is generated and WKEN (WDT_CTL[4]) enabled. In the meanwhile, the WKF (WDT_CTL[5]) will be set to 1 automatically. User can check WKF (WDT_CTL[5]) status via software to recognize if the system has been woken up by WDT time-out interrupt or not.

4.9.7 WDT Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
WDT Base Address: **WDT_BA = 0x4000_6000**				
WDT_CTL	WDT_BA+0x00	R/W	WDT Control Register	0x0000_0700
WDT_ALTCTL	WDT_BA+0x04	R/W	WDT Alternative Control Register	0x0000_0000

4.9.8 WDT Register Description

4.9.8.1 WDT Control Register (WDT_CTL)

Register	Offset	R/W	Description	Reset Value
WDT_CTL	WDT_BA+0x00	R/W	WDT Control Register	0x0000_0700

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Bits	Descriptions	
[31]	ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect) 0 = ICE debug mode acknowledgement affects WDT counting. WDT up counter will be held while CPU is held by ICE. 1 = ICE debug mode acknowledgement disabled. WDT up counter will keep going no matter CPU is held by ICE or not. **Note**: This bit is write-protected. Refer to the SYS_REGLCTL register.
[30:17]	Reserved	Reserved.
[16]	TOF	WDT Time-out Flag This bit will be set to 1 while WDT up counter value reaches the selected WDT time-out interval 0 = WDT time-out interrupt does not occur. 1 = WDT time-out interrupt occurred. **Note**: This bit is cleared by writing 1 to it.
[15:11]	Reserved	Reserved.
[10:8]	TOUTSEL	WDT Time-out Interval Selection (Write Protect) These three bits select the time-out interval period for the WDT. 000 = 2^4 * WDT_CLK. 001 = 2^6 * WDT_CLK. 010 = 2^8 * WDT_CLK. 011 = 2^10 * WDT_CLK. 100 = 2^12 * WDT_CLK. 101 = 2^14 * WDT_CLK. 110 = 2^16 * WDT_CLK. 111 = 2^18 * WDT_CLK. **Note**: This bit is write-protected. Refer to the SYS_REGLCTL register.
[7]	WDTEN	WDT Enable Bit (Write Protect) 0 = WDT Disabled (This action will reset the internal up counter value). 1 = WDT Enabled. **Note1**: This bit is write-protected. Refer to the SYS_REGLCTL register.
[6]	INTEN	WDT Time-out Interrupt Enable Bit (Write Protect) If this bit is enabled, the WDT time-out interrupt signal is generated and inform to CPU. 0 = WDT time-out interrupt Disabled. 1 = WDT time-out interrupt Enabled. **Note**: This bit is write-protected. Refer to the SYS_REGLCTL register.
[5]	WKF	WDT Time-out Wake-up Flag (Write Protect) This bit indicates the interrupt wake-up flag status of WDT 0 = WDT does not cause chip wake-up. 1 = Chip wake-up from Idle or Power-down mode if WDT time-out interrupt signal generated. **Note1**: This bit is write-protected. Refer to the SYS_REGLCTL register. **Note2**: This bit is cleared by writing 1 to it.

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[4]	WKEN	WDT Time-out Wake-up Function Control (Write Protect) If this bit is set to 1, while WDT time-out interrupt flag IF (WDT_CTL[3]) is generated to 1 and interrupt enable bit INTEN (WDT_CTL[6]) is enabled, the WDT time-out interrupt signal will generate a wake-up trigger event to chip. 0 = Wake-up trigger event Disabled if WDT time-out interrupt signal generated. 1 = Wake-up trigger event Enabled if WDT time-out interrupt signal generated. **Note1**: This bit is write-protected. Refer to the SYS_REGLCTL register. **Note2**: Chip can be woken-up by WDT time-out interrupt signal generated only if WDT clock source is selected to RCL.
[3]	IF	WDT Time-out Interrupt Flag This bit will be set to 1 while WDT up counter value reaches the selected WDT time-out interval 0 = WDT time-out interrupt did not occur. 1 = WDT time-out interrupt occurred. **Note**: This bit is cleared by writing 1 to it.
[2]	RSTF	WDT Time-out Reset Flag This bit indicates the system has been reset by WDT time-out reset or not. 0 = WDT time-out reset did not occur. 1 = WDT time-out reset occurred. **Note**: This bit is cleared by writing 1 to it.
[1]	RSTEN	WDT Time-out Reset Enable Bit (Write Protect) Setting this bit will enable the WDT time-out reset function If the WDT up counter value has not been cleared after the specific WDT reset delay period expires. 0 = WDT time-out reset function Disabled. 1 = WDT time-out reset function Enabled. **Note**: This bit is write-protected. Refer to the SYS_REGLCTL register.
[0]	RSTCNT	Reset WDT Up Counter (Write Protect) 0 = No effect. 1 = Reset the internal 18-bit WDT up counter value. **Note1**: This bit is write-protected. Refer to the SYS_REGLCTL register. **Note2**: This bit will be automatically cleared by hardware.

4.9.8.2 WDT Alternative Control Register (WDT_ALTCTL)

Register	Offset	R/W	Description	Reset Value
WDT_ALTCTL	WDT_BA+0x04	R/W	WDT Alternative Control Register	0x0000_0000

Bits	Descriptions	
[31:2]	Reserved	Reserved.
[1:0]	RSTDSEL	WDT Reset Delay Selection (Write Protect) When WDT time-out happened, user has a time named WDT Reset Delay Period to clear WDT counter by setting RSTCNT (WDT_CTL[0]) to prevent WDT time-out reset happened. User can select a suitable setting of RSTDSEL for different WDT Reset Delay Period.

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		00 = WDT Reset Delay Period is 1026* WDT_CLK. 01 = WDT Reset Delay Period is 130 * WDT_CLK. 10 = WDT Reset Delay Period is 18 * WDT_CLK. 11 = WDT Reset Delay Period is 3 * WDT_CLK. **Note1**: This bit is write-protected. Refer to the SYS_REGLCTL register. **Note2**: This register will be reset to 0 if WDT time-out reset happens.

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4.10 Window Watchdog Timer (WWDT)

4.10.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

4.10.2 Feature

- 6-bit down counter value (CNTDAT) and 6-bit compare value (CMPDAT) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL) to program up to 11-bit prescale counter period of WWDT counter

4.10.3 Block Diagram

The WWDT block diagram is shown in Figure 4-65.

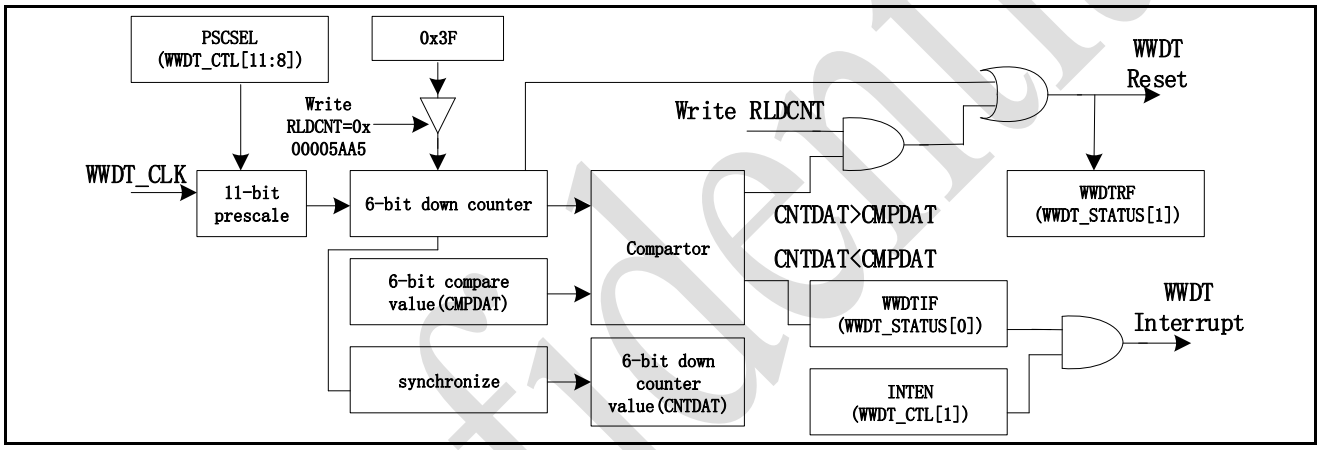

Figure 4-65 WWDT Block Diagram

4.10.4 Clock Control

The WWDT peripheral clock is enabled in wdtcken (CLK_APB1_EN[9]) and clock source can be selected in wwdtsel (CLK_APB_SEL[1]).

The WWDT clock control is shown in Figure 4-66.

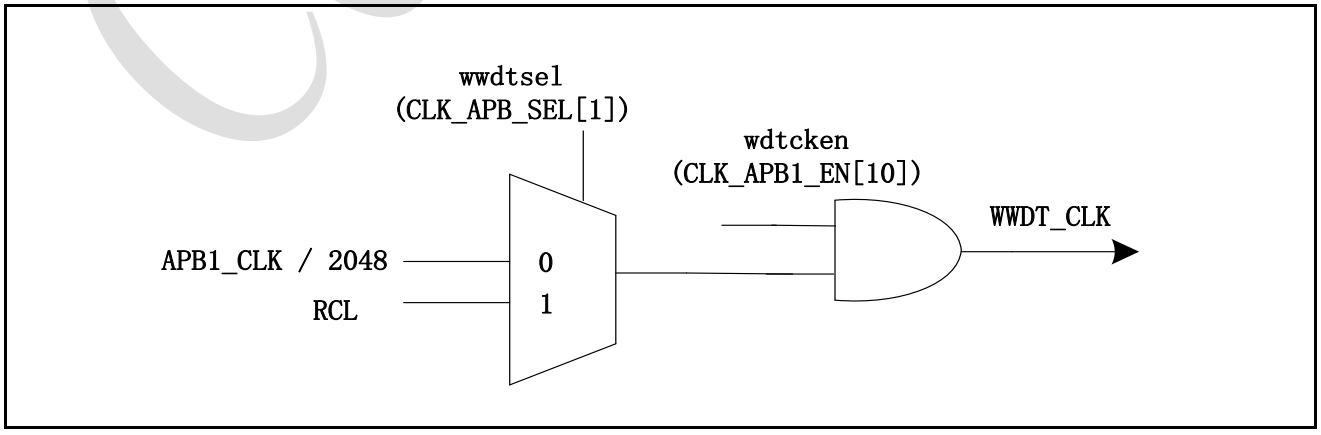

Figure 4-66 WWDT Clock Control

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4.10.5 Functional Description

The WWDT includes a 6-bit down counter with programmable prescale value to define different WWDT time-out intervals. The clock source of 6-bit WWDT is based on APB1_CLK / 2048 or 32 kHz internal low speed RC oscillator (RCL) with a programmable 11-bit prescale counter value which controlled by PSCSEL (WWDT_CTL[11:8]). Also, the correlate of PSCSEL (WWDT_CTL[11:8]) and prescale value are listed in Table 4-10.

Table 4-10 WWDT Prescaler Value Selection

PSCSEL	Prescaler Value	Max. Time-Out Period	Max. Time-Out Interval (WWDT_CLK=32 KHz)
0000	1	1 * 64 * T_{WWDT}	2ms
0001	2	2 * 64 * T_{WWDT}	4ms
0010	4	4 * 64 * T_{WWDT}	8ms
0011	8	8 * 64 * T_{WWDT}	16ms
0100	16	16 * 64 * T_{WWDT}	32ms
0101	32	32 * 64 * T_{WWDT}	64ms
0110	64	64 * 64 * T_{WWDT}	128ms
0111	128	128 * 64 * T_{WWDT}	256ms
1000	192	192 * 64 * T_{WWDT}	384ms
1001	256	256 * 64 * T_{WWDT}	512ms
1010	384	384 * 64 * T_{WWDT}	768ms
1011	512	512 * 64 * T_{WWDT}	1.024s
1100	768	768 * 64 * T_{WWDT}	1.536s
1101	1024	1024 * 64 * T_{WWDT}	2.048s
1110	1536	1536 * 64 * T_{WWDT}	3.072s
1111	2048	2048 * 64 * T_{WWDT}	4.096s

4.10.5.1 WWDT Counting

When the WWDTEN (WWDT_CTL[0]) is set, WWDT down counter will start counting from 0x3F to 0. To prevent program runs to disable WWDT counter counting unexpected, the WWDT_CTL register can only be written once after chip is powered on or reset. User cannot disable WWDT counter counting (WWDTEN), change counter prescale period (PSCSEL) or change window compare value (CMPDAT) while WWDTEN (WWDT_CTL[0]) has been enabled by user unless chip is reset.

4.10.5.2 WWDT Compare Match Flag

During down counting by the WWDT counter, the WWDTF (WWDT_STATUS[2]) is set to 1 while the WWDT counter value (CNTDAT) is equal to window compare value (CMPDAT) and WWDTF can be cleared by user.

4.10.5.3 WWDT Compare Match Interrupt Flag

During down counting by the WWDT counter, the WWDTIF (WWDT_STATUS[0]) is set to 1 while the WWDT counter value (CNTDAT) is equal to window compare value (CMPDAT) and

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INTEN(WWDT_CTL[1]) is set to 1. WWDTIF can be cleared by user;

4.10.5.4 WWDT Reset System

When WWDTIF (WWDT_STATUS[0]) is generated, user must reload WWDT counter value to 0x3F by writing 0x00005AA5 to WWDT_RLDCNT register, and also to prevent WWDT counter value reaching 0 and generating WWDT reset system signal to inform system reset. If current CNTDAT (WWDT_CNT[5:0]) is larger than CMPDAT (WWDT_CTL[21:16]) and user writes 0x00005AA5 to the WWDT_RLDCNT register, the WWDT reset system signal will be generated immediately to cause chip reset.

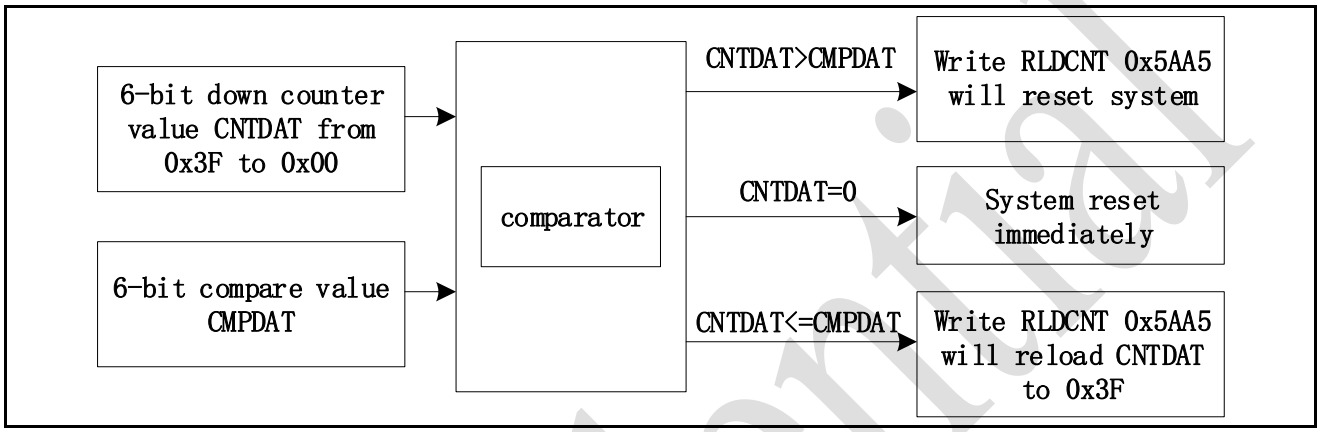

Figure 4-67 WWDT Reset and Reload Behavior

4.10.5.5 WWDT Window Setting Limitation

When user writes 0x00005AA5 to WWDT_RLDCNT register to reload WWDT counter value to 0x3F, it needs 3 WWDT clocks to sync the reload command to actually perform reload action. Notice that if user set PSCSEL (WWDT_CTL[11:8]) to 0000, the counter prescale value should be as 1, and the CMPDAT (WWDT_CTL[21:16]) must be larger than 2. Otherwise, writing WWDT_RLDCNT register to reload WWDT counter value to 0x3F is unavailable, WWDTIF (WWDT_STATUS[0]) is generated, and WWDT reset system event always happened.

Table 4-11 CMPDAT Setting Limitation

PSCSEL	Prescale	Value
0000	1	0x03 ~ 0x3F
0001	2	0x02 ~ 0x3F
others	others	0x00 ~ 0x3F

4.10.6 WWDT Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
WWDT Base Address: **WWDT_BA = 0x4000_4100**				
WWDT_RLDCNT	WWDT_BA+0x00	W	WWDT Reload Counter Register	0x0000_0000
WWDT_CTL	WWDT_BA+0x04	R/W	WWDT Control Register	0x003F_0800
WWDT_STATUS	WWDT_BA+0x08	R/W	WWDT Status Register	0x0000_0000

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WWDT_CNT	WWDT_BA+0x0C	R	WWDT Counter Value Register	0x0000_003F

4.10.7 WWDT Register Description

4.10.7.1 WWDT Reload Counter Register (WWDT_RLDCNT)

Register	Offset	R/W	Description	Reset Value
WWDT_RLDCNT	WWDT_BA+0x00	W	WWDT Reload Counter Register	0x0000_0000

Bits	Descriptions	
[31:0]	RLDCNT	WWDT Reload Counter Register Writing 0x00005AA5 to this register will reload the WWDT counter value to 0x3F. **Note**: User can only write WWDT_RLDCNT register to reload WWDT counter value when current WWDT counter value is between 0 and CMPDAT (WWDT_CTL[21:16]). If user writes WWDT_RLDCNT when current WWDT counter value is larger than CMPDAT, WWDT reset signal will generate immediately.

4.10.7.2 WWDT Control Register (WWDT_CTL)

Register	Offset	R/W	Description	Reset Value
WWDT_CTL	WWDT_BA+0x04	R/W	WWDT Control Register	0x003F_0800

Bits	Descriptions	
[31]	ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit 0 = ICE debug mode acknowledgement effects WWDT counting. WWDT down counter will be held while CPU is held by ICE. 1 = ICE debug mode acknowledgement disabled. WWDT down counter will keep going no matter CPU is held by ICE or not.
[30:22]	Reserved	Reserved
[21:16]	CMPDAT	WWDT Window Compare Bits Set this register to adjust the valid reload window. **Note**: User can only write WWDT_RLDCNT register to reload WWDT counter value when current WWDT counter value between 0 and CMPDAT. If user writes WWDT_RLDCNT register when current WWDT counter value larger than CMPDAT, WWDT reset signal will generate immediately.
[15:12]	Reserved	Reserved
[11:8]	PSCSEL	WWDT Counter Prescale Period Select Bits 0000 = Pre-scale is 1; Max time-out period is 1 * 64 * WWDT_CLK. 0001 = Pre-scale is 2; Max time-out period is 2 * 64 * WWDT_CLK. 0010 = Pre-scale is 4; Max time-out period is 4 * 64 * WWDT_CLK. 0011 = Pre-scale is 8; Max time-out period is 8 * 64 * WWDT_CLK. 0100 = Pre-scale is 16; Max time-out period is 16 * 64 * WWDT_CLK. 0101 = Pre-scale is 32; Max time-out period is 32 * 64 * WWDT_CLK.

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		0110 = Pre-scale is 64; Max time-out period is 64 * 64 * WWDT_CLK. 0111 = Pre-scale is 128; Max time-out period is 128 * 64 * WWDT_CLK. 1000 = Pre-scale is 192; Max time-out period is 192 * 64 * WWDT_CLK. 1001 = Pre-scale is 256; Max time-out period is 256 * 64 * WWDT_CLK. 1010 = Pre-scale is 384; Max time-out period is 384 * 64 * WWDT_CLK. 1011 = Pre-scale is 512; Max time-out period is 512 * 64 * WWDT_CLK. 1100 = Pre-scale is 768; Max time-out period is 768 * 64 * WWDT_CLK. 1101 = Pre-scale is 1024; Max time-out period is 1024 * 64 * WWDT_CLK. 1110 = Pre-scale is 1536; Max time-out period is 1536 * 64 * WWDT_CLK. 1111 = Pre-scale is 2048; Max time-out period is 2048 * 64 * WWDT_CLK.
[7:2]	Reserved	Reserved
[1]	INTEN	WWDT Interrupt Enable Bit If this bit is enabled, the WWDT counter compare match interrupt signal is generated and inform to CPU. 0 = WWDT counter compare match interrupt Disabled. 1 = WWDT counter compare match interrupt Enabled.
[0]	WWDTEN	WWDT Enable Bit Set this bit to enable WWDT counter counting. 0 = WWDT counter is stopped. 1 = WWDT counter is starting counting.

4.10.7.3 WWDT Status Register (WWDT_STATUS)

Register	Offset	R/W	Description	Reset Value
WWDT_STATUS	WWDT_BA+0x08	R/W	WWDT Status Register	0x0000_0000

Bits	Descriptions	
[31:3]	Reserved	Reserved
[2]	WWDTF	WWDT Compare Match Flag This bit indicates the flag status of WWDT while WWDT counter value matches CMPDAT (WWDT_CTL[21:16]). 0 = No effect. 1 = WWDT counter value matches CMPDAT. **Note**: This bit is cleared by writing 1 to it.
[1]	WWDTRF	WWDT Timer-out Reset Flag This bit indicates the system has been reset by WWDT time-out reset or not. 0 = WWDT time-out reset did not occur. 1 = WWDT time-out reset occurred. **Note**: This bit is cleared by writing 1 to it.
[0]	WWDTIF	WWDT Compare Match Interrupt Flag This bit indicates the interrupt flag status of WWDT while WWDT counter value matches CMPDAT (WWDT_CTL[21:16]). 0 = No effect. 1 = WWDT counter value matches CMPDAT.

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		Note: This bit is cleared by writing 1 to it.

4.10.7.4 WWDT Counter Value Register (WWDT_CNT)

Register	Offset	R/W	Description	Reset Value
WWDT_CNT	WWDT_BA+0x0C	R	WWDT Counter Value Register	0x0000_003F

Bits	Descriptions	
[31:6]	Reserved	Reserved
[5:0]	CNTDAT	WWDT Counter Value CNTDAT will be updated continuously to monitor 6-bit WWDT down counter value.

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4.11 UART Controller (UART)

4.11.1 Overview

The PAN2025 provides two channels of Universal Asynchronous Receiver/Transmitters (UART). The UART0/1/2/3 performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART0/1/2/3 channel supports five types of interrupts. The UART0/1/2/3 has 8 bytes Receiver/Transmitter FIFO.

4.11.2 Features

- Full duplex, asynchronous communication
- Separates receive/transmit 8/8 bytes entry FIFO for data payloads
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UART_TOUT[15:8] register
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit 5, 6, 7, 8 character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit 1, 1.5, or 2 stop bit generation

4.11.3 Block Diagram

The UART0/1/2/3 clock control and block diagram are shown in Figure 4-68.

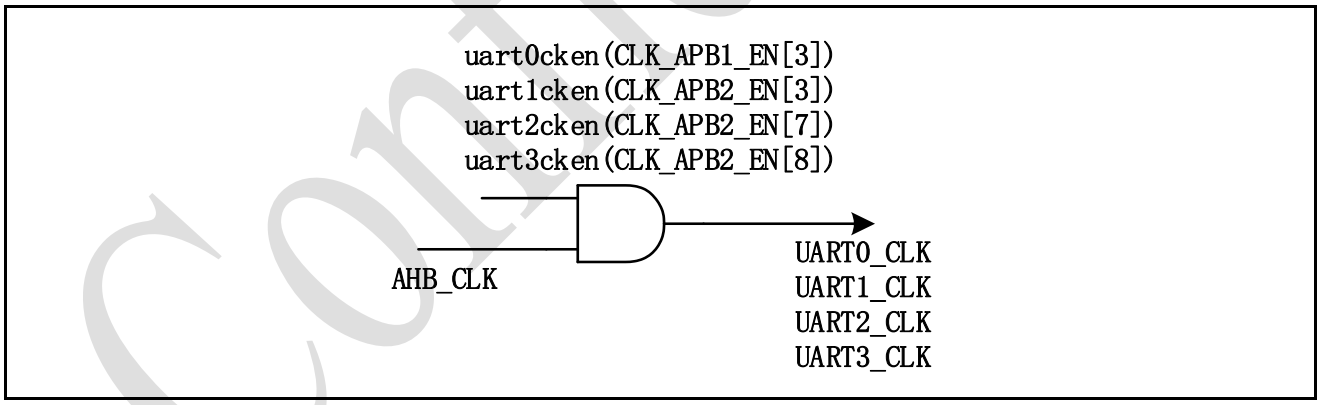

Figure 4-68 UART0/1/2/3 Controller Clock Control

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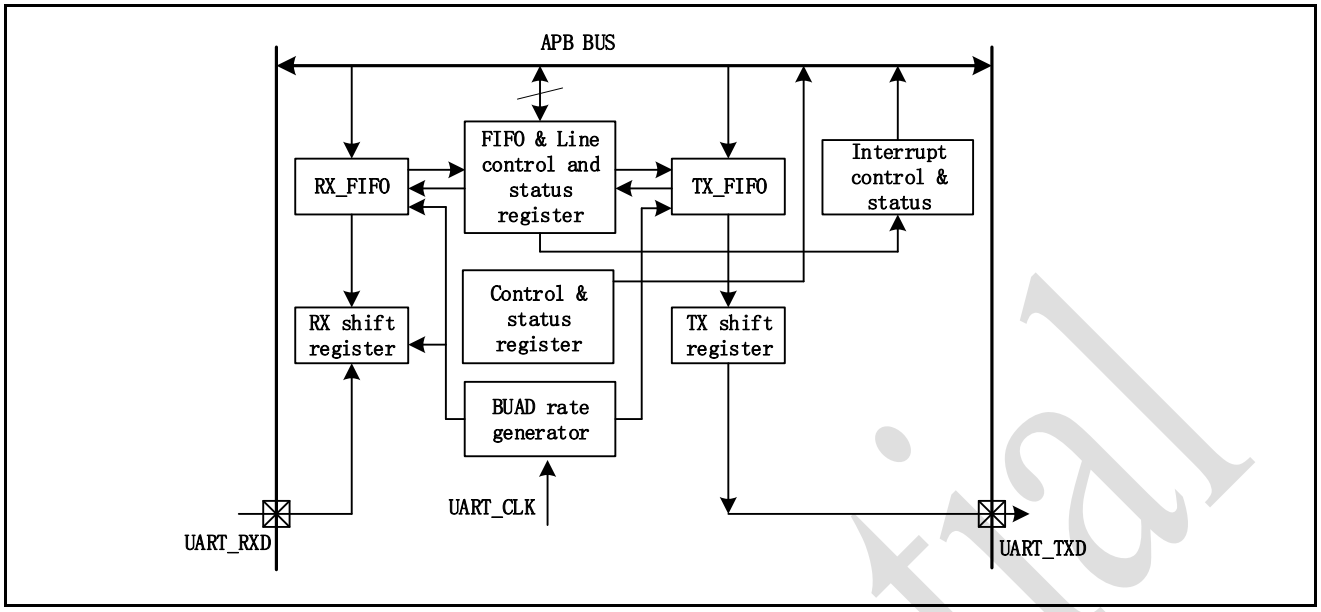

Figure 4-69 UART Controller Block Diagram

Each block is described in detail as follows:

TX_FIFO/TX_BUF

The UART transmitter is buffered with a 8-byte FIFO to reduce the number of interrupts presented to the CPU.

RX_FIFO/RX_BUF

The UART receiver is buffered with a 8-byte FIFO (plus three error bits per byte) to reduce the number of interrupts presented to the CPU.

TX shift Register

This block is shifting the transmitting data out serial control block.

RX Shift Register

This block is shifting the receiving data in serial control block.

Baud Rate Generator

Divide the external clock by the divisor to get the desired baud rate clock. Refer to baud rate equation.

FIFO & Line Control and Status Register

This field is register set that including the FIFO control registers (UART_FIFO), FIFO status registers (UART_FIFOSTS), and line control register (UART_LINE) for transmitter and receiver. The time-out control register (UART_TOUT) identifies the condition of time-out interrupt.

Interrupt Control and Status Register

There are five types of interrupts, transmitter FIFO empty interrupt (THERIF), receiver data available interrupt (RDAIF), receive line status interrupt (parity error or framing error or break interrupt)

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(RLSIF), time-out interrupt (RXTOINT), Buffer error interrupt (BUFERRINT). Interrupt enabling register (UART_INTEN) enables or disables the responding interrupt and interrupt status register (UART_INTSTS) identifying the occurrence of the responding interrupt.

4.11.4 Basic Configuration

The UART Controller function pins are configured in SYS_P0_MFP/SYS_P1_MFP/SYS_P5_MFP registers for UART0, configured in SYS_P1_MFP/ SYS_P2_MFP/ SYS_P4_MFP registers for UART1, configured in SYS_P1_MFP/ SYS_P2_MFP registers for UART2 and configured in SYS_P0_MFP/ SYS_P3_MFP registers for UART3.

The UART Controller clock are enabled in uart0cken (CLK_APB1_EN[3]) for UART0, uart1cken (CLK_APB2_EN[3]) for UART1, uart2cken (CLK_APB2_EN[7]) for UART2 and uart3cken (CLK_APB2_EN[8]) for UART3.

4.11.5 Functional Description

The UART Controller supports UART data transmit and receive mode.

4.11.5.1 UART Controller Baud Rate Generator

The UART Controller includes a programmable baud rate generator capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UARTx_CLK / 2 * [BRD + 1].

Table 4-12 Controller Baud Rate Parameter Setting Table

UART Peripheral Clock = 48 MHz	
Baud Rate	**BRD**
921600	25
460800	51
230400	103
115200	207
57600	416
38400	624
19200	1249
9600	2499
4800	4999

4.11.5.2 UART Controller FIFO Control and Status

The UART0/1/2/3 Controller is built-in with an 8 bytes transmitter FIFO (TX_FIFO) and an 8 bytes receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU. The CPU can read the status of the UART0/1/2/3 at any time during operation. The reported status information includes the type and condition of the transfer operations being performed by the UART0/1/2/3, as well as 3 error conditions (parity error, framing error, break interrupt) probably occur while receiving data.

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4.11.5.3 UART Controller Interrupt and Status

UART Controller supports 5 types of interrupts. The interrupts are listed as following:

- Receiver threshold level reached interrupt (RDAINT)
- Transmitter FIFO empty interrupt (THREINT)
- Line status interrupt (parity error, frame error or break interrupt) (RLSINT)
- Receiver buffer time-out interrupt (RXTOINT)
- Buffer error interrupt (BUFERRINT)

Table 4-13 describes the interrupt sources and flags. The interrupt is generated when the interrupt flag is generated and the interrupt enable bit is set. User must clear the interrupt flag after the interrupt is generated.

Table 4-13 Controller Interrupt Source and Flag

Interrupt Source	Interrupt Indicator	Interrupt Enable Bit	Interrupt Flag	Flag Cleared By
Receive Data Available Interrupt	RDAINT	RDAIEN	RDAIF	Read UART_DAT
Transmit Holding Register Empty Interrupt	THREINT	THREIEN	THREIF	Write UART_DAT
Receive Line Status Interrupt	RLSINT	RLSIEN	RLSIF = (BIF or FEF or PEF)	Writing '1' to BIF/FEF/ PEF
			RLSIF = ADDRDETF	Writing '1' to ADDRDETF
RX Time-out Interrupt	RXTOINT	RXTOIEN	RXTOIF	Read UART_DAT
Buffer Error Interrupt	BUFERRINT	BUFERRIEN	BUFERRIF = (TXOVIF or RXOVIF)	Writing '1' to TXOVIF / RXOVIF

4.11.5.4 UART Function Mode

The UART0/1/2/3 Controller provides UART function. The UART baud rate is up to 1 Mbps.

The UART0/1/2/3 provides full-duplex and asynchronous communications. The UART0/1/2/3 transmitter and receiver contain 8 bytes FIFO for payloads. User can program receiver buffer trigger level and receiver buffer time-out detection for receiver. The transmitting data delay time between the last stop and the next start bit can be programmed by setting DLY (UART_TOUT [15:8]) register.

Table 4-14 Line Control of Word and Stop Length Setting

NSB (UART_LINE[2])	WLS (UART_LINE[1:0])	Word Length (Bit)	Stop Length (Bit)
0	00	5	1
0	01	6	1
0	10	7	1
0	11	8	1
1	00	5	1.5
1	01	6	2

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1	10	7	2
1	11	8	2

Table 4-15 Line Control of Parity Bit Setting

Parity Type	SPE (UART_LINE[5])	EPE (UART_LINE[4])	PBE (UART_LINE[3])	Description
No Parity	x	x	0	No parity bit output.
Odd Parity	0	0	1	Odd Parity is calculated by adding all the "1's" in a data stream and adding a parity bit to the total bits, to make the total count an odd number.
Even Parity	0	1	1	Even Parity is calculated by adding all the "1's" in a data stream and adding a parity bit to the total bits, to make the count an even number.
Forced Mask Parity	1	0	1	Parity bit always logic 1. Parity bit on the serial byte is set to "1" regardless of total number of "1's" (even or odd counts).
Forced Space Parity	1	1	1	Parity bit always logic 0. Parity bit on the serial byte is set to "0" regardless of total number of "1's" (even or odd counts).

4.11.6 UART Register Map

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
UART Base Address: **UART0_BA = 0x4000_3000** **UART1_BA = 0x4001_3000** **UART2_BA = 0x4001_7000** **UART3_BA = 0x4001_8000**				
UART_DAT x = 0, 1, 2, 3	UARTx_BA+0x00	R/W	UART Receive/Transmit Buffer Register	Undefined
UART_INTEN x = 0, 1, 2, 3	UARTx_BA+0x04	R/W	UART Interrupt Enable Register	0x0000_0000
UART_FIFO x = 0, 1, 2, 3	UARTx_BA+0x08	R/W	UART FIFO Control Register	0x0000_0000
UART_LINE x = 0, 1, 2, 3	UARTx_BA+0x0C	R/W	UART Line Control Register	0x0000_0003

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UART_FIFOSTS x = 0, 1, 2, 3	UARTx_BA+0x18	R/W	UART FIFO Status Register	0x1040_4000
UART_INTSTS x = 0, 1, 2, 3	UARTx_BA+0x1C	R/W	UART Interrupt Status Register	0x0000_0002
UART_TOUT x = 0, 1, 2, 3	UARTx_BA+0x20	R/W	UART Time-out Register	0x0000_0028
UART_BAUD x = 0, 1, 2, 3	UARTx_BA+0x24	R/W	UART Baud Rate Divisor Register	0x0000_0000

4.11.7 UART Register Description

4.11.7.1 Receive/Transmit Buffer Register (UART_DAT)

Register	Offset	R/W	Description	Reset Value
UART_DAT x = 0, 1, 2, 3	UARTx_BA+0x00	R/W	UART Receive/Transmit Buffer Register	Undefined

Bits	Description	
[31:8]	Reserved	Reserved.
[7:0]	DAT	Receiving/Transmit Buffer Write Operation: By writing one byte to this register, the data byte will be stored in transmitter FIFO. The UART Controller will send out the data stored in transmitter FIFO top location through the UART_TXD. Read Operation: By reading this register, the UART will return an 8-bit data received from receiving FIFO.

4.11.7.2 Interrupt Enable Register (UART_INTEN)

Register	Offset	R/W	Description	Reset Value
UART_INTEN x = 0, 1, 2, 3	UARTx_BA+0x04	R/W	UART Interrupt Enable Register	0x0000_0000

Bits	Description	
[31:12]	Reserved	Reserved.
[11]	TOCNTEN	Time-out Counter Enable Bit 0 = Time-out counter disabled. 1 = Time-out counter enabled.
[10:6]	Reserved	Reserved.
[5]	BUFERRIEN	Buffer Error Interrupt Enable Bit 0 = Buffer Error Interrupt Masked disabled. 1 = Buffer Error Interrupt Masked enabled.
[4]	RXTOIEN	RX Time-out Interrupt Enable Bit

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		0 = RXTOINT disabled. 1 = RXTOINT enabled.
[3]	Reserved	Reserved.
[2]	RLSIEN	Receive Line Status Interrupt Enable Bit 0 = RLSINT disabled 1 = RLSINT enabled.
[1]	THREIEN	Transmit Holding Register Empty Interrupt Enable Bit 0 = THREINT disabled. 1 = THREINT enabled.
[0]	RDAIEN	Receive Data Available Interrupt Enable Bit 0 = RDAINT disabled. 1 = RDAINT enabled.

4.11.7.3 FIFO Control Register (UART_FIFO)

Register	Offset	R/W	Description	Reset Value
UART_FIFO x = 0, 1, 2, 3	UARTx_BA+0x08	R/W	UART FIFO Control Register	0x0000_0000

Bits	Description	
[31:8]	Reserved	Reserved.
[7:4]	RFITL	RX FIFO Interrupt (RDAINT) Trigger Level (Only Available in UART0) When the number of bytes in the receive FIFO equals the RFITL then the RDAIF will be set (if RDAIEN in UART_INTEN register is enabled, an interrupt will generate). 0000 = RX FIFO Interrupt Trigger Level is 1 byte. 0001 = RX FIFO Interrupt Trigger Level is 2 bytes. 0010 = RX FIFO Interrupt Trigger Level is 4 bytes. 0011 = RX FIFO Interrupt Trigger Level is 6 bytes. Other = Reserved.
[3]	Reserved	Reserved.
[2]	TXRST	TX Field Software Reset When TX_RST is set, all the byte in the transmit FIFO and TX internal state machine are be cleared. 0 = No effect. 1 = Reset TX internal state machine and pointers reset. Note: This bit will auto clear needs at least 3 UART Controller peripheral clock cycles.
[1]	RXRST	RX Field Software Reset When RX_RST is set, all the byte in the receiver FIFO and RX internal state machine are cleared. 0 = No effect. 1 = Reset RX internal state machine and pointers reset. Note: This bit will auto clear needs at least 3 UART Controller peripheral clock cycles.
[0]	Reserved	Reserved.

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4.11.7.4 Line Control Register (UART_LINE)

Register	Offset	R/W	Description	Reset Value
UART_LINE x = 0, 1, 2, 3	UARTx_BA+0x0C	R/W	UART Line Control Register	0x0000_0003

Bits	Description	
[31:7]	Reserved	Reserved.
[6]	BCB	Break Control Bit When this bit is set to logic 1, the serial data output (TX) is forced to the Spacing State (logic 0). This bit acts only on TX and has no effect on the transmitter logic. 0 = Break control disabled. 1 = Break control enabled.
[5]	SPE	Stick Parity Enable Bit 0 = Stick parity disabled. 1 = If PBE (UART_LINE[3]) and EPE (UART_LINE[4]) are logic 1, the parity bit is transmitted and checked as logic 0. If PBE (UART_LINE[3]) is 1 and EPE (UART_LINE[4]) is 0 then the parity bit is transmitted and checked as 1.
[4]	EPE	Even Parity Enable Bit 0 = Odd number of logic 1's is transmitted and checked in each word. 1 = Even number of logic 1's is transmitted and checked in each word. This bit has effect only when PBE (UART_LINE[3]) is set.
[3]	PBE	Parity Bit Enable Bit 0 = No parity bit. 1 = Parity bit is generated on each outgoing character and is checked on each incoming data.
[2]	NSB	Number of "STOP Bit" 0 = One "STOP bit" is generated in the transmitted data. 1 = When select 5-bit word length, 1.5 "STOP bit" is generated in the transmitted data. When select 6-, 7- and 8-bit word length, 2 "STOP bit" is generated in the transmitted data.
[1:0]	WLS	Word Length Select Bit 00 = Word length is 5-bit. 01 = Word length is 6-bit. 10 = Word length is 7-bit. 11 = Word length is 8-bit.

4.11.7.5 FIFO Status Register (UART_FIFOSTS)

Register	Offset	R/W	Description	Reset Value
UART_FIFOSTS x = 0, 1, 2, 3	UARTx_BA+0x18	R/W	UART FIFO Status Register	0x1040_4000

Bits	Description

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[31:29]	Reserved	Reserved.
[28]	TXEMPTYF	Transmitter Empty Flag (Read Only) This bit is set by hardware when TX FIFO (UART_DAT) is empty and the STOP bit of the last byte has been transmitted. 0 = TX FIFO is not empty. 1 = TX FIFO is empty. Note: This bit is cleared automatically when TX FIFO is not empty or the last byte transmission has not completed.
[27:25]	Reserved	Reserved.
[24]	TXOVIF	TX Overflow Error Interrupt Flag If TX FIFO (UART_DAT) is full, an additional write to UART_DAT will cause this bit to logic 1. 0 = TX FIFO does not overflow. 1 = TX FIFO overflows. Note: This bit is cleared by writing 1 to it.
[23]	TXFULL	Transmitter FIFO Full (Read Only) This bit indicates TX FIFO full or not. 0 = TX FIFO is not full. 1 = TX FIFO is full. Note: This bit is set when the number of usage in TX FIFO Buffer is equal to 8, otherwise is cleared by hardware.
[22]	TXEMPTY	Transmitter FIFO Empty (Read Only) This bit indicates TX FIFO empty or not. 0 = TX FIFO is not empty. 1 = TX FIFO is empty. Note: When the last byte of TX FIFO has been transferred to Transmitter Shift Register, hardware sets this bit high. It will be cleared when writing data into THR (TX FIFO not empty).
[21:19]	Reserved	Reserved.
[18:16]	TXPTR	TX FIFO Pointer (Read Only) This field indicates the TX FIFO Buffer Pointer. When CPU writes one byte into UART_DAT, TXPTR increases one. When one byte of TX FIFO is transferred to Transmitter Shift Register, TXPTR decreases one. The Maximum value shown in TXPTR is 7. When the using level of TX FIFO Buffer equal to 8, the TXFULL bit is set to 1 and TXPTR will show 0. As one byte of TX FIFO is transferred to Transmitter Shift Register, the TXFULL bit is cleared to 0 and TXPTR will show 7.
[15]	RXFULL	Receiver FIFO Full (Read Only) This bit initiates RX FIFO full or not. 0 = RX FIFO is not full. 1 = RX FIFO is full. Note: This bit is set when the number of usage in RX FIFO Buffer is equal to 8, otherwise is cleared by hardware.
[14]	RXEMPTY	Receiver FIFO Empty (Read Only) This bit initiate RX FIFO empty or not.

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		0 = RX FIFO is not empty. 1 = RX FIFO is empty. Note: When the last byte of RX FIFO has been read by CPU, hardware sets this bit high. It will be cleared when UART receives any new data.
[13:11]	Reserved	Reserved.
[10:8]	RXPTR	RX FIFO Pointer (Read Only) This field indicates the RX FIFO Buffer Pointer. When UART receives one byte from external device, RXPTR increases one. When one byte of RX FIFO is read by CPU, RXPTR decreases one. The Maximum value shown in RXPTR is 7. When the using level of RX FIFO Buffer equal to 8, the RXFULL bit is set to 1 and RXPTR will show 0. As one byte of RX FIFO is read by CPU, the RXFULL bit is cleared to 0 and RXPTR will show 7.
[7]	Reserved	Reserved.
[6]	BIF	Break Interrupt Flag (Read Only) This bit is set to logic 1 whenever the received data input (RX) is held in the “spacing state” (logic 0) for longer than a full word transmission time (that is, the total time of “start bit” + data bits + parity + stop bits). 0 = No Break interrupt is generated. 1 = Break interrupt is generated. Note: This bit is read only, but software can write 1 to clear it.
[5]	FEF	Framing Error Flag (Read Only) This bit is set to logic 1 whenever the received character does not have a valid “stop bit” (that is, the stop bit follows the last data bit or parity bit is detected as logic 0). 0 = No framing error is generated. 1 = Framing error is generated. Note: This bit is read only, but can be cleared by writing ‘1’ to it .
[4]	PEF	Parity Error Flag (Read Only) This bit is set to logic 1 whenever the received character does not have a valid “parity bit”. 0 = No parity error is generated. 1 = Parity error is generated.. Note: This bit is read only, but can be cleared by writing ‘1’ to it.
[3:1]	Reserved	Reserved.
[0]	RXOVIF	RX Overflow Error Interrupt Flag This bit is set when RX FIFO overflow. If the number of bytes of received data is greater than RX_FIFO (UART_DAT) size, 8 bytes this bit will be set. 0 = RX FIFO did not overflow. 1 = RX FIFO overflowed. Note: This bit is cleared by writing 1 to it.

4.11.7.6 Interrupt Status Control Register (UART_INTSTS)

Register	Offset	R/W	Description	Reset Value
UART_INTSTS	UARTx_BA+0x1C	R/W	UART Interrupt Status Register	0x0000_0002

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x = 0, 1, 2, 3				

Bits	Description	
[31:14]	Reserved	Reserved.
[13]	BUFERRINT	Buffer Error Interrupt Indicator (Read Only) This bit is set if BUFERRIEN (UART_INTEN[5]) and BUFERRIF (UART_INTSTS[5]) are both set to 1. 0 = No buffer error interrupt is generated. 1 = buffer error interrupt is generated.
[12]	RXTOINT	Time-out Interrupt Indicator (Read Only) This bit is set if RXTOIEN (UART_INTEN[4]) and RXTOIF (UART_INTSTS[4]) are both set to 1. 0 = No Time-out interrupt is generated. 1 = Time-out interrupt is generated.
[11]	Reserved	Reserved.
[10]	RLSINT	Receive Line Status Interrupt (Read Only) This bit is set if RLSIEN (UART_INTEN[2]) and RLSIF (UART_INTSTS[2]) are both set to 1. 0 = No RLS interrupt is generated. 1 = RLS interrupt is generated.
[9]	THREINT	Transmit Holding Register Empty Interrupt Indicator (Read Only) This bit is set if THREIEN (UART_INTEN[1]) and THREIF (UART_INTSTS[1]) are both set to 1. 0 = No THRE interrupt is generated. 1 = THRE interrupt is generated.
[8]	RDAINT	Receive Data Available Interrupt Indicator (Read Only) This bit is set if RDAIEN (UART_INTEN[0]) and RDAIF (UART_INTSTS[0]) are both set to 1. 0 = No RDA interrupt is generated. 1 = RDA interrupt is generated.
[7:6]	Reserved	Reserved.
[5]	BUFERRIF	Buffer Error Interrupt Flag (Read Only) This bit is set when the TX/RX FIFO overflow flag (TXOVIF (UART_FIFOSTS[24] or RXOVIF(UART_FIFOSTS[0])) is set. When BUFERRIF (UART_INTSTS[5]) is set, the transfer is not correct. If BUFERRIEN (UART_INTEN[5]) is enabled, the buffer error interrupt will be generated. 0 = No buffer error interrupt flag is generated. 1 = Buffer error interrupt flag is generated. Note: This bit is read only and reset to 0 when all bits of TXOVIF (UART_FIFOSTS[24]) and RXOVIF (UART_FIFOSTS[0]) are cleared.
[4]	RXTOIF	Time-out Interrupt Flag (Read Only) This bit is set when the RX FIFO is not empty and no activities occurred in the RX FIFO and the time-out counter equal to TOIC (UARTTOUT[7:0]). If RXTOIEN (UART_INTEN [4]) is

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		enabled, the Tout interrupt will be generated. 0 = No Time-out interrupt flag is generated. 1 = Time-out interrupt flag is generated. Note: This bit is read only and user can read UART_DAT (RX is in active) to clear it.
[3]	Reserved	Reserved.
[2]	RLSIF	Receive Line Interrupt Flag (Read Only) This bit is set when the RX receive data have parity error, framing error or break error (at least one of 3 bits, BIF, FEF and PEF, is set). If RLSIEN (UART_INTEN [2]) is enabled, the RLS interrupt will be generated. 0 = No RLS interrupt flag is generated. 1 = RLS interrupt flag is generated. Note1: In RS-485 function mode, this field is set including “receiver detects and receives address byte character (bit 9 = 1) bit". At the same time, the bit of ADDRDETF (UART_FIFOSTS[3]) is also set. Note2: This bit is read only and reset to 0 when all bits of BIF (UART_FIFOSTS[6]), FEF (UART_FIFOSTS[5]), PEF (UART_FIFOSTS[4]) and ADDRDETF (UART_FIFOSTS[3]) are cleared.
[1]	THREIF	Transmit Holding Register Empty Interrupt Flag (Read Only) This bit is set when the last data of TX FIFO is transferred to Transmitter Shift Register. If THREIEN (UART_INTEN [1]) is enabled, the THRE interrupt will be generated. 0 = No THRE interrupt flag is generated. 1 = THRE interrupt flag is generated. Note: This bit is read only and it will be cleared when writing data into UART_DAT (TX FIFO not empty).
[0]	RDAIF	Receive Data Available Interrupt Flag (Read Only) When the number of bytes in the RX FIFO equals the RFITL(UART_FIFO[7:4]) then the RDAIF(UART_INTSTS[0]) will be set. If RDAIEN (UART_INTEN [0]) is enabled, the RDA interrupt will be generated. 0 = No RDA interrupt flag is generated. 1 = RDA interrupt flag is generated. Note: This bit is read only and it will be cleared when the number of unread bytes of RX FIFO drops below the threshold level (RFITL (UART_FIFO[7:4])).

4.11.7.7 Time-out Register (UART_TOUT)

Register	Offset	R/W	Description	Reset Value
UART_TOUT x = 0, 1, 2, 3	UARTx_BA+0x20	R/W	UART Time-out Register	0x0000_0028

Bits	Description	
[31:16]	Reserved	Reserved.
[15:8]	DLY	TX Delay Time Value This field is used to program the transfer delay time between the last stop bit and next start bit.

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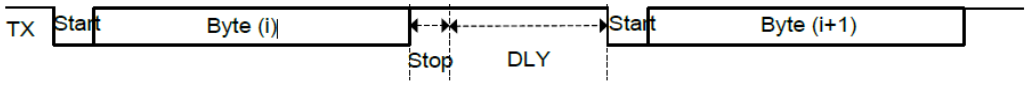
		The Unit is bit time. 
[7:0]	TOIC	Time-out Interrupt Comparator The time-out counter resets and starts counting (the counting clock = baud rate) whenever the RX FIFO receives a new data word. Once the content of time-out counter (TOUT_CNT) is equal to that of time-out interrupt comparator (TOIC), a receiver time-out interrupt (RXTOINT) is generated if RXTOIEN (UART_INTEN[4]) is enabled. A new incoming data word or RX FIFO empty clears RXTOINT. In order to avoid receiver time-out interrupt generation immediately during one character is being received, TOIC value should be set between 40 and 255. So, for example, if TOIC is set with 40, the time-out interrupt is generated after four characters are not received when 1 stop bit and no parity check is set for UART transfer.

4.11.7.8 Baud Rate Divider Register (UART_BAUD)

Register	Offset	R/W	Description	Reset Value
UART_BAUD x = 0, 1, 2, 3	UARTx_BA+0x24	R/W	UART Baud Rate Divisor Register	0x0000_0000

Bits	Description	
[31:16]	Reserved	Reserved.
[15:0]	BRD	Baud Rate Divider The field indicates the baud rate divider. The specific relationship can refer to Table 4-12.

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4.12 I2C Serial Interface Controller (I2C)

4.12.1 Overview

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method for data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. There is one I2C0 controller which supports Power-down wake-up function.

4.12.2 Features

The I2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Supports one I2C port
- Master/Slave mode
- Bi-directional data transfer between masters and slaves
- Multi-master bus
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter that requests the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address registers with mask option)
- Supports Power-down wake-up function

4.12.3 Basic Configuration

The basic configurations of I2C0 are as follow:

- I2C0 pins are configured on SYS_P2_MFP, SYS_P3_MFP, SYS_P4_MFP and SYS_P5_MFP registers.
- Enable I2C clock (i2c0cken) on CLK_APB1_EN [0] register.
- Reset I2C controller (I2C0RST) on IPRST1 [0] register.

4.12.4 Block Diagram

The block diagram of I2C controller is shown in Figure 4-70.

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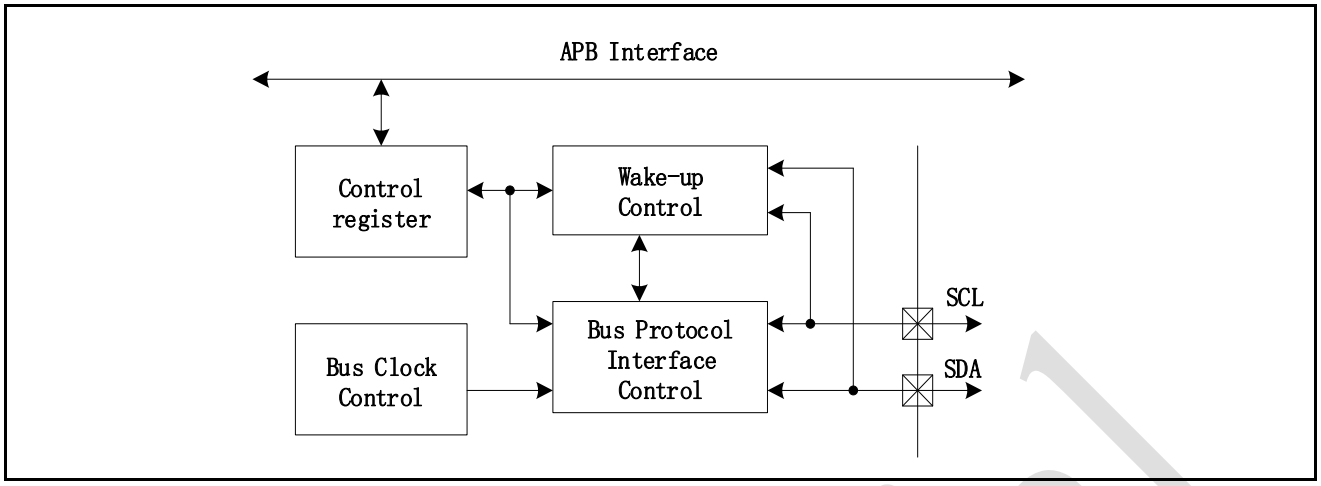

Figure 4-70 I2C Controller Block Diagram

4.12.5 Functional Description

On I2C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronous on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 4-71 for more details about I2C Bus Timing.

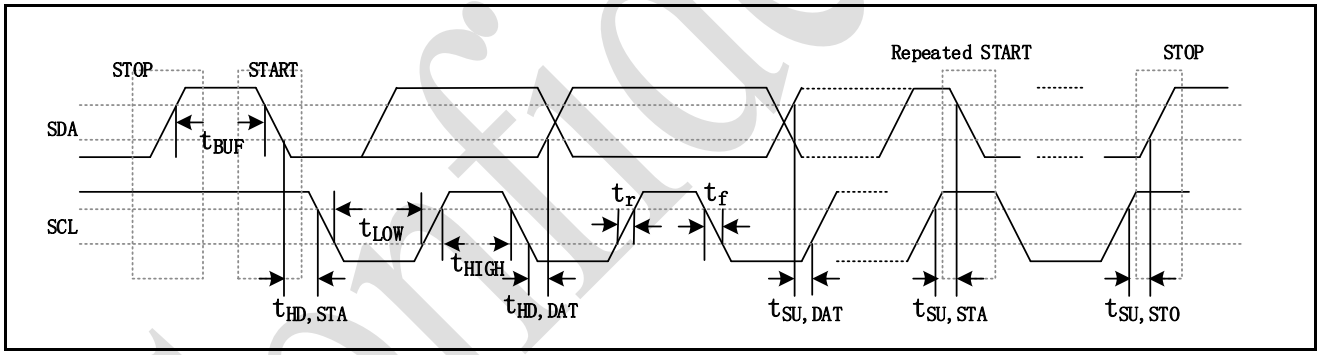

Figure 4-71 I2C Bus Timing

The device's on-chip I2C provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. To enable this port, the bit I2CEN (I2C_CTL[6]) should be set to '1'. The I2C hardware interfaces to the I2C bus via two pins: SDA and SCL. When I/O pins are used as I2C ports, user must set the pins function to I2C in advance.

There is a two-level buffer to improve the performance of I2C bus. In two-level buffer mode, the next transmitted or the last received data can be active even if the current data is transmitted or the last received isn't read back yet.

The I2C SCL bus is stretched low when there is SI event. The NSTRETCH control bit is used to force the I2C SCL bus is no stretched under the SI event.

There are under run or overrun interrupt when the two-level buffer mode is enabled and the interrupt event enable is set.

Note: A pull-up resistor is needed for I2C operation as the SDA and SCL are open-drain pins.

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4.12.5.1 I2C Protocol

Figure 4-72 shows the typical I2C protocol. Normally, a standard communication consists of four parts:

1) START or Repeated START signal generation

2) Slave address and R/W bit transfer

3) Data transfer

4) STOP signal generation

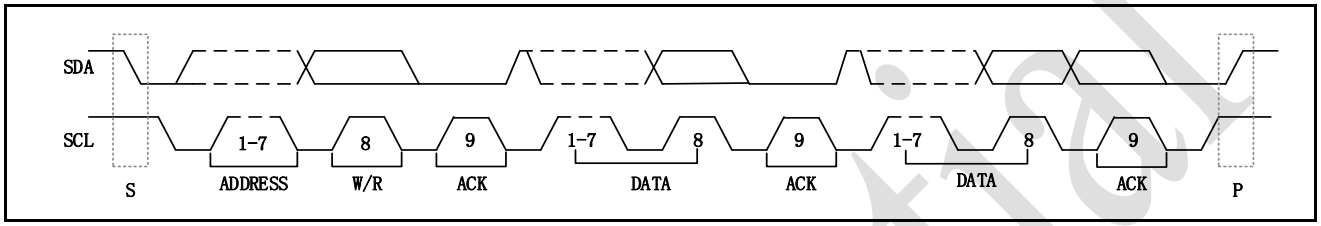

Figure 4-72 I2C Protocol

4.12.5.1.1. START or Repeated START signal

When the bus is free/idle, which means that no master device is engaging the bus (both SCL and SDA lines are high), a master can initiate a transfer by sending a START signal. A START signal, usually referred as the S-bit, is defined as a HIGH to LOW transition on the SDA line while SCL is HIGH. The START signal denotes the beginning of a new data transfer.

A Repeated START is not a STOP signal between two START signals and usually referred to as the "Sr" bit. The master uses this method to communicate with another slave or the same slave in a different transfer direction (e.g. from writing to a device to reading from a device) without releasing the bus.

4.12.5.1.2. STOP signal

The master can terminate the communication by generating a STOP signal. A STOP signal, usually referred to as the "P" bit, is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH.

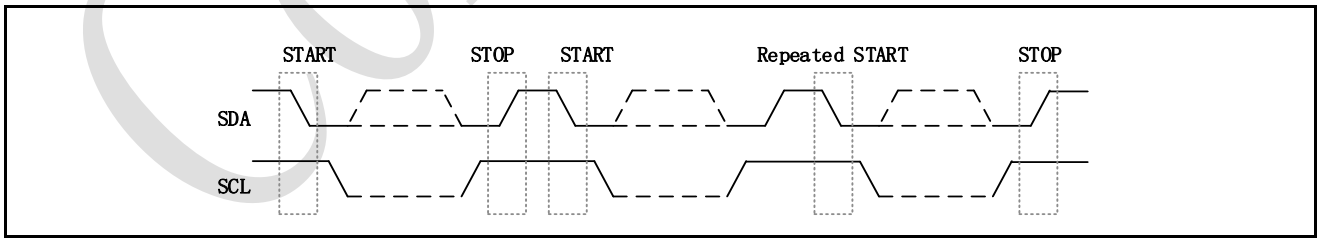

Figure 4-73 START and STOP Condition

4.12.5.1.3. Slave Address Transfer

The first byte of data transferred by the master immediately after the START signal is the Slave address (SLA). This is a 7-bit calling address followed by a Read/Write (RW) bit. The R/W bit signals of the slave indicate the data transfer direction. No two slaves in the system can have the

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same address. Only the slave with an address that matches the one transmitted by the master will respond by returning an acknowledge bit by pulling the SDA low at the 9th SCL clock cycle.

4.12.5.1.4. Data Transfer

When a slave receives a correct address with an R/W bit, the data will follow R/W bit specified to transfer. Each transferred byte is followed by an acknowledge bit on the 9th SCL clock cycle. If the slave signals a Not Acknowledge (NACK), the master can generate a STOP signal to abort the data transfer or generate a Repeated START signal and start a new transfer cycle.

If the master, as the receiving device, does Not Acknowledge (NACK) the slave, the slave releases the SDA line for the master to generate a STOP or Repeated START signal.

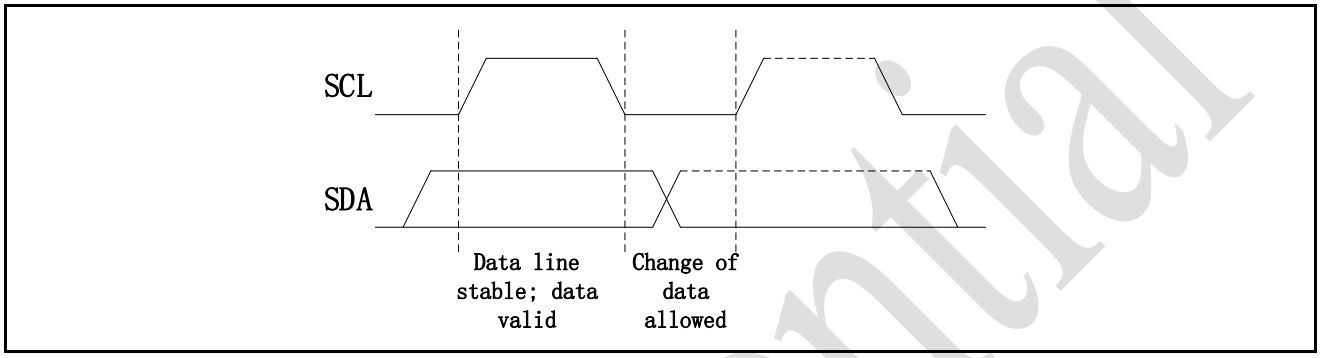

Figure 4-74 Bit Transfer on I2C Bus

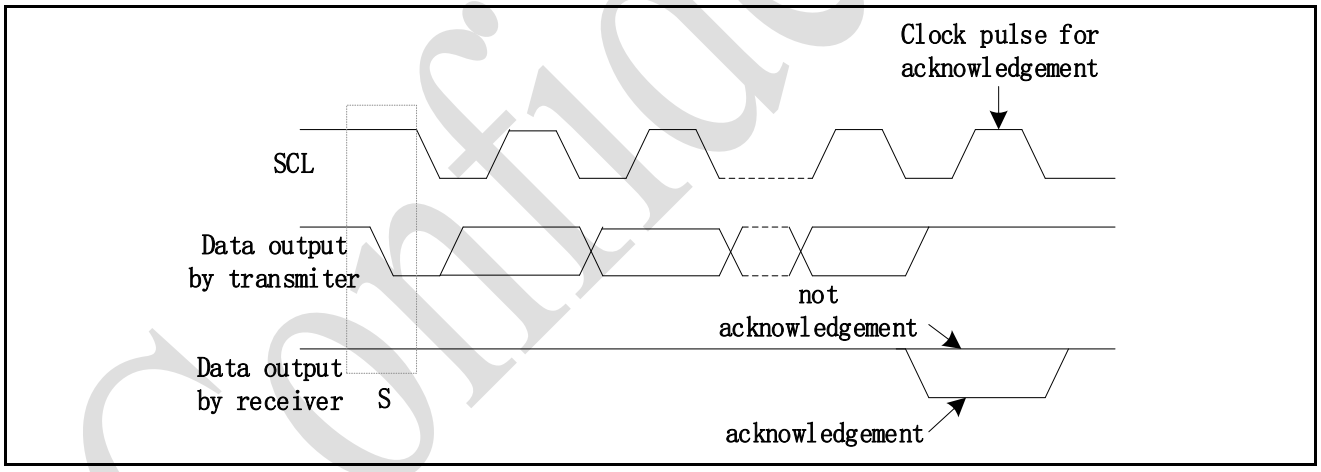

Figure 4-75 Acknowledge on I2C Bus

4.12.5.1.5. Data transfer on I2C bus

Figure 4-76 shows how a master transmits data to slave. A master addresses a slave with a 7-bit address and 1-bit write index to denote that the master wants to transmit data to the slave. The master keeps transmitting data after the slave returns acknowledge to the master.

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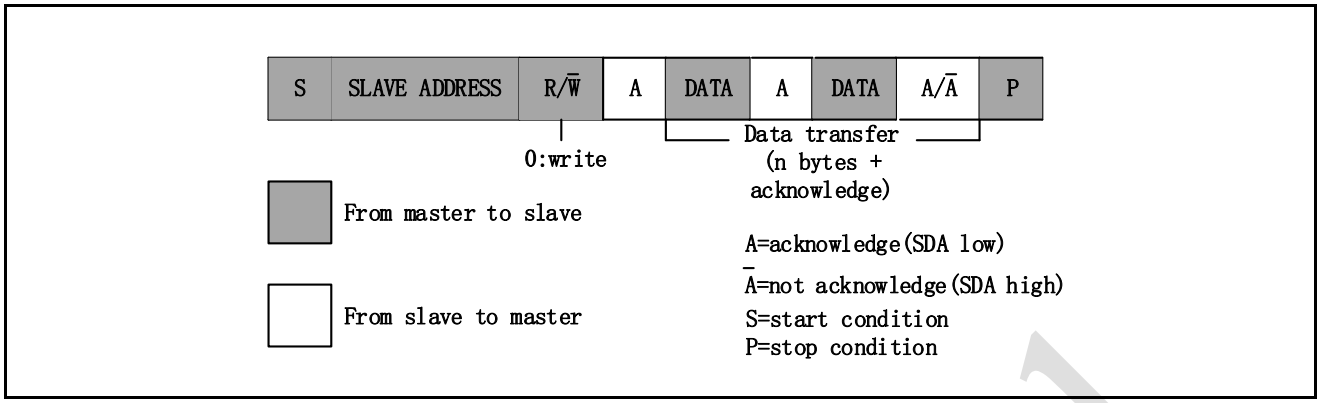

Figure 4-76 Master Transmits Data to Slave

Figure 4-77 shows how a master read data from slave. A master addresses a slave with a 7-bit address and 1-bit read index to denote that the master wants to read data from the slave. The slave will start transmitting data after the slave returns acknowledge to the master.

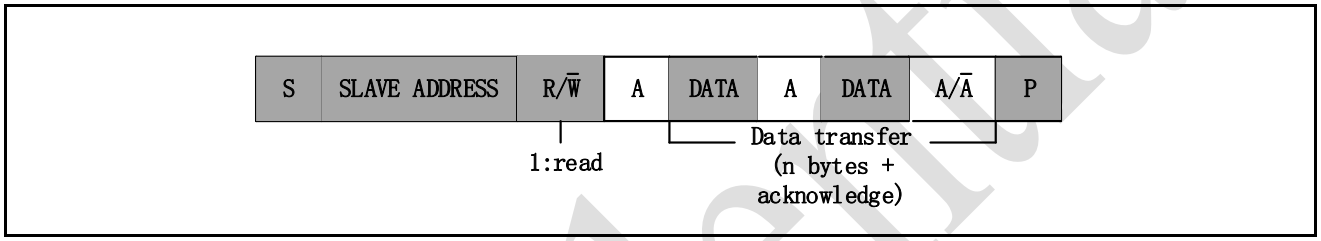

Figure 4-77 Master Reads Data from Slave

4.12.5.2 Operation Modes

The on-chip I2C ports support three operation modes, Master, Slave, and General Call Mode.

In a given application, an I2C port may operate as a master or as a slave. In Slave mode, the I2C port hardware looks for its own slave address and the general call address. If one of these addresses is detected, and if the slave is willing to receive or transmit data from/to master(by setting the AA bit), acknowledge pulse will be transmitted out on the 9th clock, hence an interrupt is requested on both master and slave devices if interrupt is enabled. When the microcontroller wishes to become the bus master, hardware waits until the bus is free before entering Master mode so that a possible slave action is not be interrupted. If bus arbitration is lost in Master mode, I2C port switches to Slave mode immediately and can detect its own slave address in the same serial transfer.

To control the I2C bus transfer in each mode, user needs to set I2C_CTL, I2C_DAT registers according to current status code of I2C_STATUS register. In other words, for each I2C bus action, user needs to check current status by I2C_STATUS register, and then set I2C_CTL, I2C_DAT registers to take bus action. Finally, check the response status by I2C_STATUS.

The bits, STA, STO and AA in I2C_CTL register are used to control the next state of the I2C hardware after the SI flag of I2C_CTL [3] register is cleared. Upon completion of the new action, a new status code will be updated in I2C_STATUS register and the SI flag of I2C_CTL register will be set. If the I2C interrupt control bit INTEN (I2C_CTL [7]) is set, appropriate action or software branch of the new status code can be performed in the Interrupt service routine.

Figure 4-78 shows the current I2C status code is 0x08, and then set I2C_DATA=SLA+W and (STA,STO,SI,AA) = (0,0,1,x) to send the address to I2C bus. If a slave on the bus matches the address and response ACK, the I2C_STATUS will be updated by status code 0x18.

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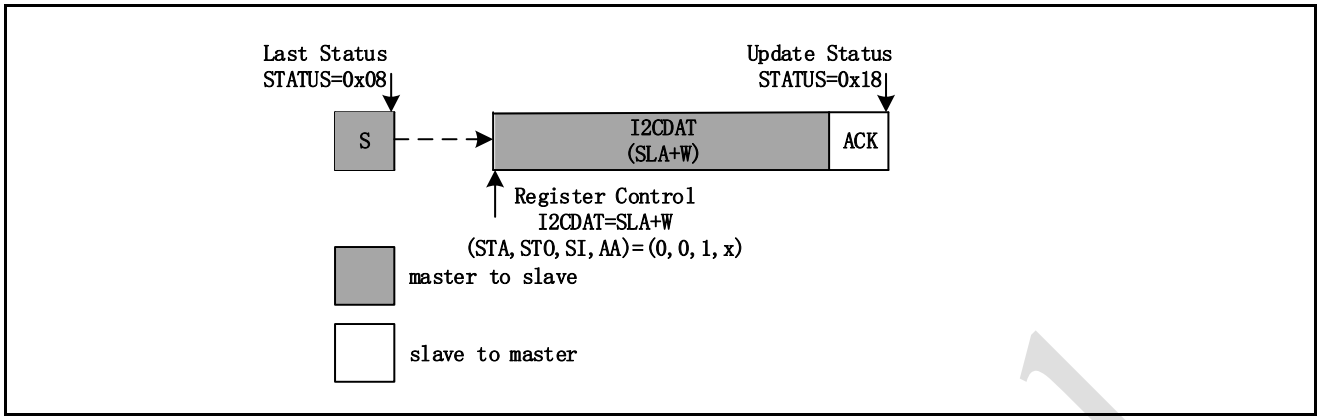

Figure 4-78 Control I2C Bus according to Current I2C Status

4.12.5.2.1. Master Mode

All possible protocols for I2C master are shown in Figure 4-79 and Figure 4-80. User needs to follow proper path of the flow to implement required I2C protocol.

In other words, user can send a START signal to bus and I2C will be in Master Transmitter mode (as shown in Figure 4-79) or Master receiver mode (as shown in Figure 4-80) after START signal has been sent successfully and new status code would be 0x08. Followed by START signal, user can send slave address, read/write bit, data and Repeat START, STOP to perform I2C protocol.

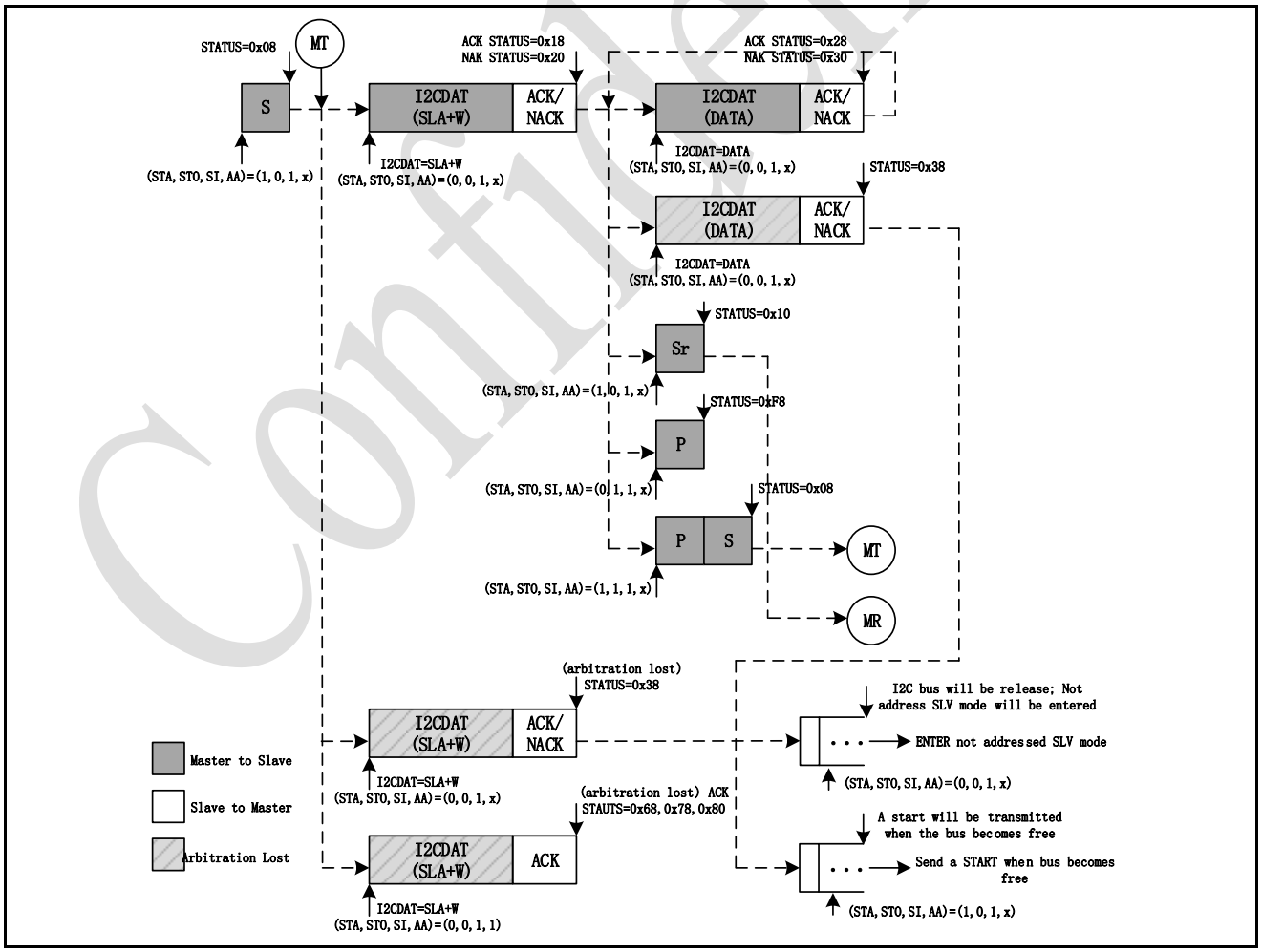

Figure 4-79 Master Transmitter Mode Control Flow

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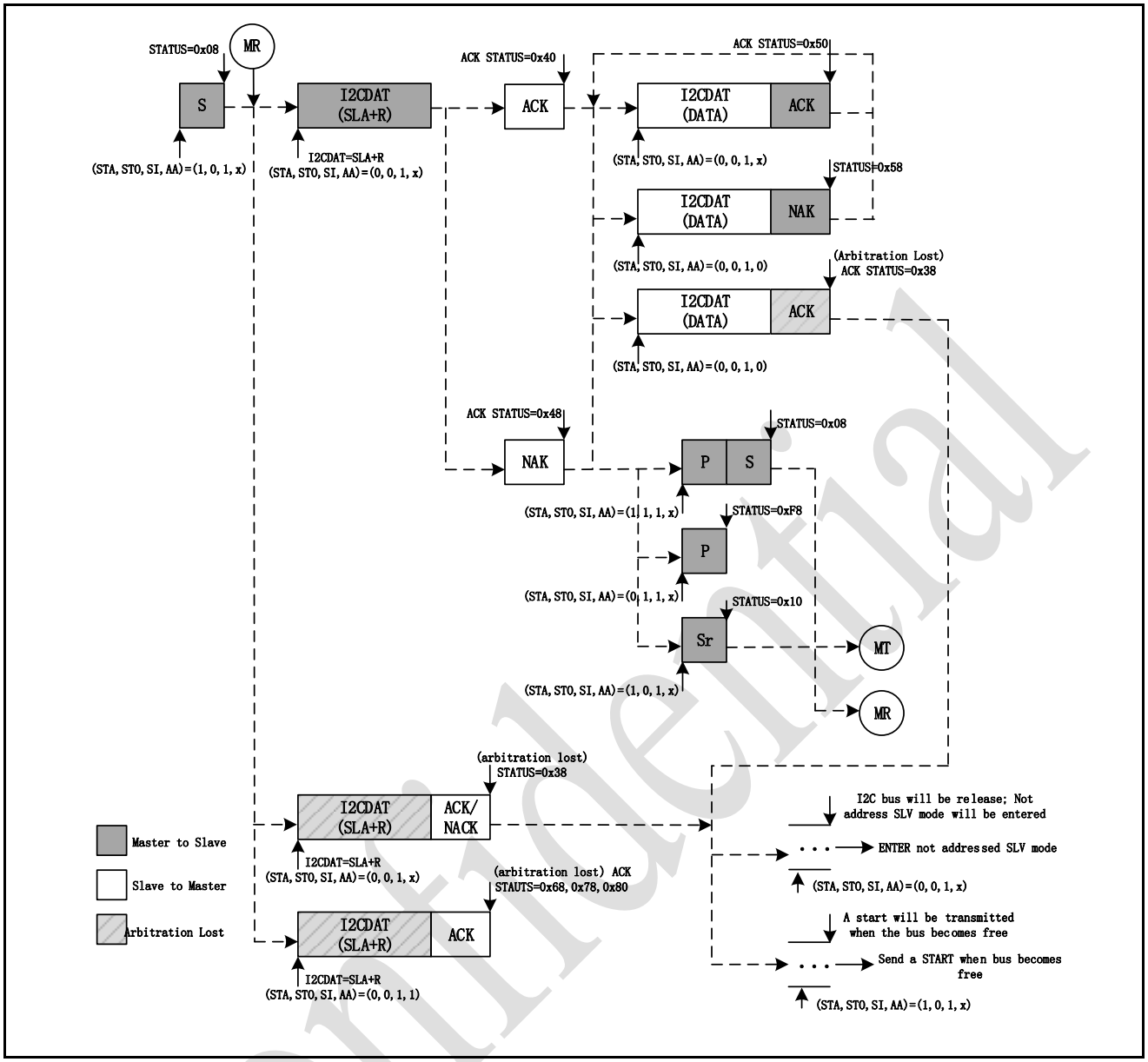

Figure 4-80 Master Receiver Mode Control Flow

If the I2C is in Master mode and gets arbitration lost, the status code will be 0x38. In status 0x38, user may set (STA, STO, SI, AA) = (1, 0, 1, X) to send START to re-start Master operation when bus becomes free. Otherwise, user may set (STA, STO, SI, AA) = (0, 0, 1, X) to release I2C bus and enter not addressed Slave mode.

4.12.5.2.2. Slave Mode

When reset as default, I2C is not addressed and will not recognize the address on I2C bus. User can set slave address by I2C_ADDRx and set (STA, STO, SI, AA) = (0, 0, 1, 1) to let I2C recognize the address sent by master. Figure 4-81 shows all the possible flow for I2C in Slave mode. Users need to follow a proper flow (as shown in Figure 4-81) to implement their own I2C protocol.

If bus arbitration is lost in Master mode, the I2C port switches to Slave mode immediately and can detect its own slave address in the same serial transfer. If the detected address is SLA+W (Master want to write data to Slave) after arbitration lost, the status code is 0x68. If the detected address is SLA+R (Master want to read data from Slave) after arbitration lost, the status code is 0xB0.

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Note: During I2C communication, the SCL clock will be released when writing '1' to clear the SI flag in Slave mode.

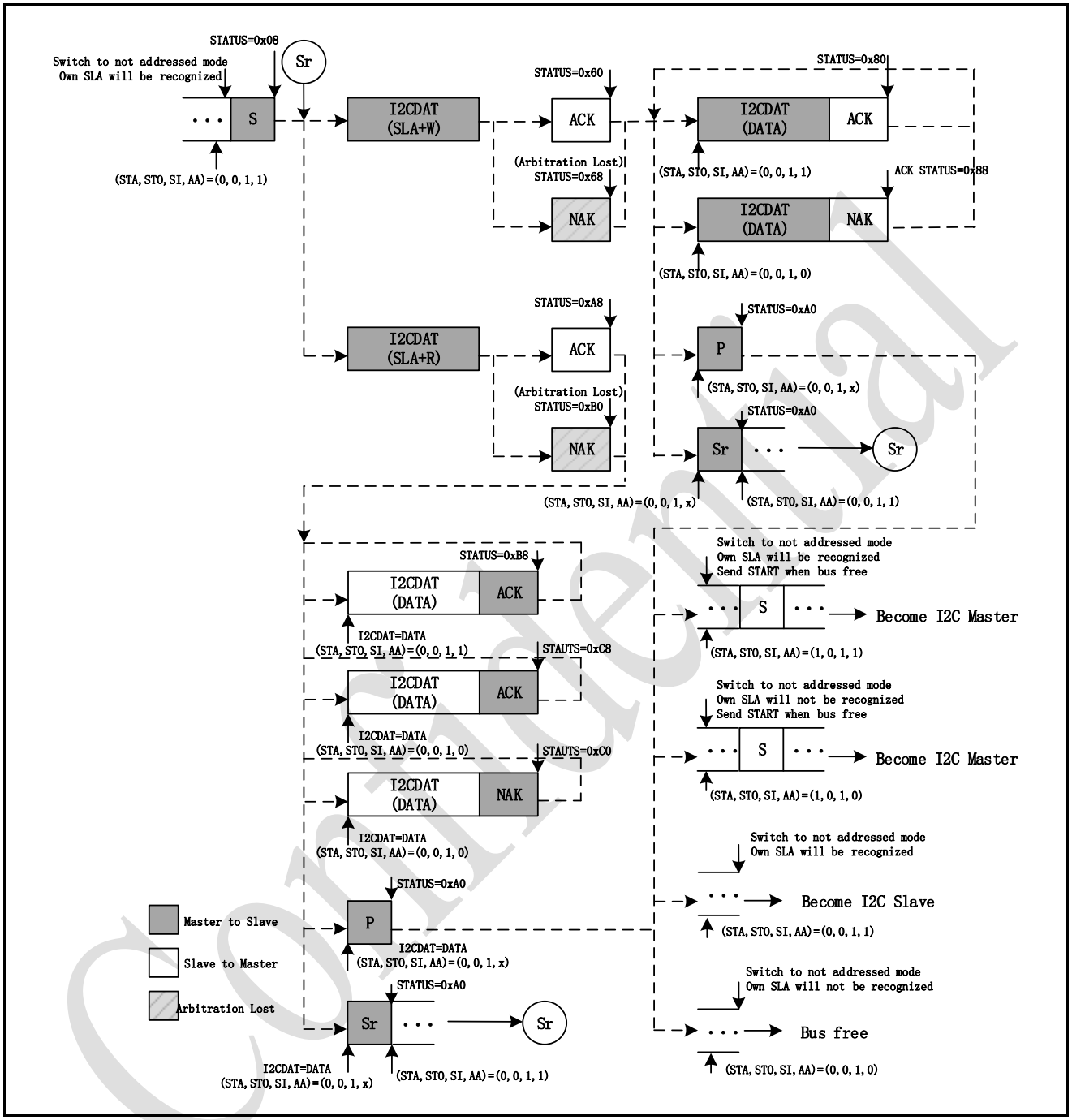

Figure 4-81 Slave Mode Control Flow

If I2C is still receiving data in addressed Slave mode but got a STOP or Repeat START, the status code will be 0xA0. User could follow the action for status code 0x88 as shown in Figure 6.11-15 when getting 0xA0 status.

If I2C is still transmitting data in addressed Slave mode but got a STOP or Repeat START, the status code will be 0xA0. User could follow the action for status code 0xC8 as shown in Figure 1.10-15 when getting 0xA0 status.

Note: After slave gets status of 0x88, 0xC8, 0xC0 and 0xA0, slave can switch to not address mode

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and own SLA will not be recognized. If entering this status, slave will not receive any I2C signal or address from master. At this status, I2C should be reset to leave this status.

4.12.5.2.3. General Call (GC) Mode

If the GC bit (I2C_ADDRx [0]) is set, the I2C port hardware will respond to General Call address (00H). User can clear GC bit to disable general call function. When the GC bit is set and the I2C is in Slave mode, it can receive the general call address by 0x00 after master send general call address to I2C bus, then it will follow status of GC mode.

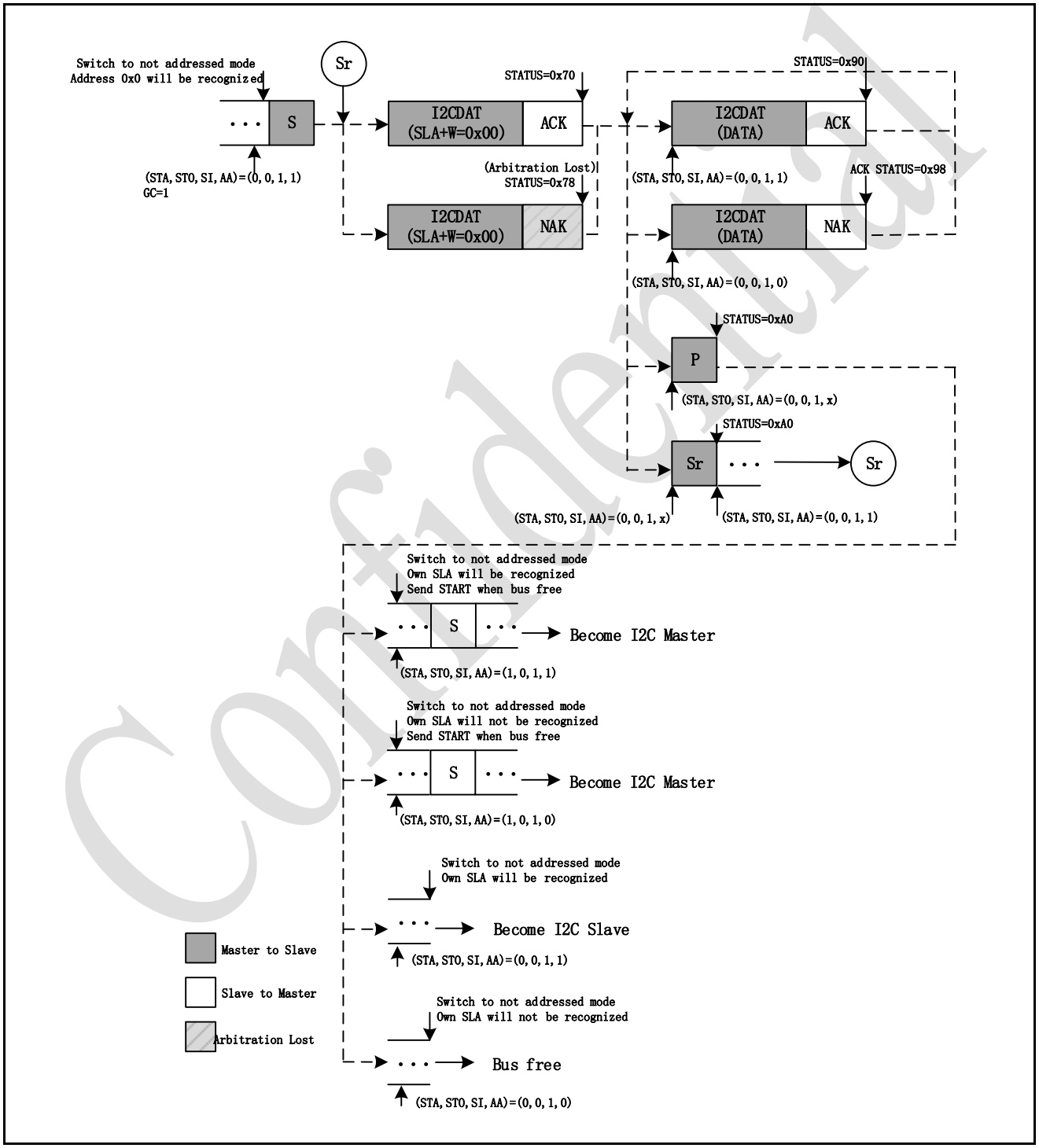

Figure 4-82 GC Mode

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If I2C is still receiving data in GC mode but got a STOP or Repeat START, the status code will be 0xA0. User could follow the action for status code 0x98 in Figure 4-82 when getting 0xA0 status.

Note: After slave gets status of 0x98 and 0xA0, slave can switch to not address mode and own SLA will not be recognized. If entering this status, slave will not receive any I2C signal or address from master. At this time, the I2C controller should be reset to exit this status.

4.12.5.2.4. Multi-Master

In some applications, there are two or more masters on the same I2C bus to access slaves, and the masters may transmit data simultaneously. The I2C supports multi-master by including collision detection and arbitration to prevent data corruption.

- When I2C_STATUS = 0x38, an “Arbitration Lost” is received. Arbitration lost event maybe occur during the send START bit, data bits or STOP bit. User could set (STA, STO, SI, AA) = (1, 0, 1, X) to send START again when bus free, or set (STA, STO, SI, AA) = (0, 0, 1, X) to send STOP to back to not addressed Slave mode.
- When I2C_STATUS = 0x00, a “Bus Error” is received. To recover I2C bus from a bus error, STO should be set and SI should be cleared, and then STO is cleared to release bus.
  - Set (STA, STO, SI, AA) = (0, 1, 1, X) to stop current transfer
  - Set (STA, STO, SI, AA) = (0, 0, 1, X) to release bus

4.12.5.3 I2C Protocol Registers

To control the I2C port through the following fifteen special function registers: I2C_CTL (control register), I2C_STATUS (status register), I2C_DAT (data register), I2C_ADDRn (address registers, n=0~3), I2C_ADDRMSKn (address mask registers, n=0~3), I2C_CLKDIV (clock rate register) and I2C_TOCTL (time-out counter register), I2C_CTL1 (control register 1) and I2C_STATUS1 (status register 1).

4.12.5.3.1. Address Registers (I2C_ADDR)

The I2C port is equipped with four slave address registers I2C_ADDRn (n=0~3). The contents of the register are irrelevant when I2C is in Master mode. In Slave mode, the bit field I2C_ADDRn[7:1] must be loaded with the chip’s own slave address. The I2C hardware will react if the contents of I2C_ADDRn are matched with the received slave address.

The I2C ports support the “General Call” function. If the GC bit (I2C_ADDRn[0]) is set, the I2C port hardware will respond to General Call address (00H). Clearing GC bit will disable general call function.

When GC bit is set and the I2C is in Slave mode, it can receive the general call address by 00H after Master send general call address to I2C bus, then it will follow status of GC mode.

4.12.5.3.2. Slave Address Mask Registers (I2C_ADDRMSK)

The I2C bus controller supports multiple address recognition with four address mask registers I2C_ADDRMSKx (x=0~3). When the bit in the address mask register is set to 1, it means the received corresponding address bit is "Don’t care". If the bit is set to 0, it means the received corresponding register bit should be exactly the same as address register.

4.12.5.3.3. Data Register (I2C_DAT)

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This register contains a byte of serial data to be transmitted or a byte which just has been received. The CPU can read from or write to this 8-bit (I2C_DAT[7:0]) directly while it is not in the process of shifting a byte. When I2C is in a defined state and the serial interrupt flag (SI) is set, data in I2C_DAT[7:0] remains stable. While data is being shifted out, data on the bus is simultaneously being shifted in; I2C_DAT[7:0] always contains the last data byte present on the bus.

The acknowledge bit is controlled by the I2C hardware and cannot be accessed by the CPU. Serial data is shifted through into I2C_DAT[7:0] on the rising edges of serial clock pulses on the SCL line. When a byte has been shifted into I2C_DAT[7:0], the serial data is available in I2C_DAT[7:0], and the acknowledge bit (ACK or NACK) is returned by the control logic during the ninth clock pulse. In order to monitor bus status while sending data, the bus date will be shifted to I2C_DATA[7:0] when sending I2C_DATA[7:0] to bus. In the case of sending data, serial data bits are shifted out from I2C_DAT [7:0] on the falling edge of SCL clocks, and is shifted to I2C_DAT [7:0] on the rising edge of SCL clocks.

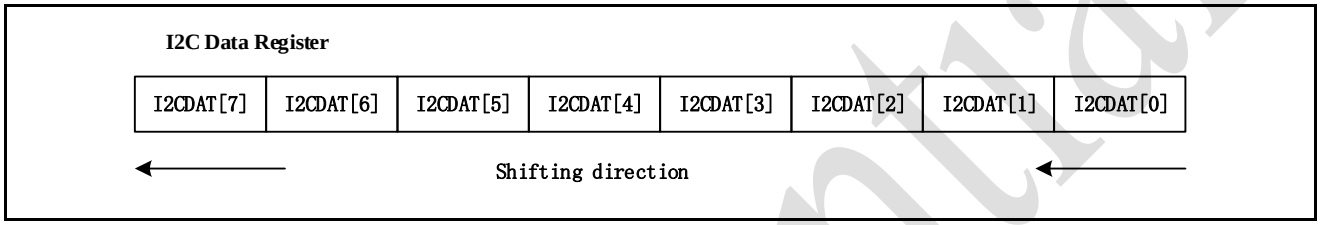

Figure 4-83 I2C Data Shifting Direction

4.12.5.3.4. Control Register (I2C_CTL)

The CPU can read from and write to I2C_CTL[7:0] directly. When the I2C port is enabled by setting I2CEN (I2C_CTL [6]) to high, the internal states will be controlled by I2C_CTL and I2C logic hardware.

There are two bits are affected by hardware: the SI bit is set when the I2C hardware requests a serial interrupt, and the STO bit is cleared when a STOP condition is present on the bus. The STO bit is also cleared when I2CEN = 0.

Once a new status code is generated and stored in I2C_STATUS, the I2C Interrupt Flag bit SI (I2C_CTL [3]) will be set automatically. If the Enable Interrupt bit INTEN (I2C_CTL [7]) is set at this time, the I2C interrupt will be generated. The bit field I2C_STATUS[7:0] stores the internal state code, the content keeps stable until SI is cleared by software.

4.12.5.3.5. Status Register (I2C_STATUS)

I2C_STATUS[7:0] is an 8-bit read-only register. The bit field I2C_STATUS[7:0] contain the status code. There are 26 possible status codes. All states are listed in section Table 6.11-1. When I2C_STATUS[7:0] is F8H, no serial interrupt is requested. All other I2C_STATUS[7:0] values correspond to defined I2C states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2C_STATUS[7:0] one cycle after SI is set by hardware and is still present one cycle after SI has been reset by software.

In addition, the state 00H stands for a Bus Error, which occurs when a START or STOP condition is present at an incorrect position in the I2C format frame. A Bus Error may occur during the serial transfer of an address byte, a data byte or an acknowledge bit. To recover I2C from bus error, STO should be set and SI should be cleared to enter Not Addressed Slave mode. Then STO is cleared to release bus and to wait for a new communication. I2C bus cannot recognize stop condition during this action when bus error occurs.

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Table 4-16 I2C Status Code Description

Master Mode		Slave Mode	
STATUS	Description	STATUS	Description
0x08	Start	0xA0	Slave Transmit Repeat Start or Stop
0x10	Master Repeat Start	0xA8	Slave Transmit Address ACK
0x18	Master Transmit Address ACK	0xB0	Slave Transmit Arbitration Lost
0x20	Master Transmit Address NACK	0xB8	Slave Transmit Data ACK
0x28	Master Transmit Data ACK	0xC0	Slave Transmit Data NACK
0x30	Master Transmit Data NACK	0xC8	Slave Transmit Last Data ACK
0x38	Master Arbitration Lost	0x60	Slave Receive Address ACK
0x40	Master Receive Address ACK	0x68	Slave Receive Arbitration Lost
0x48	Master Receive Address NACK	0x80	Slave Receive Data ACK
0x50	Master Receive Data ACK	0x88	Slave Receive Data NACK
0x58	Master Receive Data NACK	0x70	GC mode Address ACK
0x00	Bus error	0x78	GC mode Arbitration Lost
		0x90	GC mode Data ACK
		0x98	GC mode Data NACK
0xF8	Bus Released Note: The status “0xF8” exists in both master/slave modes, and it won’t raise interrupt.		

4.12.5.3.6. I2C Clock Baud Rate Bits (I2C_CLKDIV)

The data baud rate of I2C is determined by the I2C_CLKDIV[7:0] register when I2C is in Master mode. It is not necessary in a Slave mode. In Slave mode, I2C will automatically synchronize with any clock frequency from master I2C device.

4.12.5.3.7. I2C Time-out Counter Register (I2C_TOCTL)

There is a 14-bit time-out counter which can be used to deal with the I2C bus hang-up. If the time-out counter is enabled, the counter starts up_counting until it overflows (TOIF=1) and generates I2C interrupt to CPU or stops counting by clearing I2CEN to 0. When time-out counter is enabled, setting flag SI to high will reset counter and re-start up_counting after SI is cleared. If I2C bus is hung up, it causes the I2C_STATUS and flag SI are not updated for a period, the 14-bit time-out counter may overflow and acknowledge CPU the I2C interrupt. Refer to Figure 1.10-17 for the 14-bit time-out counter. User may write 1 to clear TOIF to 0.

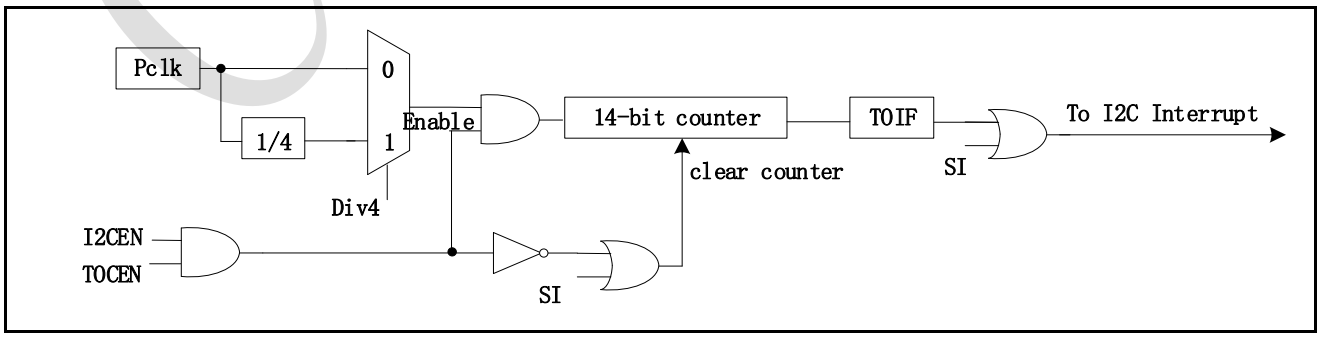

Figure 4-84 I2C Time-out Count Block Diagram

4.12.5.3.8. I2C Control Register 1 (I2C_CTL1)

The NSTRETCH (I2C_CTL1[2]) bit is used to no stretch the bus clock when this bit is set to 1.

For the TWOLVFIFO (I2C_CTL1[1]) bit , it is used to enable the two-level buffer for I2C transmitted or received buffer. It is used to improve the performance of the I2C bus. If this bit is set to 1, the control bit of STA (I2C_CTL[5]) for repeat start or STO (I2C_CTL[4]) bit should be set after the current interrupt is cleared. For example, if there are 4 data to be transmitted and then stopped. The STOP bit shall be set after the 3rd data's interrupt event is cleared. At this time, the 4_{th} data can be transmitted and the I2C stops after the 4_{th} data transmission done.

The two-level buffer status interrupt enable can be enabled by I2C_CTL1[4:3] to generate the under run or overrun event.

When entering Power-down mode, other I2C master can wake-up the chip by addressing the I2C device, and user must configure the related setting before entering Sleep mode. When the chip is woken-up by address match with one of the four address register, the following data will be abandoned at this time. Note that only I2C0 channel supports wake-up function.

4.12.5.3.9. I2C Status Register 1 (I2C_STATUS1)

The two-level buffer status, busy free information, buffer empty, buffer full and overrun or under run are also listed in this register.

When system is woken up by other I2C master device, WKIF is set to indicate this event. User needs to write "1" to clear this bit. The other status bits are used to indicate the current buffer status when the TWOLVFIFO (I2C_CTL1[1]) is set. Note that only I2C0 channel supports wake-up function.

4.12.5.4 Example of Random Read on EEPROM

The following steps are used to configure the I2C related registers when using I2C to read data from EEPROM.

1. Set the multi-function pin in the "SYS_P3_MFP" registers as SCL and SDA pins.
2. Enable I2C APB clock, i2c0cken=1 in the "CLK_APB1_EN" register.
3. Set I2C_RST=1 to reset I2C controller then set I2C controller to normal operation, I2C0RST=0 in the "IPRST1" register.
4. Set I2CEN=1 to enable I2C controller in the "I2C_CTL" register.
5. Give I2C clock a divided register value for I2C clock rate in the "I2C_CLKDIV".
6. Set SETENA=0x00040000 in the "NVIC_ISER" register to set I2C IRQ.
7. Set INTEN =1 to enable I2C Interrupt in the "I2C_CTL" register.
8. Set I2C address registers which are "I2C_ADDR0~I2C_ADDR3".

Random read operation is one of the methods toaccess EEPROM. The method allows the master to access any address of EEPROM space.

Figure 4-85 shows the EEPROM random read operation.

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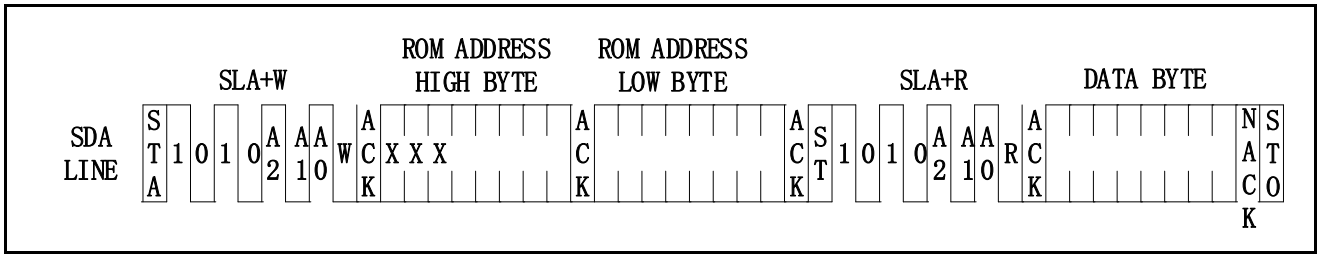

Figure 4-85 EEPROM Random Read

Figure 4-86 shows how to use I2C controller to implement the protocol of EEPROM random read.

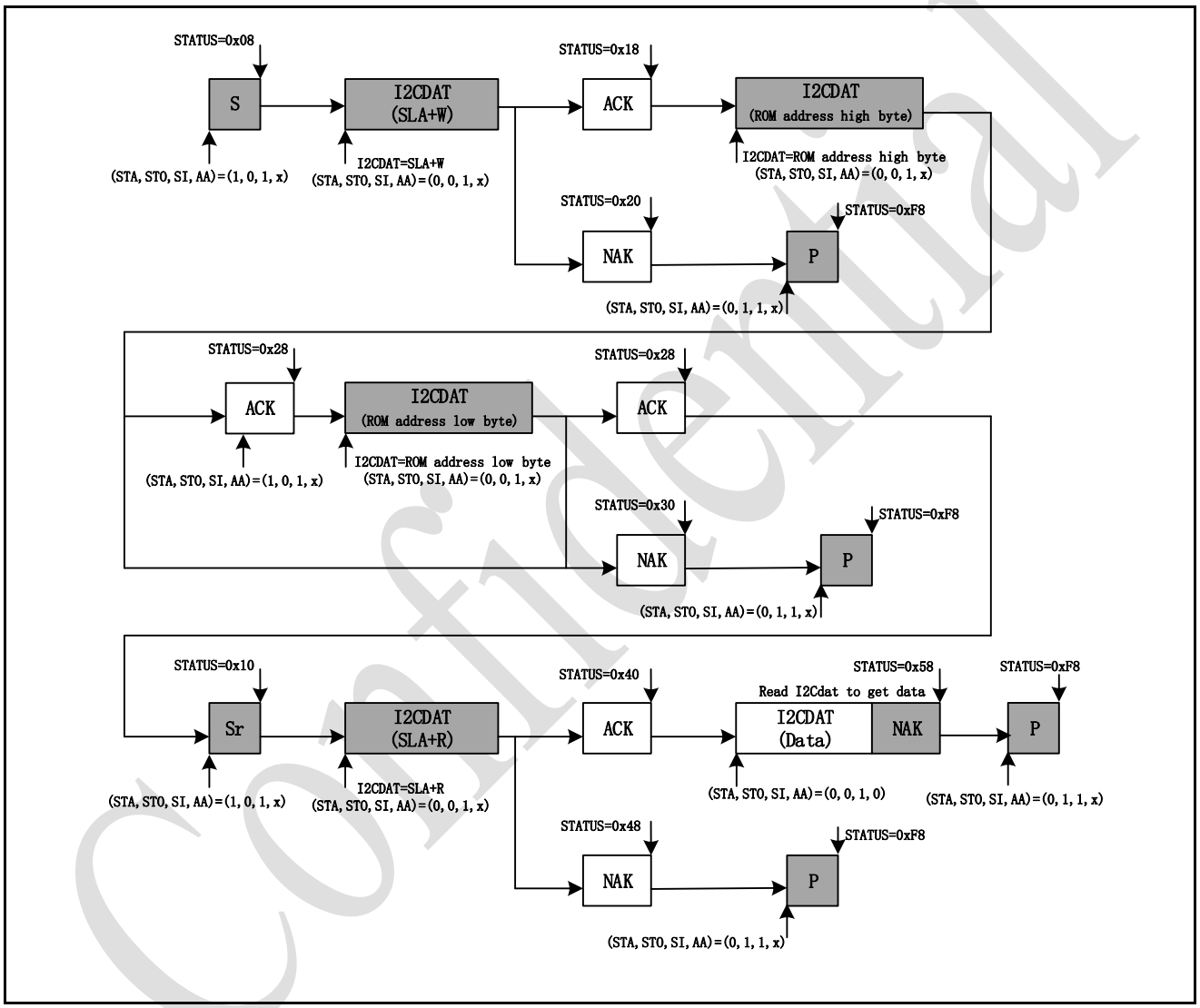

Figure 4-86 Protocol of EEPROM Random Read

The I2C controller sends START to bus to be a master. Then it sends a SLA+W (Slave address + Write bit) to EERPOM followed by two bytes data address to set the EEPROM address to read. Finally, a Repeat START followed by SLA+R is sent to read the data from EEPROM.

4.12.6 I2C Register Map

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value

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I2C Base Address: I2C0_BA = 0x4000_0000				
I2C_CTL	I2C0_BA+0x00	R/W	I2C Control Register	0x0000_0000
I2C_DAT	I2C0_BA+0x08	R/W	I2C DATA Register	0x0000_00FF
I2C_STATUS	I2C0_BA+0x0C	R	I2C Status Register	0x0000_00F8
I2C_CLKDIV	I2C0_BA+0x10	R/W	I2C Clock Divided Register	0x0000_0004
I2C_TOCTL	I2C0_BA+0x14	R/W	I2C Time-out Control Register	0x0000_0000
I2C_ADDR0	I2C0_BA+0x04	R/W	I2C Slave Address Register 0	0x0000_0000
I2C_ADDR1	I2C0_BA+0x18	R/W	I2C Slave Address Register 1	0x0000_0000
I2C_ADDR2	I2C0_BA+0x1C	R/W	I2C Slave Address Register 2	0x0000_0000
I2C_ADDR3	I2C0_BA+0x20	R/W	I2C Slave Address Register 3	0x0000_0000
I2C_ADDRMSK0	I2C0_BA+0x24	R/W	I2C Slave Address Mask Register 0	0x0000_0000
I2C_ADDRMSK1	I2C0_BA+0x28	R/W	I2C Slave Address Mask Register 1	0x0000_0000
I2C_ADDRMSK2	I2C0_BA+0x2C	R/W	I2C Slave Address Mask Register 2	0x0000_0000
I2C_ADDRMSK3	I2C0_BA+0x30	R/W	I2C Slave Address Mask Register 3	0x0000_0000
I2C_CTL1	I2C0_BA+0x3C	R/W	I2C Control Register 1	0x0000_0000
I2C_STATUS1	I2C0_BA+0x40	R/W	I2C Status Register 1	0x0000_0000

4.12.7 I2C Register Description

4.12.7.1 I2C Control Register (I2C_CTL)

Register	Offset	R/W	Description	Reset Value
I2C_CTL	I2C0_BA+0x00	R/W	I2C Control Register	0x0000_0000

Bits	Description	
[31:8]	Reserved	Reserved.
[7]	INTEN	Interrupt Enable Bit 0 = I2C interrupt Disabled. 1 = I2C interrupt Enabled.
[6]	I2CEN	I2C Controller Enable Bit 0 = I2C Controller Disabled. 1 = I2C Controller Enabled. Set to enable I2C serial function controller. When I2CEN=1 the I2C serial function enables. The function of multi-function pin must be set to I2C first.
[5]	STA	I2C START Control Bit Set STA to logic 1 to enter Master mode. I2C hardware sends a START or repeats the START condition to bus when the bus is free.
[4]	STO	I2C STOP Control Bit In Master mode, setting STO to transmit a STOP condition to bus then I2C hardware will check the bus condition if a STOP condition is detected this bit will be cleared by hardware automatically. In Slave mode, setting STO resets I2C hardware to the defined “not addressed” Slave mode. This means it is NO LONGER in the Slave receiver mode to receive data from the master transmit device.

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[3]	SI	I2C Interrupt Flag When a new I2C state is present in the I2C_STATUS register, the SI flag is set by hardware, and if bit INTEN (I2C_CTL[7]) is set, the I2C interrupt is requested. SI must be cleared by software. This bit can be cleared by software writing '1'.
[2]	AA	Assert Acknowledge Control Bit When AA=1 is prior to address or data received, an acknowledged (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when 1.) A slave is acknowledging the address sent from master, 2.) The receiver devices are acknowledging the data sent by transmitter. When AA=0 prior to address or data received, a Not acknowledged (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line.
[1:0]	Reserved	Reserved.

4.12.7.2 I2C Data Register (I2C_DAT)

Register	Offset	R/W	Description	Reset Value
I2C_DAT	I2C0_BA+0x08	R/W	I2C DATA Register	0x0000_00FF

Bits	Description	
[31:8]	Reserved	Reserved.
[7:0]	DAT[7:0]	I2C Data Register Bit [7:0] is located with the 8-bit transferred data of the I2C serial port.

4.12.7.3 I2C Status Register (I2C_STATUS)

Register	Offset	R/W	Description	Reset Value
I2C_STATUS	I2C0_BA+0x0C	R	I2C Status Register	0x0000_00F8

Bits	Description	
[31:8]	Reserved	Reserved.
[7:0]	STATUS[7:0]	I2C Status Register The three least significant bits are always 0. The five most significant bits contain the status code. There are 26 possible status codes. When I2C_STATUS contains F8H, no serial interrupt is requested. All the other I2C_STATUS values correspond to defined I2C states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2C_STATUS one cycle after SI is set by hardware and is still present one cycle after SI has been reset by software. In addition, the states 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the formation frame. Examples of illegal position are during the serial transfer of an address byte, a data byte or an acknowledge bit.

4.12.7.4 I2C Clock Divided Register (I2C_CLKDIV)

Register	Offset	R/W	Description	Reset Value
I2C_CLKDIV	I2C0_BA+0x10	R/W	I2C Clock Divided Register	0x0000_0004

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Bits	Description	
[31:8]	Reserved	Reserved.
[7:0]	DI-VIDER[7:0]	I2C Clock Divided Register The I2C clock rate bits: Data Baud Rate of I2C = (system clock) / (4* (I2C_CLKDIV+1)). Note: The minimum value of I2C_CLKDIV is 4.

4.12.7.5 I2C Time-out Control Register (I2C_TOCTL)

Register	Offset	R/W	Description	Reset Value
I2C_TOCTL	I2C0_BA+0x14	R/W	I2C Time-out Control Register	0x0000_0000

Bits	Description	
[31:3]	Reserved	Reserved.
[2]	TOCEN	Time-out Counter Enable Bit 0 = Time-out counter Disabled. 1 = Time-out counter Enabled. Note: When the 14-bit time-out counter is enabled, it will start counting when SI is cleared. Set-ting 1 to the SI flag will reset counter and re-start up_counting after SI is cleared.
[1]	TOCURIEN	Time-out Counter Input Clock Divided By 4 0 = Time-out counter input clock divided by 4 Disabled. 1 = Time-out counter input clock divided by 4 Enabled. Note: When enabled, the time-out period is extended 4 times.
[0]	TOIF	Time-out Flag This bit is set by hardware when I2C time-out happened and it can interrupt CPU if I2C interrupt enable bit (INTEN) is set to 1. Note: This bit can be cleared by software writing ‘1’.

4.12.7.6 I2C Slave Address Register (I2C_ADDRx)

Register	Offset	R/W	Description	Reset Value
I2C_ADDR0	I2C0_BA+0x04	R/W	I2C Slave Address Register 0	0x0000_0000
I2C_ADDR1	I2C0_BA+0x18	R/W	I2C Slave Address Register 1	0x0000_0000
I2C_ADDR2	I2C0_BA+0x1C	R/W	I2C Slave Address Register 2	0x0000_0000
I2C_ADDR3	I2C0_BA+0x20	R/W	I2C Slave Address Register 3	0x0000_0000

Bits	Description	
[31:8]	Reserved	Reserved.
[7:1]	ADDR[7:1]	I2C Address The content of this register is irrelevant when I2C is in Master mode. In Slave mode, the seven most significant bits must be loaded with the MCU’s own address. The I2C hardware will react if either of the address is matched.
[0]	GC	General Call Function Control 0 = General Call Function Disabled. 1 = General Call Function Enabled.

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4.12.7.7 I2C Slave Address Mask Register (I2C_ADDRMSKx)

Register	Offset	R/W	Description	Reset Value
I2C_ADDRMSK0	I2C0_BA+0x24	R/W	I2C Slave Address Mask Register 0	0x0000_0000
I2C_ADDRMSK1	I2C0_BA+0x28	R/W	I2C Slave Address Mask Register 1	0x0000_0000
I2C_ADDRMSK2	I2C0_BA+0x2C	R/W	I2C Slave Address Mask Register 2	0x0000_0000
I2C_ADDRMSK3	I2C0_BA+0x30	R/W	I2C Slave Address Mask Register 3	0x0000_0000

Bits	Description	
[31:8]	Reserved	Reserved.
[7:1]	ADDRMSK[7:1]	I2C Address Mask Bits 0 = I2C address mask Disabled (the received corresponding register bit should be exactly the same as address register). 1 = I2C address mask Enabled (the received corresponding address bit is “Don’t care”).
[0]	Reserved	Reserved.

4.12.7.8 I2C Control Register 1 (I2C_CTL1)

Register	Offset	R/W	Description	Reset Value
I2C_CTL1	I2C0_BA+0x3C	R/W	I2C Control Register 1	0x0000_0000

Bits	Description	
[31:3]	Reserved	Reserved.
[2]	NSTRETCH	No Stretch On The I2C Bus 0 = The I2C SCL bus is stretched by hardware if the SI is not cleared in slave mode. 1 = The I2C SCL bus is not stretched by hardware if the SI is not cleared in slave mode.
[1]	Reserved	Reserved.
[0]	WKEN	Wake-up Enable Bit 0 = I2C wake-up function Disabled. 1 = I2C wake-up function Enabled. The system can be woken up by I2C bus when the system is set into Power mode and the received data matched one of the addresses in Address Register.

4.12.7.9 I2C Status Register 1 (I2C_STATUS1)

Register	Offset	R/W	Description	Reset Value
I2C_STATUS1	I2C0_BA+0x40	R/W	I2C Status Register 1	0x0000_0000

Bits	Description	
[31:1]	Reserved	Reserved.
[0]	WKIF	I2C Wake-up Interrupt Flag When chip is woken up from Power-down mode by I2C, this bit is set to 1. This bit can be cleared by software writing “1”.

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4.13 Serial Peripheral Interface (SPI)

4.13.1 Overview

The PAN2025 provides two channels of Serial Peripheral Interface (SPI). The SPI applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. The SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. SPI controller can be configured as a master or a slave device.

4.13.2 Features

- Supports Master or Slave mode operation
- Configurable transfer bit length
- Provides one 32-bit FIFO buffer
- Supports MSB first or LSB first transfer

4.13.3 Block Diagram

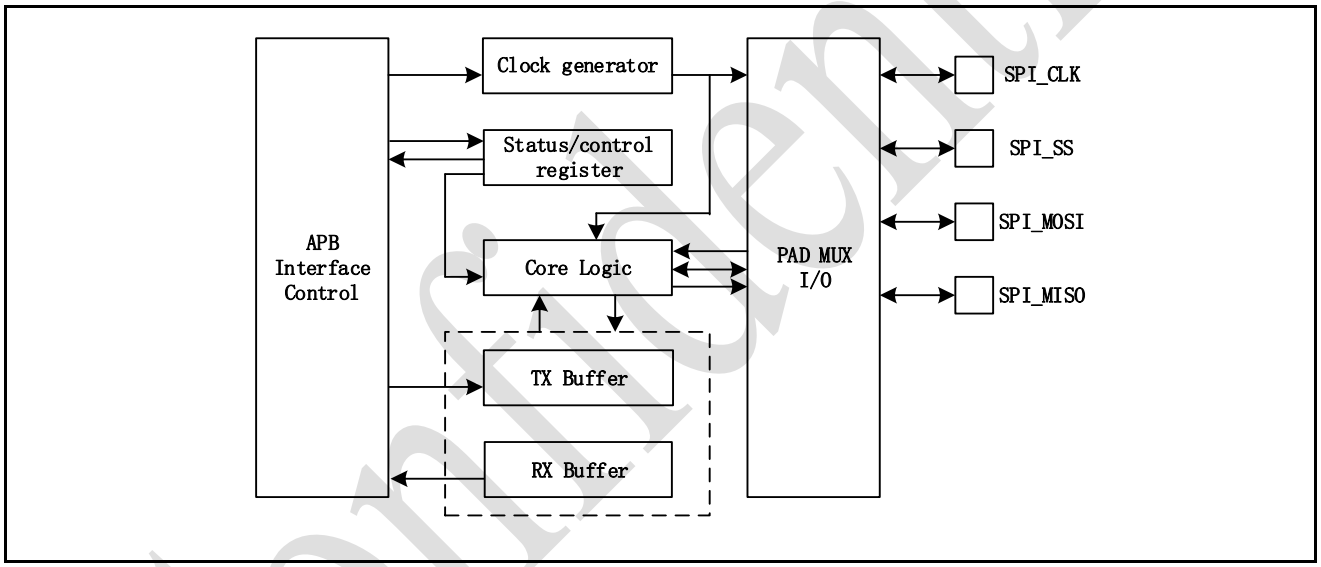

Figure 4-87 SPI Block Diagram

4.13.4 Basic Configuration

The SPI pin functions are configured in SYS_P0_MFP, SYS_P1_MFP, SYS_P2_MFP and SYS_P5_MFP register. The SPI0 peripheral clock can be enabled in CLK_APB1_EN[1].

4.13.5 Functional Description

4.13.5.1 Terminology

SPI Peripheral Clock and Serial Bus Clock

The SPI controller needs the SPI peripheral clock to drive the SPI logic unit to perform the data transfer. The SPI bus clock is the clock presented on SPI_CLK pin. The SPI peripheral clock frequency is determined by the settings of clock source, and clock divisor (SPI_CLKDIV[7:0]). The DIVIDER setting of SPI_CLKDIV register determines the divisor of the clock rate calculation.

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In SPI Master mode, the SPI peripheral clock is equal to the SPI bus clock.

In SPI Slave mode, the SPI bus clock is provided by an off-chip master device. The SPI peripheral clock frequency of slave device must be faster than the bus clock frequency of the master device connected together. The frequency of SPI peripheral clock cannot be faster than the APB clock frequency regardless of Master mode or Slave mode

Master/Slave Mode

The SPI controller can be set as Master or Slave mode by setting the SLAVE bit (SPI_CTL[18]) to communicate with the off-chip SPI slave or master device. The application block diagrams in Master and Slave mode are shown in Figure 4-88 and Figure 4-89.

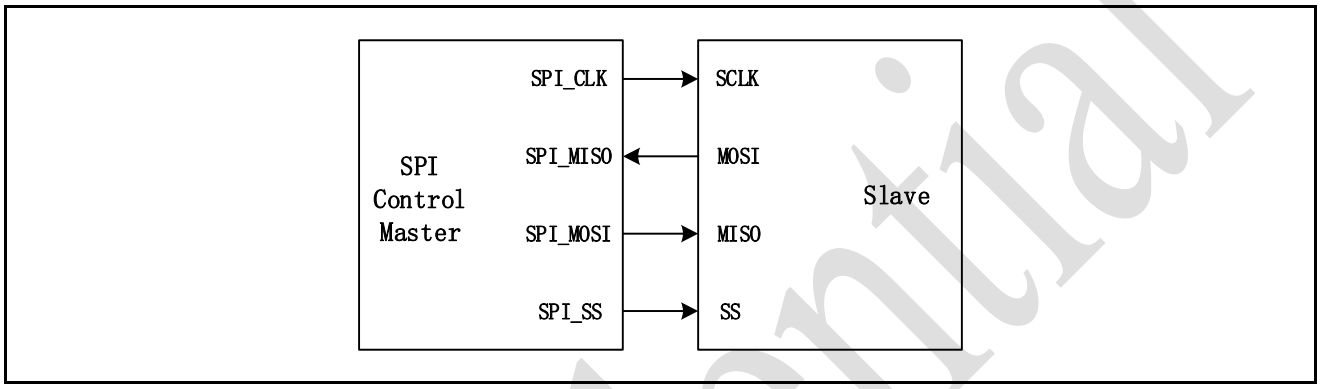

Figure 4-88 SPI Master Mode Application Block Diagram

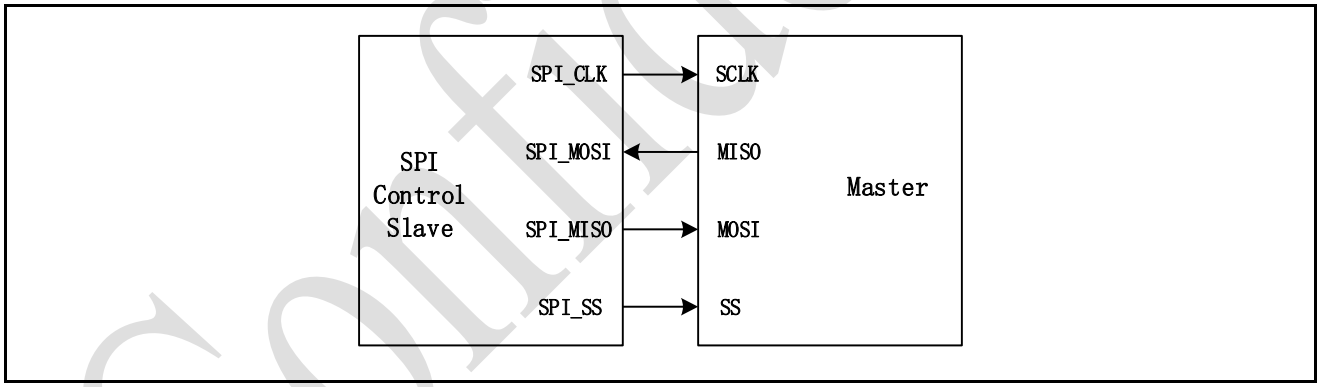

Figure 4-89 SPI Slave Mode Application Block Diagram

Clock Polarity

The CLKPOL bit (SPI_CTL[11]) defines the bus clock idle state. If CLKPOL = 1, the output SPI_CLK is high at idle state; otherwise it is at low if CLKPOL = 0.

Transmit/Receive Bit Length

The bit length of a transaction word is defined in DWIDTH bit field (SPI_CTL[7:3]). It can be configured up to 32-bit length in a transaction word to transmitting and receiving.

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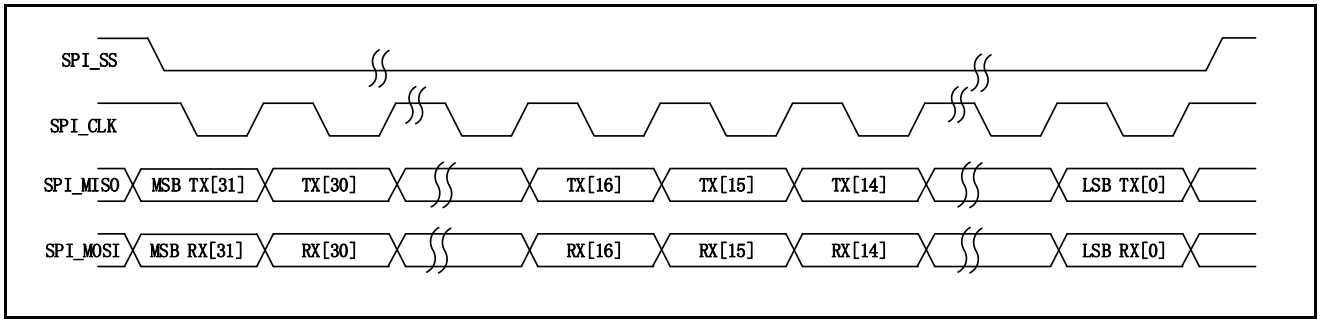

Figure 4-90 32 Bits in One Transaction

LSB/MSB First

The LSB bit (SPI_CTL[10]) de7-1fines the data transmission either from LSB or MSB firstly to start to transmit/receive data.

Transmit Edge

The TXNEG bit (SPI_CTL[2]) defines the data transmitted out either on negative-edge or on positive-edge of serial clock SPI_CLK.

Receive Edge

The RXNEG bit (SPI_CTL[1]) defines the data received in either on negative-edge or on positive-edge of serial clock SPI_CLK.

Note: the settings of TXNEG and RXNEG are mutual exclusive. In other words, do not transmit and receive data on the same clock edge.

Slave Selection

In Master mode, the SPI controller can drive one off-chip slave device through the slave select output pin SPI_SS. In Slave mode, the off-chip master device drives the slave select signal from the SPI_SS input pin to the SPI controller. In Master/Slave mode, the active state of slave selected signal can be programmed to low active or high active in SSACTPOL bit (SPI_SSCTL[2]). The selection of trigger condition depends on what type of peripheral slave/master device is connected.

In Slave mode, number of received bits meet the requirement which defined in DWIDTH (SPI_CTL[7:3]) among one transaction done (the transaction done means the unit transfer interrupt flag is set to 1 when the slave select signal is inactivated or the SPI controller finishes one data transfer).

Level-trigger / Edge-trigger

In Slave mode, the slave select signal can be configured as level-trigger or edge-trigger. In edge-trigger, the data transfer starts from an active edge of the slave select signal and ends on an inactive edge of the slave select signal. The unit-transfer interrupt flag UNITIF (SPI_CTL[16]) will be set to 1 as an inactive edge is detected. If master does not send an inactive edge to slave, the transfer procedure will not be completed and the unit-transfer interrupt flag of slave will not be set. In level-trigger, the unit-transfer interrupt flag of slave will be set when one of the following two conditions occurs. The first condition is that if the number of transferred bit matches the settings of DWIDTH (SPI_CTL[7:3]), the unit-transfer interrupt flag of slave will be set. The second condition, if master set the slave select pin to inactive level during the transfer in progress, it will force slave device to terminate the current transfer no matter how many bits have been transferred and the unit-transfer

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interrupt flag will be set.

4.13.5.2 Automatic Slave Select

In Master mode, if the bit AUTOSS (SPI_SSCTL[3]) is set, the slave select signal will be generated automatically and output to SPI_SS pin according to SS (SPI_SSCTL[0]) whether enabled or not. It means that the slave select signal, which is enabled in SS (SPI_SSCTL[0], is asserted by the SPI controller when transmit/receive is started by setting the SPIEN bit (SPI_CTL[0]) and is de-asserted after the data transfer is finished. If the AUTOSS bit is cleared, the slave select output signal will be asserted and de-asserted by manual setting and clearing the related bit in SS (SPI_SSCTL[0]). The active level of the slave select output signal is specified in SSACTPOL bit (SPI_SSCTL[2]).

4.13.5.3 Interrupt

SPI unit-transfer interrupt

As the SPI controller finishes a unit transfer, the unit transfer interrupt flag UNITIF (SPI_CTL[16]) will be set to 1. The unit transfer interrupt event will generate an interrupt to CPU if the unit transfer interrupt enable bit UNITIEN (SPI_CTL[17]) is set. The unit transfer interrupt flag can be cleared only by writing 1 to it.

SPI Slave Select Inactive Interrupt

If the SPI Slave Select from act from active to inactive, the slave select inactive flag SSINATF (SPI_SLVCTL[17]) will be set to 1. The slave select inactive interrupt flag SSINATIF (SPI_SLVCTL[18]) will be set if the slave select inactive interrupt enable bit SSINAIEN (SPI_SLVCTL [16]) is set. SSINATF and SSINATIF can be cleared only by writing 1 to it.

SPI Read Overrun Interrupt

If the previous received data (SPI_RX) is not read by CPU before the new data is received, the RXOVIF will set to 1and generate an interrupt to CPU when RXOVIEN is set. RXOVIF can be cleared only by writing 1 to it.

4.13.6 Timing Diagram

The active state of slave select signal can be defined by the settings of SSACTPOL bit (SPI_SSCTL[2]). The serial clock (SPI_CLK) idle state can be configured as high state or low state by setting the CLKPOL bit (SPI_CTL[11]). It also provides the bit length of a transaction word in DWIDTH (SPI_CTL[7:3]), and transmit/receive data from MSB or LSB first in LSB bit (SPI_CTL[10]). User also can select which edge of bus clock to transmit/receive data in TXNEG/RXNEG (SPI_CTL[2:1]). Four SPI timing diagrams for master/slave operations and the related settings are shown below.

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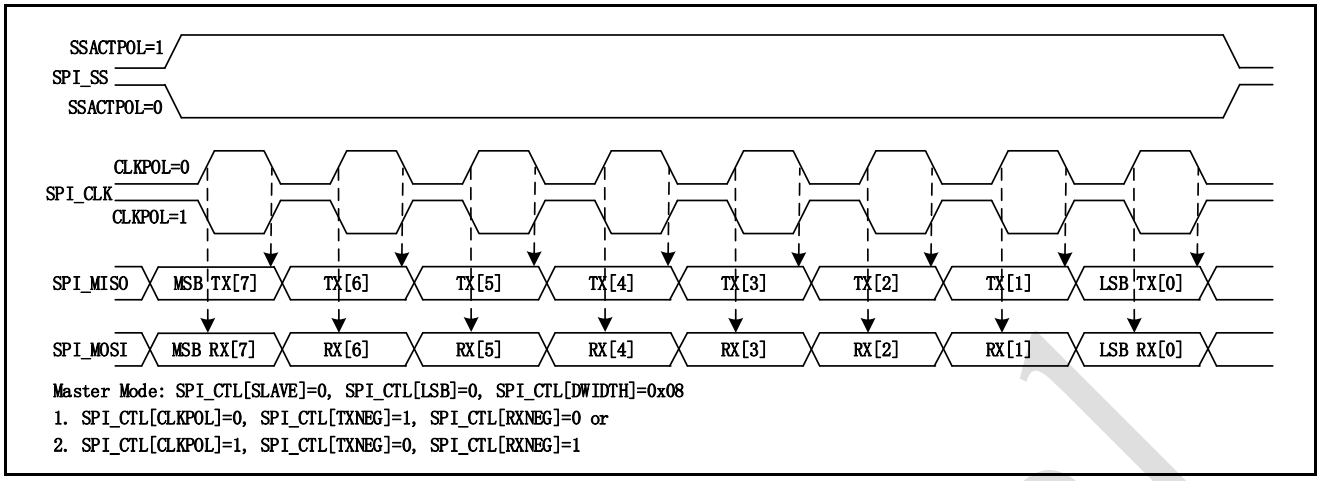

Figure 4-91 SPI Timing in Master Mode

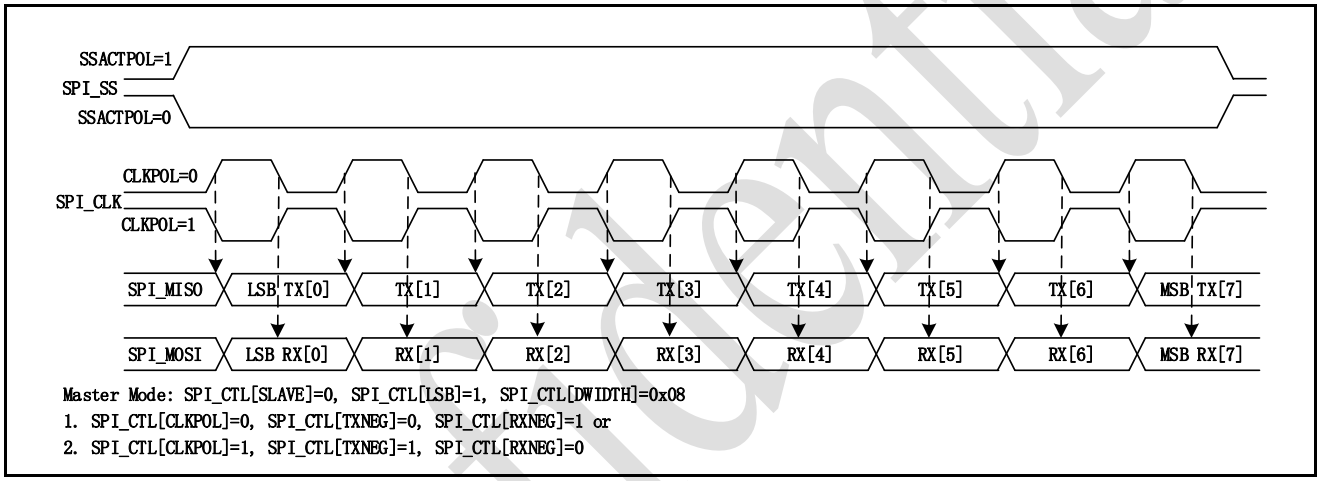

Figure 4-92 SPI Timing in Master Mode (Alternate Phase of SPI_CLK)

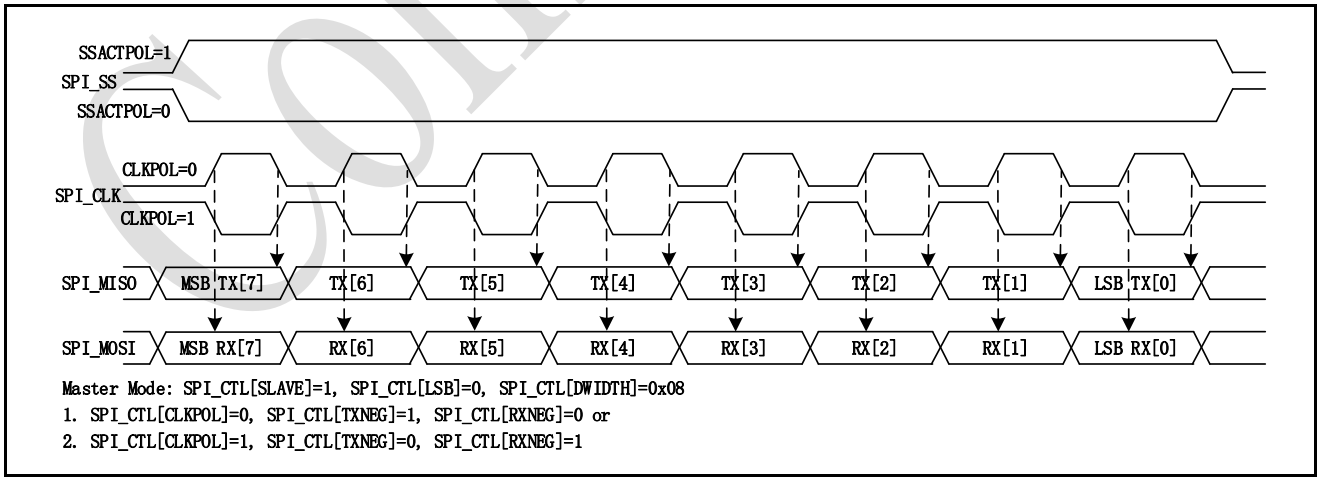

Figure 4-93 SPI Timing in Slave Mode

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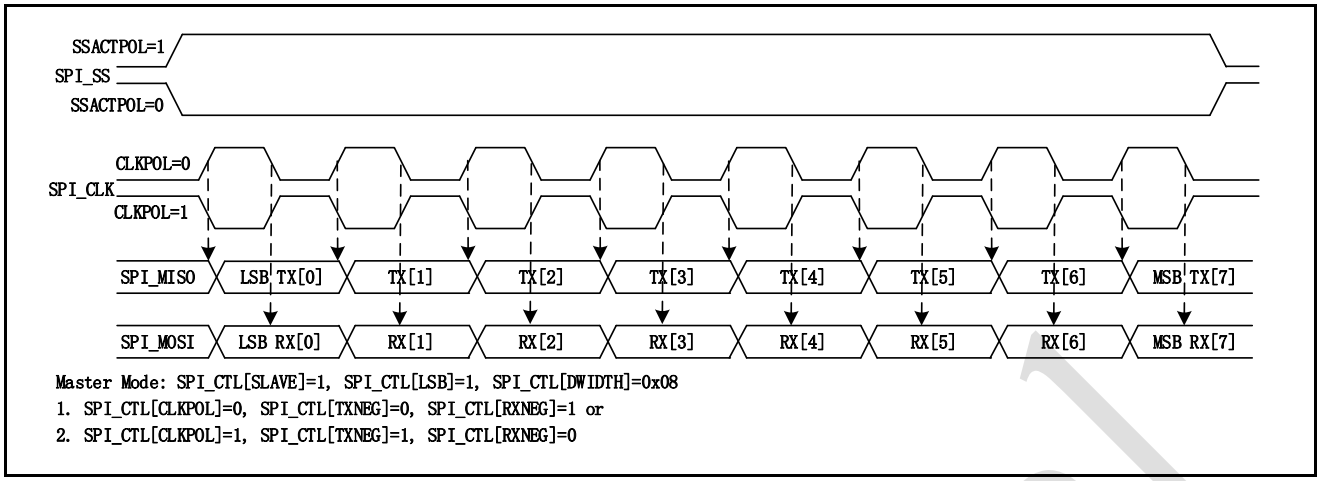

Figure 4-94 SPI Timing in Slave Mode (Alternate Phase of SPI_CLK)

Example 1: SPI controller is set as a master to access an off-chip slave device with following specifications:

- Data bit is latched at positive-edge of bus clock
- Data bit is driven at negative-edge of bus clock
- Data bit is transferred from MSB first
- Data width is 8 bits
- SPI_CLK is low at idle state
- Only one byte data is transmitted/received in a transaction
- Connect with an off-chip slave device. Slave select signal is active low

The operation flow is described follows.

1) Set the DIVIDER (SPI_CLKDIV[7:0]) to determine the output frequency of bus clock.

2) Write the related settings into the SPI_CTL register to control this SPI master actions

1. Set this SPI controller as master device in SLAVE bit (SPI_CTL[18] = 0)
2. Force the serial clock low at idle state in CLKPOL bit (SPI_CTL[11] = 0)
3. Select data transmitted at negative edge of bus clock in TXNEG bit (SPI_CTL[2] = 1)
4. Select data latched at positive edge of bus clock in RXNEG bit (SPI_CTL[1] = 0)
5. Set the bit length of word transfer as 8-bit in DWIDTH bit field (SPI_CTL[7:3] = 0x08)
6. Set MSB transfer first in LSB bit (SPI_CTL[10] = 0)

3) Write the SPI_SSCTL register a proper value for the related settings of Master mode.

1. Clear the Automatic Slave Select bit AUTOSS (SPI_SSCTL[3] = 0).
   Select low level trigger output of slave select signal in the Slave Select Active Level control bit, SSACTPOL (SPI_SSCTL[2] = 0).
2. Set the slave select signal to be active by setting the Slave Select control bit SS (SPI_SSCTL[0]) to active the off-chip slave device.

4) If this SPI master attempts to transmit (write) one byte data to the off-chip slave device, write the byte data that will be transmitted into the SPI_TX register.

5) If this SPI master just only attempts to receive (read) one byte data from the off-chip slave device and does not care what data will be transmitted, the software does not need to update the SPI_TX register.

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6) Set the SPIEN bit (SPI_CTL[0] = 1) to start the data transfer on the SPI interface.

7) Waiting for SPI interrupt (if the Unit-Transfer Interrupt Enable UNITIEN bit (SPI_CTL[17]) is set) or just polling the SPIEN bit (SPI_CTL[0]) till it is cleared to 0 by hardware automatically.

8) Read out the received one byte data from SPI_RX[7:0].

9) Go to 4) to continue another data transfer or set SS bit (SPI_SSCTL [0]) to 0 to inactivate the off-chip slave device.

Example 2: The SPI controller is set as a slave device that is connected by an off-chip master device. The off-chip master device communicates with the on-chip SPI slave controller through the SPI interface with the following specifications:

- Data bit is latched at positive-edge of bus clock
- Data bit is driven at negative-edge of bus clock
- Data bit is transferred from LSB first
- Data width is 8 bits
- SPI_CLK is high at idles state
- Only one byte data is transmitted/received in a transaction
- Slave select signal is high level trigger

The operation flow is as follows.

1) Write the SPI_SSCTL register a proper value for the related settings of Slave mode.

2) Select high level and level trigger for the input of slave select signal by setting the Slave Select Active Level control bit SSACTPOL (SPI_SSCTL[2] = 1)

3) Write the related settings into the SPI_CTL register to control this SPI slave actions

1. Set this SPI controller as slave device in SLAVE bit (SPI_CTL[18] = 1)
2. Select the serial clock as high at idle state in CLKPOL bit (SPI_CTL[11] = 1)
3. Select data transmitted at negative-edge of serial clock in TXNEG bit (SPI_CTL[2] = 1)
4. Select data latched at positive-edge of serial clock in RXNEG bit (SPI_CTL[1] = 0)
5. Set the bit length of word transfer as 8 bits in DWIDTH bit field (SPI_CTL[7:3] = 0x08)
6. Set LSB transfer first in LSB bit (SPI_CTL[10] = 1)

4) If this SPI slave attempts to transmit (be read) one byte data to the off-chip master device, write the byte data that will be transmitted into the SPI_TX register.

5) If this SPI slave just only attempts to receive (be written) one byte data from the off-chip master device and does not care what data will be transmitted, the SPI_TX does not need to be updated by software.

6) Set the SPIEN bit (SPI_CTL[0] = 1) to wait for the slave select trigger input and bus clock input from the off-chip master device to start the data transfer on the SPI interface.

7) Waiting for SPI interrupt (if the Unit-Transfer Interrupt Enable UNITIEN bit (SPI_CTL[17]) is set) or just polling the SPIEN bit (SPI_CTL[0]) until it is cleared to 0 by hardware automatically.

8) Read out the received one byte data from SPI_RX[7:0].

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9) Go to 4) to continue another data transfer or clear the SPIEN bit (SPI_CTL[0]) to stop data transfer.

4.13.7 SPI Register Map

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
SPI Base Address: **SPI0_BA = 0x4000_1000**				
SPI_CTL	SPI0_BA+0x00	R/W	SPI Control and Status Register	0x0000_0004
SPI_CLKDIV	SPI0_BA+0x04	R/W	SPI Clock Divider Register	0x0000_0001
SPI_SSCTL	SPI0_BA+0x08	R/W	SPI Slave Select Register	0x0000_0000
SPI_RX	SPI0_BA+0x10	R	SPI Data Receive Register	0x0000_0000
SPI_TX	SPI0_BA+0x20	W	SPI Data Transmit Register	0x0000_0000
SPI_SLVCTL	SPI0_BA+0x3C	R/W	SPI Slave Control and Status Register	0x0002_0000
SPI_FIFOCTL	SPI0_BA+0x40	R/W	SPI FIFO Control Register	0x0000_0000
SPI_STATUS	SPI0_BA+0x44	R/W	SPI Status Register	0x0002_0000

4.13.8 SPI Register Description

4.13.8.1 SPI Control and Status Register (SPI_CTL)

Register	Offset	R/W	Description	Reset Value
SPI_CTL	SPI0_BA+0x00	R/W	SPI Control and Status Register	0x0000_0004

Bits	Description	
[31:19]	Reserved	Reserved.
[18]	SLAVE	Slave Mode Control 0 = Master mode. 1 = Slave mode.
[17]	UNITIEN	Unit-transfer Interrupt Enable Bit 0 = SPI unit-transfer interrupt Disabled. 1 = SPI unit-transfer interrupt Enabled.
[16]	UNITIF	Unit-transfer Interrupt Flag 0 = The transfer does not finish yet. 1 = The SPI controller has finished one unit transfer. Note 1: This bit will be cleared by writing 1 to itself. Note 2: It's a mutual mirror bit of SPI_STATUS[16].
[15:12].	Reserved	Reserved
[11]	CLKPOL	Clock Polarity 0 = SPI_CLK idle low. 1 = SPI_CLK idle high.
[10]	LSB	LSB First 0 = The MSB is transmitted/received first.

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		1 = The LSB is transmitted/received first.
[9]	Reserved	Reserved.
[8]	UNITF	Unit-transfer Flag 0 = The transfer does not finish yet. 1 = The SPI controller has finished one unit transfer. Note 1: This bit will be cleared by writing 1 to itself. Note 2: It's a mutual mirror bit of SPI_STATUS[8].
[7:3]	DWIDTH	Transmit Bit Length This field specifies how many bits are transmitted in one transmit/receive. The minimum bit length is 8 bits and can up to 32 bits. DWIDTH = 0x01~0x07 …. reserved (can't use). DWIDTH = 0x08 …. 8 bits. DWIDTH = 0x09 …. 9 bits. …… DWIDTH = 0x1F …. 31 bits. DWIDTH = 0x00 …. 32 bits.
[2]	TXNEG	Transmit On Negative Edge 0 = The transmitted data output signal is driven on the rising-edge of SPI_CLK. 1 = The transmitted data output signal is driven on the falling-edge of SPI_CLK.
[1]	RXNEG	Receive On Negative Edge 0 = The received data input signal latched on the rising-edge of SPI_CLK. 1 = The received data input signal latched on the falling-edge of SPI_CLK.
[0]	SPIEN	SPI Transfer Control Bit And Busy Status During the data transfer, this bit keeps the value of 1. As the transfer is finished, this bit will be cleared automatically. 0 = No data transfer 1 = In Master mode, writing 1 to this bit to start the SPI data transfer; in Slave mode, writing 1 to this bit indicates that the slave is ready to communicate with a master. Note 1: All configurations should be ready before writing 1 to the SPIEN bit. Note 2: In SPI Slave mode, if the SPI bus clock is kept at idle state during a data transfer, the SPIEN bit will be cleared to 0 when slave select signal goes to inactive state.

4.13.8.2 SPI Clock Divider Register (SPI_CLKDIV)

Register	Offset	R/W	Description	Reset Value
SPI_CLKDIV	SPI0_BA+0x04	R/W	SPI Clock Divider Register	0x0000_0001

Bits	Description	
[31:8]	Reserved	Reserved.

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[7:0]	DIVIDER	Clock Divider Register (Master Only) The value in this field is the frequency divider to determine the SPI peripheral clock frequency fspi, and the SPI master's bus clock frequency on the SPI_CLK output pin. The frequency is obtained according to the following equation: $f_{spi} = \frac{f_{SPI_clock_src}}{(DIVIDER+1)*2}$ $f_{SPI_clock_src}$ is the SPI peripheral clock source.

4.13.8.3 SPI Slave Select Register (SPI_SSCTL)

Register	Offset	R/W	Description	Reset Value
SPI_SSCTL	SPI0_BA+0x08	R/W	SPI Slave Select Register	0x0000_0000

Bits	Description	
[31:4]	Reserved	Reserved.
[3]	AUTOSS	Automatic Slave Selection Function Enable Bit (Master Only) 0 = SPI_SS pin signal will be asserted/de-asserted by setting /clearing SS bit. 1 = SPI_SS pin signal will be generated automatically by hardware, which means that slave select signal will be asserted by the SPI controller when transmit/receive is started by setting SPIEN, and will be de-asserted after each transmit/receive is finished.
[2]	SSACTPOL	Slave Select Active Level (Slave Only) It defines the active status of slave select signal (SPI_SS). 0 = The slave select signal SPI_SS is active at low-level. 1 = The slave select signal SPI_SS is active at high-level.
[1]	Reserved	Reserved.
[0]	SS	Slave Select Control Bits (Master Only) If AUTOSS bit is 0, 0 = Set the SPI_SS line to inactive state. 1 = Set the SPI_SS line to active state. If AUTOSS bit is 1, 0 = Keep the SPI_SS line at inactive state. 1 = Select the SPI_SS line to be automatically driven to active state for the duration of transmission/reception, and will be driven to inactive state for the rest of the time. The active state of SPI_SS is specified in SSACTPOL bit.

4.13.8.4 SPI Data Receive Register (SPI_RX)

Register	Offset	R/W	Description	Reset Value
SPI_RX	SPI0_BA+0x10	R	SPI Data Receive Register	0x0000_0000

Bits	Description	
[31:0]	RX	Data Receive Register (Read Only) The Data Receive Register holds the value of received data of the last executed transfer. Valid

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		bits depend on the transmit bit length field DWIDTH in the SPI_CTL register. For example, if DWIDTH is set to 0x08, the bit field RX[7:0] holds the received data. The values of the other bits are unknown. The Data Receive Register is read-only register.

4.13.8.5 SPI Data Transmit Register (SPI_TX)

Register	Offset	R/W	Description	Reset Value
SPI_TX	SPI0_BA+0x20	R/W	SPI Data Transmit Register	0x0000_0000

Bits	Description	
[31:0]	TX	Data Transmit Register The Data Transmit Register holds the data to be transmitted in the next transfer. Valid bits depend on the transmit bit length field DWIDTH in the SPI_CTL register. For example, if DWIDTH is set to 0x08, the bit filed TX[7:0] will be transmitted in next transfer.

4.13.8.6 SPI Slave Control and Status Register (SPI_SLVCTL)

Register	Offset	R/W	Description	Reset Value
SPI_SLVCTL	SPI0_BA+0x3C	R/W	SPI Slave Control and Status Register	0x0002_0000

Bits	Description	
[31:19]	Reserved	Reserved.
[18]	SSINATIF	Slave Select Inactive Interrupt Flag 0 = Slave Select Inactive does not checked yet. 1 = Slave Select Inactive does checked. Note 1: This bit will be cleared by writing 1 to itself. Note 2: It's a mutual mirror bit of SPI_STATUS[18].
[17]	SSINATF	Slave Select Inactive Flag 0 = Slave Select Inactive does not checked yet. 1 = Slave Select Inactive does checked. Note 1: This bit will be cleared by writing 1 to itself. Note 2: It's a mutual mirror bit of SPI_STATUS[17].
[16]	SSINAIEN	Slave Select Inactive Interrupt Option (Master/Slave) 0 = As the slave select signal goes to inactive level, the IF bit will NOT be set to 1. 1 = As the slave select signal goes to inactive level, the IF bit will be set to 1.
[15:0]	Reserved	Reserved.

4.13.8.7 SPI FIFO Control Register (SPI_FIFOCTL)

Register	Offset	R/W	Description	Reset Value
SPI_FIFOCTL	SPI0_BA+0x40	R/W	SPI FIFO Control Register	0x0000_0000

Bits	Description	
[31:7]	Reserved	Reserved.
[6]	RXOVIEN	Receive Data Overrun Interrupt Enable Bit

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		0 = Receive Data overrun interrupt Disabled. 1 = Receive Data overrun interrupt Enabled.
[5:0]	Reserved	Reserved.

4.13.8.8 SPI Status Register (SPI_STATUS)

Register	Offset	R/W	Description	Reset Value
SPI_STATUS	SPI0_BA+0x44	R/W	SPI Status Register	0x0002_0000

Bits	Description	
[31:19]	Reserved	Reserved.
[18]	SSINATIF	Slave Select Inactive Interrupt Flag 0 = Slave Select Inactive does not checked yet. 1 = Slave Select Inactive does checked. Note 1: This bit will be cleared by writing 1 to itself. Note 2: It's a mutual mirror bit of SPI_SLVCTL[18].
[17]	SSINATF	Slave Select Inactive Flag 0 = Slave Select Inactive does not checked yet. 1 = Slave Select Inactive does checked. Note 1: This bit will be cleared by writing 1 to itself. Note 2: It's a mutual mirror bit of SPI_SLVCTL[17].
[16]	UNITIF	SPI Unit-transfer Interrupt Flag 0 = The transfer does not finish yet. 1 = The SPI controller has finished one unit transfer. Note 1: This bit will be cleared by writing 1 to itself. Note 2: It's a mutual mirror bit of SPI_CTL[16].
[15:9]	Reserved	Reserved.
[8]	UNITF	Unit-transfer Flag 0 = The transfer does not finish yet. 1 = The SPI controller has finished one unit transfer. Note 1: This bit will be cleared by writing 1 to itself. Note 2: It's a mutual mirror bit of SPI_CTL[8].
[7:3]	Reserved	Reserved.
[2]	RXOVIF	Receive Data Overrun Status If the previous received data (SPI_RX) is not read by CPU before the new data is received, the RXOVIF will set to 1and generate an interrupt to CPU when RXOVIEN is set. 0 = No overrun happen. 1 = Overrun happen. Note: This bit will be cleared by writing 1 to itself.
[1:0]	Reserved	Reserved.

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4.14 Analog-to-Digital Converter (ADC)

4.14.1 Overview

The PAN2025 contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with nine input channels. The A/D converters can be started by software, external pin (STADC/P3.2) or PWM trigger.

4.14.2 Features

- Two selectable analog input voltage ranges:
  - 0 ~ 2V, with large measuring range and low precision, generated from bandgap output.
  - 0 ~ VDD, with small measuring range and high precision.
  - Input range < 2V, 0 ~ 2V is recommended.
    Input range ≥ 2V, 0 ~ VDD is recommended for PAN2025BX and PAN2025BY.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to eight single-end analog input channels, one bandgap input channel, one RSSI input channel, one GND check channel and one Voltage input channel.
- Maximum ADC clock frequency is 16 MHz, and 14 ADC clocks per sample
- Two operating modes
  - Single mode: A/D conversion is performed once on a specified channel
  - PWM sequence mode: When PWM triggers, two of the three ADC channels from 0 to 2 will automatically convert analog data in the sequence of channel [0,1] or channel[1,2] or channel[0,2] defined by MODESEL (ADC_SEQCTL[3:2])
- An A/D conversion can be started by
  - Software write 1 to SWTRG bit
  - External pin STADC
  - PWM trigger with optional start delay period
- Each Conversion result is held in data register with valid and overrun indicators
- Conversion results can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting

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4.14.3 Block Diagram

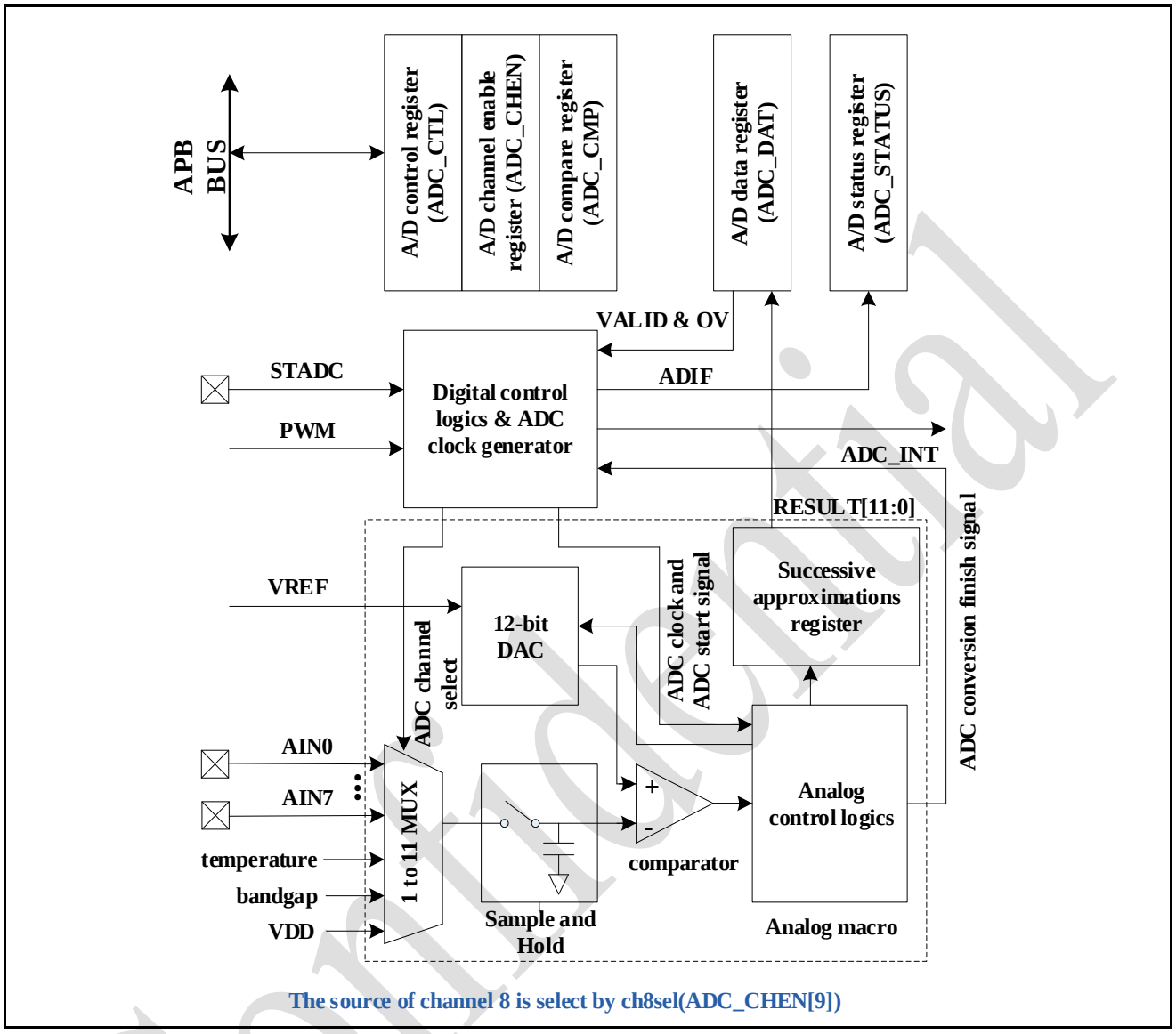

Figure 4-95 A/D Controller Block Diagram

4.14.4 Basic Configuration

The ADC pin functions are configured in SYS_P0_MFP, SYS_P1_MFP, SYS_P2_MFP, SYS_P3_MFP and SYS_P5_MFP register. It is recommended to disable the digital input path of the analog input pins to avoid the leakage current. User can disable the digital input path by configuring P0_DINOFF, P1_DINOFF, P2_DINOFF, P3_DINOFF and P5_DINOFF register.

The ADC peripheral clock can be enabled in adccken (CLK_APB1_EN[8]).

4.14.5 Functional Description

The A/D converter operates by successive approximation with 12-bit resolution. When changing the analog input channel is enabled, in order to prevent incorrect operation, software must clear SWTRG bit to 0 in the ADC_CTL register. The A/D converter discards the current conversion immediately and enters idle state while SWTRG bit is cleared.

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4.14.5.1 ADC Operation

A/D conversion is performed only once on the specified single channel. The operation is as follows:

1. A/D conversion will be started when the SWTRG bit of ADC_CTL is set to 1 by software or external trigger input.

2. When A/D conversion finished, the result is stored in the A/D data register.

3. The ADIF bit of ADC_STATUS register will be set to 1. If the ADCIEN bit of ADC_CTL register is set to 1, the ADC interrupt will be asserted.

4. The SWTRG bit remains 1 during A/D conversion. When A/D conversion ends, the SWTRG bit is automatically cleared to 0 and the A/D converter enters idle state.

5. Figure 4-96 shows an example timing diagram for Single mode.

Note: If software enables more than one channel, the channel with the smallest number will be selected and the other enabled channels will be ignored.

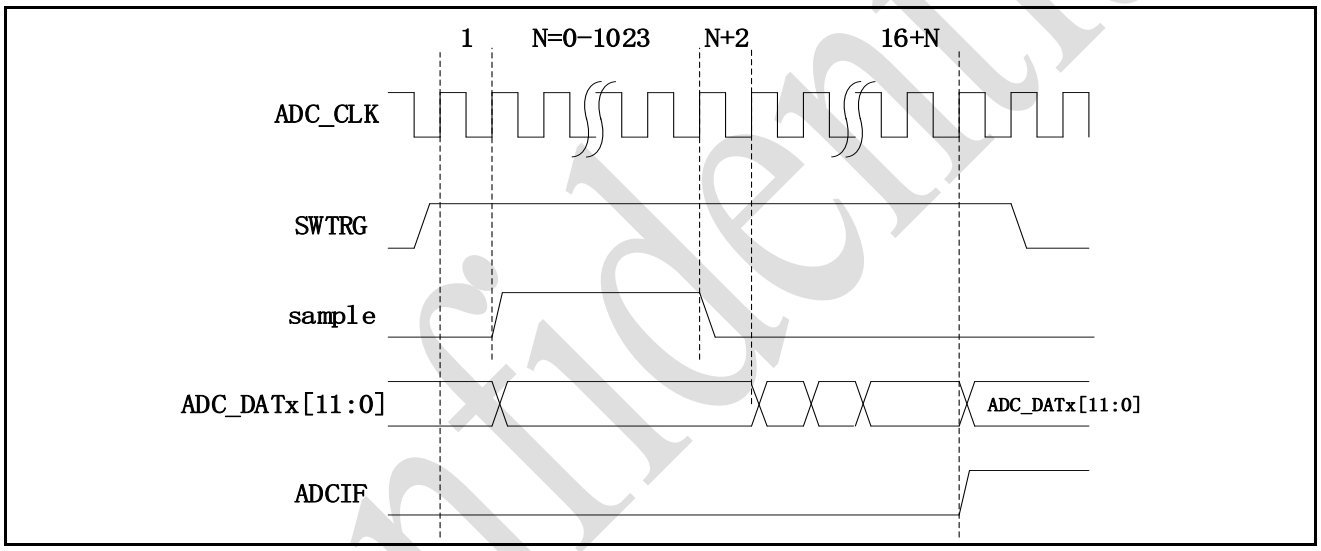

Figure 4-96 Single Mode Conversion Timing Diagram

4.14.5.2 External Trigger Input Sampling and A/D Conversion Time

A/D conversion can be triggered by external pin request. When the HWTRGEN (ADC_CTL[8]) bit is set to 1 to enable ADC external trigger function, setting the HWTRGSEL (ADC_CTL[5:4]) bits to 00b is to select external trigger input from the STADC pin. Software can set HWTRGCOND to select trigger condition between falling or rising edge. An 8-bit sampling counter is used to deglitch. If edge trigger condition is selected, the high and low state must be kept at least 4 SYS_CLK. Pulse that is shorter than this specification will be ignored.

4.14.5.3 PWM Trigger

A/D conversion can also be triggered by PWM request. When the HWTRGEN is set to high to enable ADC external hardware trigger function, setting the HWTRGSEL (ADC_CTL[5:4]) bits to 11b is to select external hardware trigger input source from PWM trigger. When PWM trigger is enabled, setting DELAY (ADC_TRGDLY[7:0]) bits can insert a delay time between PWM trigger condition and ADC start conversion.

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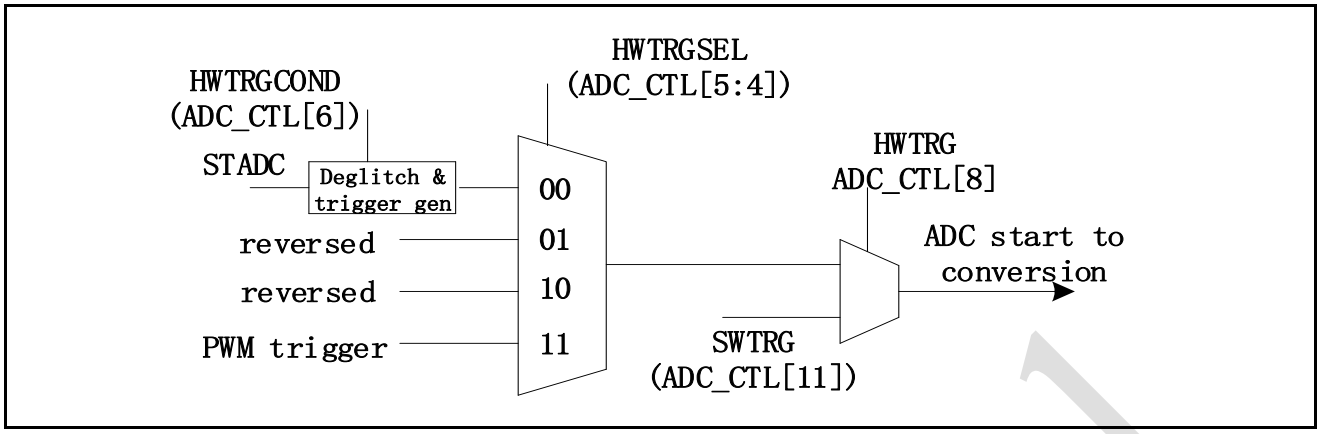

Figure 4-97 ADC Start Conversion Conditions

4.14.5.4 Conversion Result Monitor by Compare Mode Function

The PAN2025 ADC controller provides two compare registers, ADC_CMP0 and ADC_CMP1, to monitor maximum two specified channels. Software can select which channel to be monitored by setting CMPCH (ADC_CMPx[5:0]). CMPCOND bit is used to determine the compare condition. If CMPCOND bit is cleared to 0, the internal match counter will increase one when the conversion result is less than the value specified in CMPDAT (ADC_CMPx[25:16]) ; if CMPCOND bit is set to 1, the internal match counter will increase one when the conversion result is greater than or equal to the value specified in CMPDAT[11:0]. When the conversion of the channel specified by CMPCH is completed, the comparing action will be triggered one time automatically. When the compare result meets the setting, compare match counter will increase 1, otherwise, the compare match counter will be clear to 0. When the match counter reaches the setting of (CMPMCNT+1) then ADCMPIF bit will be set to 1, if ADCMPIE bit is set then an ADC_INT interrupt request is generated. Software can use it to monitor the external analog input pin voltage transition in scan mode without imposing a load on software. Figure 4-98 show detailed logic diagram.

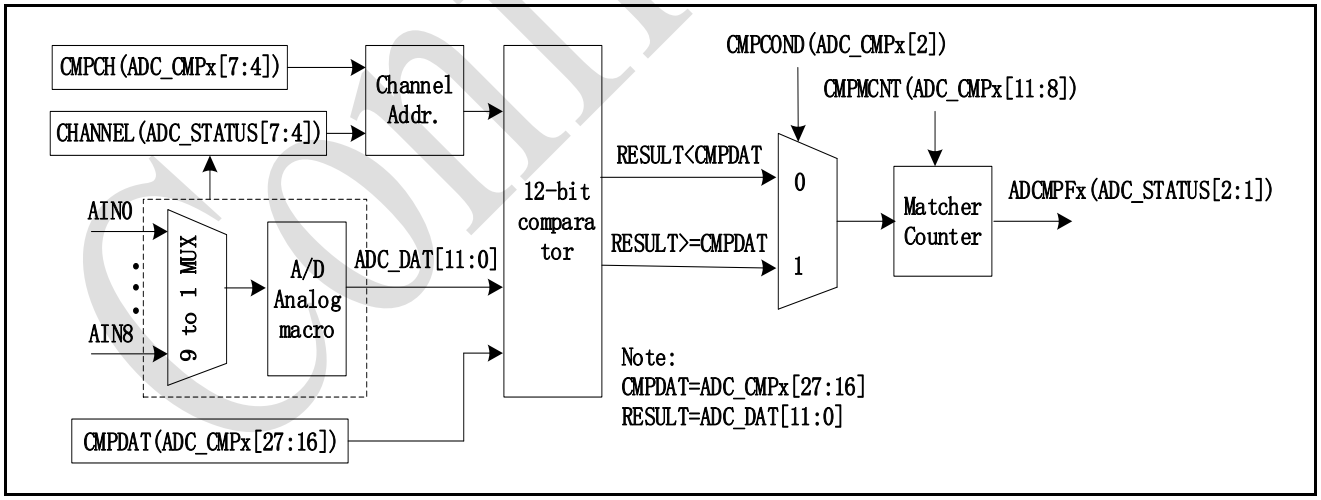

Figure 4-98 A/D Conversion Result Monitor Logics Diagram

4.14.5.5 Interrupt Sources

There are three interrupt sources of ADC interrupt. When an ADC operation mode finishes its conversion, the A/D conversion end flag, ADIF, will be set to 1. The ADCMPIF0 and ADCMPIF1 are the compare flags of compare function. When the conversion result meets the settings of

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ADC_CMP0/1, the corresponding flag will be set to 1. When one of the flags, ADIF, ADCMPIF0 and ADCMPIF1, is set to 1 and the corresponding interrupt enable bit, ADCIEN of ADC_CTL and ADCMPIE of ADC_CMP0/1, is set to 1, the ADC interrupt will be asserted. Software can clear these flags to revoke the interrupt request.

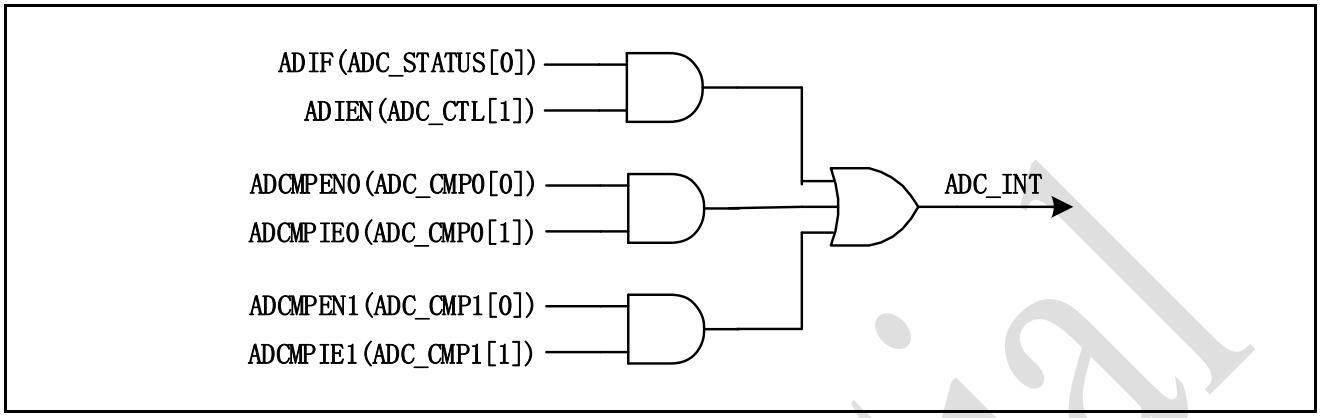

Figure 4-99 A/D Controller Interrupt

4.14.5.6 Flag Sources

There are three flag sources of ADC conversion. When an ADC operation mode finishes its conversion, the A/D conversion end flag, ADCF, will be set to 1. The ADCMPF0 and ADCMPF1 are the compare flags of compare function. When the conversion result meets the settings of ADC_CMP0/1, the corresponding flag will be set to 1. .

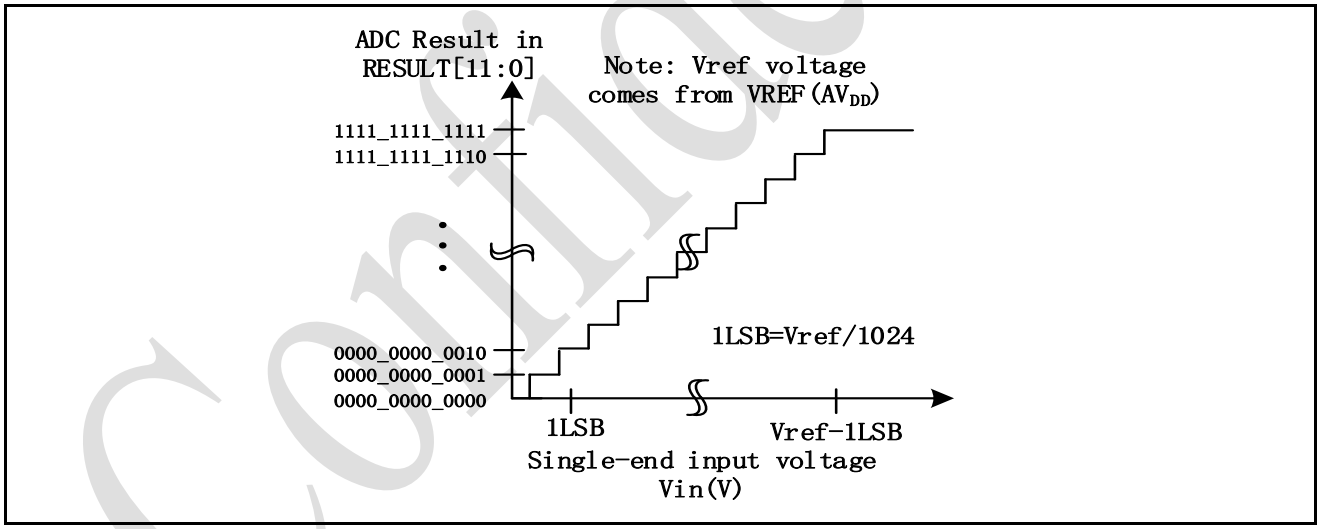

Figure 4-100 Conversion Result Mapping Diagram of ADC Single-end Input

4.14.5.7 PWM Sequential

Support sequential mode for 2 channels to reduce half interrupt frequency. When the SEQEN (ADC_SEQCTL[0]) is set to high to enable A/D PWM sequential function, setting the TRG1CTL (ADC_SEQCTL[11:8]) and TRG2CTL (ADC_SEQCTL[19:16]) are to select external trigger input from the PWM channel 0/2/4, type can be rising/center/falling/period, When ADC sequential mode is enabled, two of three ADC channels from 0 to 2 will automatically convert analog data in the sequence of channel [0, 1] or channel[1,2] or channel[0,2] defined by MODESEL (ADC_SEQCTL[3:2]). By the way, if SEQTYPE (ADC_SEQCTL[1]) is set to low, ADC delay time is only

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inserted before the first conversion. The second conversion starts immediately after the first conversion is completed. (for 2/3- shunt type), if SEQTYPE (ADC_SEQCTL[1]) is set to high, ADC delay time is inserted before each conversion. (for 1-shunt type), By the way, Valid ADC channel are CH0~2 in 2/3-shunt type, Valid ADC channel are CH0~8 in 1-shunt type, Figure 4-101 and Figure 4-102 show the function diagram.

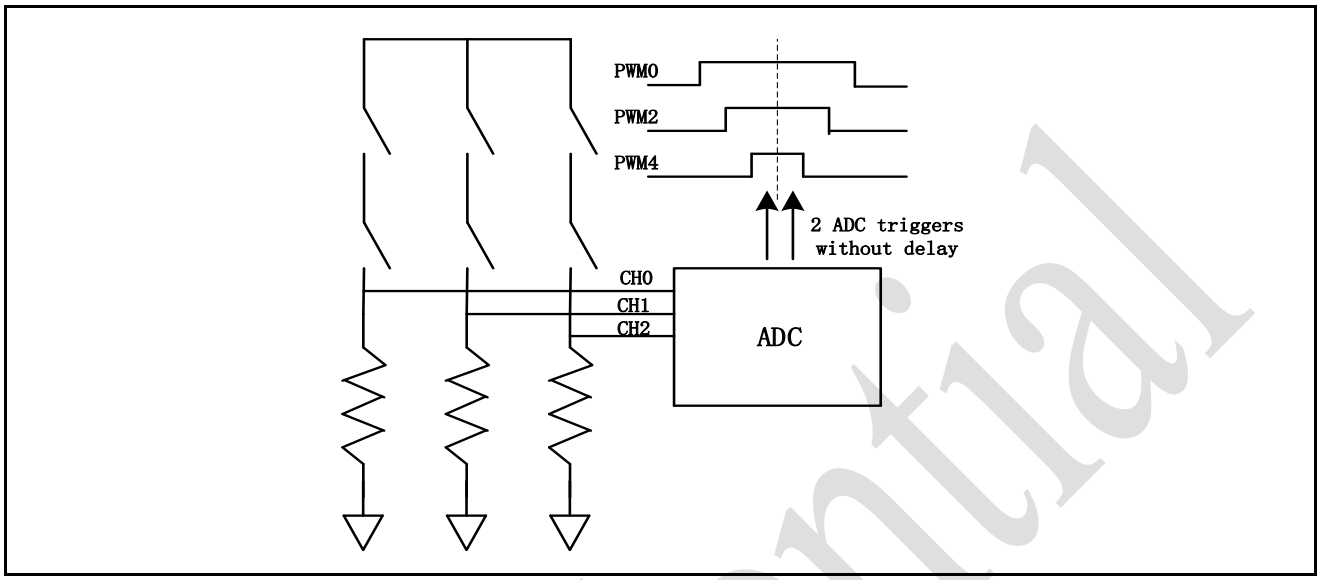

Figure 4-101 ADC Sequential Mode Type is 2/3-shunt

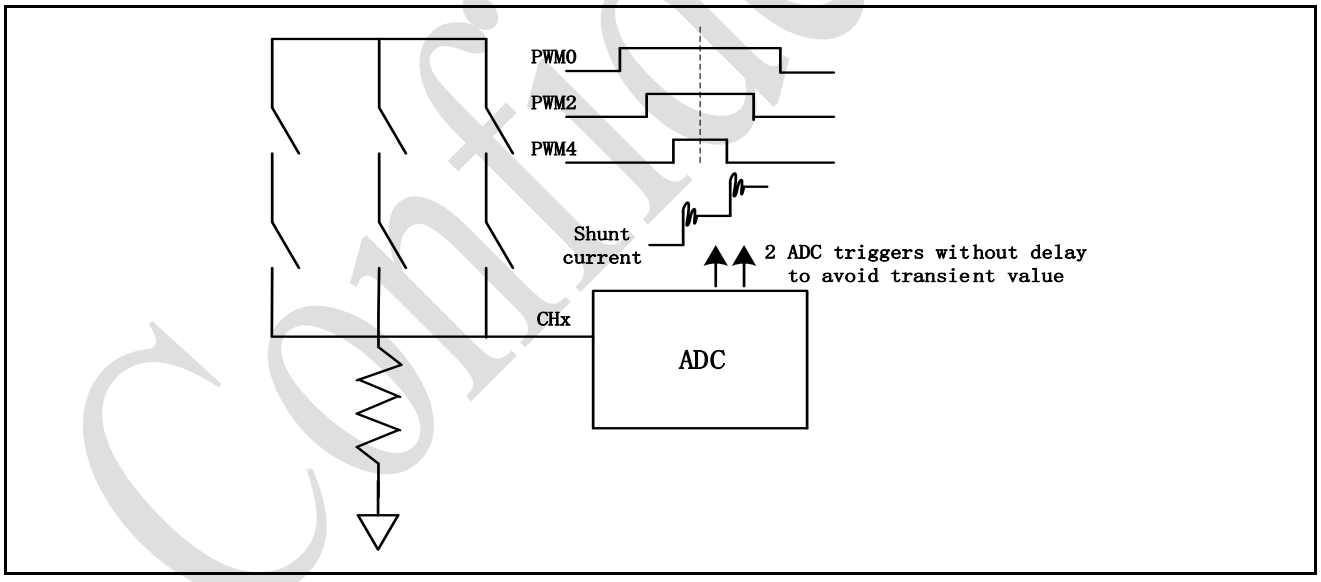

Figure 4-102 ADC Sequential Mode Type is 1-shunt

4.14.6 ADC Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
ADC Base Address:				

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ADC_BA = 0x4000_5000				
ADC_DAT	ADC_BA+0x00	R	A/D Data Register	0x0000_0000
ADC_CTL	ADC_BA+0x20	R/W	A/D Control Register	0x0000_0000
ADC_CHEN	ADC_BA+0x24	R/W	A/D Channel Enable Register	0x0000_0000
ADC_CMP0	ADC_BA+0x28	R/W	A/D Compare Register 0	0x0000_0000
ADC_CMP1	ADC_BA+0x2C	R/W	A/D Compare Register 1	0x0000_0000
ADC_STATUS	ADC_BA+0x30	R/W	A/D Status Register	0x0000_0000
ADC_TRGDLY	ADC_BA+0x44	R/W	A/D Trigger Delay Control Register	0x0000_0000
ADC_EXTSMPT	ADC_BA+0x48	R/W	A/D Sampling Time Counter Register	0x0000_0002
ADC_SEQCTL	ADC_BA+0x4C	R/W	A/D PWM Sequential Mode Control Register	0x0000_0000
ADC_SEQDAT1	ADC_BA+0x50	R	A/D PWM Sequential Mode First Result Register1	0x0000_0000
ADC_SEQDAT2	ADC_BA+0x54	R	A/D PWM Sequential Mode Second Result Register1	0x0000_0000
ADC_CTL2	ADC_BA+0x58	R/W	A/D Control Register 2	0x0101_0000

4.14.7 ADC Register Description

4.14.7.1 ADC Data Register (ADC_DAT)

Register	Offset	R/W	Description	Reset Value
ADC_DAT	ADC_BA+0x00	R	A/D Data Register	0x0000_0000

Bits	Description	
[31:18]	Reserved	Reserved.
[17]	VALID	Valid Flag This bit is set to 1 when ADC conversion is completed and cleared by hardware after the ADC_DAT register is read. 0 = Data in RESULT[11:0] bits not valid. 1 = Data in RESULT[11:0] bits valid.
[16]	OV	Over Run Flag If converted data in RESULT[11:0] has not been read before the new conversion result is loaded to this register, OV is set to 1. It is cleared by hardware after the ADC_DAT register is read. 0 = Data in RESULT[11:0] is recent conversion result. 1 = Data in RESULT[11:0] overwrote.
[15:12]	Reserved	Reserved.
[11:0]	RESULT	A/D Conversion Result This field contains conversion result of ADC.

4.14.7.2 ADC Control Register (ADC_CTL)

Register	Offset	R/W	Description	Reset Value
ADC_CTL	ADC_BA+0x20	R/W	A/D Control Register	0x0000_0000

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Bits	Description	
[31:12]	Reserved	Reserved.
[11]	SWTRG	Software Trigger A/D Conversion Start SWTRG bit can be set to 1 from two sources: software and external pin STADC. SWTRG will be cleared to 0 by hardware automatically after conversion complete. 0 = Conversion stopped and A/D converter entered idle state. 1 = Conversion start.
[10:9]	Reserved	Reserved.
[8]	HWTRGEN	Hardware External Trigger Enable Bit Enable or disable triggering of A/D conversion by external STADC pin. If external trigger is enabled, the SWTRG bit can be set to 1 by the selected hardware trigger source. 0= External trigger disabled. 1= External trigger enabled.
[7]	Reserved	Reserved.
[6]	HWTRGCOND	Hardware External Trigger Condition This bit decides whether the external pin STADC trigger event is falling or raising edge. The signal must be kept at stable state at least 4 SYS_CLK at high and low state for edge trigger. 0 = Falling edge. 1 = Raising edge.
[5:4]	HWTRGSEL	Hardware Trigger Source Select Bit 00 = A/D conversion is started by external STADC pin. 11 = A/D conversion is started by PWM trigger. Others = Reserved. Note: Software should disable TRGEN and SWTRG before change TRGS.
[3:2]	Reserved	Reserved.
[1]	ADCIEN	A/D Interrupt Enable Bit A/D conversion end interrupt request is generated if ADCIEN bit is set to 1. 0 = A/D interrupt function disabled. 1 = A/D interrupt function enabled.
[0]	ADCEN	A/D Converter Enable Bit 0 = A/D Converter disabled. 1 = A/D Converter enabled. Note: Before starting A/D conversion function, this bit should be set to 1. Clear it to 0 to disable A/D converter analog circuit to save power consumption.

4.14.7.3 ADC Channel Enable Register (ADC_CHEN)

Register	Offset	R/W	Description	Reset Value
ADC_CHEN	ADC_BA+0x24	R/W	A/D Channel Enable Register	0x0000_0000

Bits	Description	
[31:13]	Reserved	Reserved.
[12]	CHEN12	Temperature check Enable Bit

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		0 = Temperature check disabled. 1 = Temperature check enabled.
[11]	CHEN11	GND check Enable Bit 0 = GND check disabled. 1 = GND check enabled.
[10]	CHEN10	VDD/2 check Enable Bit 0 = VDD/2 check disabled. 1 = VDD/2 check enabled.
[9]	CHEN9	Bandgap check Enable Bit 0 = bandgap check disabled. 1 = bandgap check enabled.
[8]	CHEN8	RSSI check Enable Bit 0 = RSSI check disabled. 1 = RSSI check enabled.
[7]	CHEN7	Analog Input Channel 7 Enable Bit 0 = Channel 7 disabled. 1 = Channel 7 enabled.
[6]	CHEN6	Analog Input Channel 6 Enable Bit 0 = Channel 6 disabled. 1 = Channel 6 enabled.
[5]	CHEN5	Analog Input Channel 5 Enable Bit 0 = Channel 5 disabled. 1 = Channel 5 enabled.
[4]	CHEN4	Analog Input Channel 4 Enable Bit 0 = Channel 4 disabled. 1 = Channel 4 enabled.
[3]	CHEN3	Analog Input Channel 3 Enable Bit 0 = Channel 3 disabled. 1 = Channel 3 enabled.
[2]	CHEN2	Analog Input Channel 2 Enable Bit 0 = Channel 2 disabled. 1 = Channel 2 enabled.
[1]	CHEN1	Analog Input Channel 1 Enable Bit 0 = Channel 1 disabled. 1 = Channel 1 enabled.
[0]	CHEN0	Analog Input Channel 0 Enable Bit 0 = Channel 0 disabled. 1 = Channel 0 enabled. Note: If software enables more than one channel, the channel with the smallest number will be selected and the other enabled channels will be ignored.

4.14.7.4 A/D Compare Register 0/1 (ADC_CMP0/1)

Register	Offset	R/W	Description	Reset Value

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ADC_CMP0	ADC_BA+0x28	R/W	A/D Compare Register 0	0x0000_0000
ADC_CMP1	ADC_BA+0x2C	R/W	A/D Compare Register 1	0x0000_0000

Bits	Description	
[31:28]	Reserved	Reserved.
[27:16]	CMPDAT	Comparison Data The 12-bit data is used to compare with conversion result of specified channel.
[15:12]	Reserved	Reserved.
[11:8]	CMPMCNT	Compare Match Count When the specified A/D channel analog conversion result matches the compare condition defined by CMPCOND[2], the internal match counter will increase 1. When the internal counter reaches the value to (CMPMCNT+1), the ADCMPFx bit will be set.
[7]	Reserved	Reserved.
[6:3]	CMPCH	Compare Channel Selection Set this field to select which channel's result to be compared. Note: Valid setting of this field is channel 0~7.
[2]	CMPCOND	Compare Condition 0 = Set the compare condition as that when a 12-bit A/D conversion result is less than the 12-bit CMPDAT (ADC_CMPx[25:16]), the internal match counter will increase one. 1 = Set the compare condition as that when a 12-bit A/D conversion result is greater or equal to the 12-bit CMPDAT (ADC_CMPx[25:16]), the internal match counter will increase one. Note: When the internal counter reaches the value to (CMPMCNT+1), the ADCMPFx bit will be set.
[1]	ADCMPIE	A/D Compare Interrupt Enable Bit If the compare function is enabled and the compare condition matches the setting of CMPCOND and CMPMCNT, ADCMPIE bit will be asserted, in the meanwhile, if ADCMPIE is set to 1, a compare interrupt request is generated. 0 = Compare function interrupt Disabled. 1 = Compare function interrupt Enabled.
[0]	ADCMPEN	A/D Compare Enable Bit Set 1 to this bit to enable comparing CMPDAT (ADC_CMPx[25:16]) with specified channel conversion results when converted data is loaded into the ADC_DAT register. 0 = Compare function Disabled. 1 = Compare function Enabled.

4.14.7.5 A/D Status Register (ADC_STATUS)

Register	Offset	R/W	Description	Reset Value
ADC_STATUS	ADC_BA+0x30	R/W	A/D Status Register	0x0000_0000

Bits	Description	
[31:27]	Reserved	Reserved.
[26]	ADCMPF1	A/D Compare Flag 1

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		When the selected channel A/D conversion result meets the setting condition in ADC_CMP1, this bit is set to 1. 0 = Conversion result in ADC_DAT does not meet the ADC_CMP1 setting. 1 = Conversion result in ADC_DAT meets the ADC_CMP1 setting. Note: This bit can be cleared to 0 by software writing 1.
[25]	ADCMPF0	A/D Compare Flag 0 When the selected channel A/D conversion result meets the setting condition in ADC_CMP0, this bit is set to 1. 0 = Conversion result in ADC_DAT does not meet the ADC_CMP0 setting. 1 = Conversion result in ADC_DAT meets the ADC_CMP0 setting. Note: This bit can be cleared to 0 by software writing 1.
[24]	ADCF	A/D Conversion End Flag A status flag that indicates the end of A/D conversion. ADIF is set to 1 When A/D conversion ends. Note: This bit can be cleared to 0 by software writing 1.
[23:17]	Reserved	Reserved.
[16]	OV	Overrun Flag (Read Only) It is a mirror to OV bit in ADC_DAT register.
[15:9]	Reserved	Reserved.
[8]	VALID	Data Valid Flag (Read Only) It is a mirror of VALID bit in ADC_DAT register.
[7:4]	CHANNEL	Current Conversion Channel (Read Only) This filed reflects the current conversion channel when BUSY=1. When BUSY=0, it shows the number of the next converted channel.
[3]	BUSY	BUSY/IDLE (Read Only) This bit is mirror of as SWTRG bit in ADC_CTL 0 = A/D converter is in idle state. 1 = A/D converter is busy at conversion.
[2]	ADCMPIF1	A/D Compare Interrupt Flag 1 When the selected channel A/D conversion result meets the setting condition in ADC_CMP1, this bit is set to 1. 0 = Conversion result in ADC_DAT does not meet the ADC_CMP1 setting. 1 = Conversion result in ADC_DAT meets the ADC_CMP1 setting. Note: This bit can be cleared to 0 by software writing 1.
[1]	ADCMPIF0	A/D Compare Interrupt Flag 0 When the selected channel A/D conversion result meets the setting condition in ADC_CMP0, this bit is set to 1. 0 = Conversion result in ADC_DAT does not meet the ADC_CMP0 setting. 1 = Conversion result in ADC_DAT meets the ADC_CMP0 setting. Note: This bit can be cleared to 0 by software writing 1.
[0]	ADIF	A/D Conversion End Interrupt Flag A status flag that indicates the end of A/D conversion. ADIF is set to 1 When A/D conversion ends.

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		Note: This bit can be cleared to 0 by software writing 1.

4.14.7.6 A/D Trigger Delay Controller Register (ADC_TRGDLY)

Register	Offset	R/W	Description	Reset Value
ADC_TRGDLY	ADC_BA+0x44	R/W	A/D Trigger Delay Control Register	0x0000_0000

Bits	Description	
[31:8]	Reserved	Reserved.
[7:0]	DELAY	PWM Trigger Delay Timer Set this field will delay ADC start conversion time after PWM trigger. PWM trigger delay time is (4 * DELAY) * system clock.

4.14.7.7 A/D Sampling Register (ADC_EXTSMPT)

Register	Offset	R/W	Description	Reset Value
ADC_EXTSMPT	ADC_BA+0x48	R/W	A/D Sampling Time Counter Register	0x0000_0010

Bits	Description	
[31:5]	Reserved	Reserved.
[4:0]	EXTSMPT	Additional ADC Sample Clock If the ADC input is unstable, user can set this register to increase the sampling time to get a stable ADC input signal. The default sampling time is 2 ADC clocks. 1-16 ADC clock number will be inserted to lengthen the sampling clock. Set 0 will disable ADC

4.14.7.8 A/D PWM Sequential Register (ADC_SEQCTL)

Register	Offset	R/W	Description	Reset Value
ADC_SEQCTL	ADC_BA+0x4C	R/W	A/D PWM Sequential Mode Control Register	0x0000_0000

Bits	Description	
[31:20]	Reserved	Reserved.
[19:16]	TRG2CTL	PWM Trigger Source Selection For TRG2CTL[3:2] 00 = PWM Trigger source is PWM0_CH0. 01 = PWM Trigger source is PWM0_CH 2. 10 = PWM Trigger source is PWM0_CH 4. 11 = PWM Trigger source is PWM0_CH 6. PWM Trigger Type Selection for TRG2CTL[1:0] 00 = Rising of the selected PWM. 01 = Center of the selected PWM. 10 = Falling of the selected PWM. 11 = Period of the selected PWM.

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		Note: PWM trigger source is valid for 1-shunt type and 2/3-shunt type.
[15:12]	Reserved	Reserved.
[11:8]	TRG1CTL	PWM Trigger Source Selection For TRG1CTL[3:2] 00 = PWM Trigger source is PWM0_CH 0. 01 = PWM Trigger source is PWM0_CH 2. 10 = PWM Trigger source is PWM0_CH 4. 11 = PWM Trigger source is PWM0_CH 6. PWM Trigger Type Selection for TRG1CTL[1:0] 00 = Rising of the selected PWM. 01 = Center of the selected PWM. 10 = Falling of the selected PWM. 11 = Period of the selected PWM. Note: PWM trigger source is valid for 1-shunt and 2/3-shunt type.
[7:6]	Reserved	Reserved.
[5]	TRG_SEL	TRG1CTL or TRG2CTL select for 1-shunt sequential mode. 0 = using TRG1CTL to trigger sequential conversion; 1 = using TRG2CTL to trigger sequential conversion;
[4]	DE-LAY_EN	ADC delay time inserted before 2nd conversion. 0 = ADC delay time only inserted before the 1st conversion; 1 = ADC delay time inserted before each conversion.
[3:2]	MODESEL	ADC Sequential Mode Selection 00 = Issue ADC_INT after Channel 0 then Channel 1 conversion finishes when SEQEN =1. 01 = Issue ADC_INT after Channel 1 then Channel 2 conversion finishes when SEQEN =1. 10 = Issue ADC_INT after Channel 0 then Channel 2 conversion finishes when SEQEN =1. 11 = Reserved.
[1]	SEQTYPE	ADC Sequential Mode Type 0 = 2/3-shunt type 1 = 1-shunt type
[0]	SEQEN	ADC Sequential Mode Enable Bit When ADC sequential mode is enabled, two of three ADC channels from 0 to 2 will automatically convert analog data in the sequence of channel [0, 1] or channel[1, 2] or channel[0, 2] defined by MODESEL (ADC_SEQCTL[3:2]). 0 = ADC sequential mode Disabled. 1 = ADC sequential mode Enabled.

4.14.7.9 A/D PWM Sequential Mode Result Register (ADC_SEQDAT1/2)

Register	Offset	R/W	Description	Reset Value
ADC_SEQDAT1	ADC_BA+0x50	R	A/D PWM Sequential Mode First Result Register1	0x0000_0000
ADC_SEQDAT2	ADC_BA+0x54	R	A/D PWM Sequential Mode Second Result Register1	0x0000_0000

Bits	Description	
[31:18]	Reserved	Reserved.

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[17]	VALID	Valid Flag This bit is set to 1 when ADC conversion is completed and cleared by hardware after the ADC_SEQDATx register is read. 0 = Data in RESULT[11:0] bits not valid. 1 = Data in RESULT[11:0] bits valid.
[16]	OV	Over Run Flag If converted data in RESULT[11:0] has not been read before the new conversion result is loaded to this register, OV is set to 1. It is cleared by hardware after the ADC_SEQDATx register is read. 0 = Data in RESULT[11:0] is recent conversion result. 1 = Data in RESULT[11:0] overwritten.
[15:12]	Reserved	Reserved.
[11:0]	RESULT	A/D PWM Sequential Mode Conversion Result This field contains conversion result of ADC.

4.14.7.10 ADC Control Register 2 (ADC_CTL2)

Register	Offset	R/W	Description	Reset Value
ADC_CTL2	ADC_BA+0x58	R/W	A/D Control Register 2	0x7550_0900

Bits	Description	
[31]	Reserved	Reserved.
[30:28]	ICTL_CMP	Comparator current control bits. 000 = 0 uA 001 = 0.25 uA 010 = 0.75 uA …(Step size = 0.25 uA) 111 = 1.5 uA Default value : 0x111
[27]	Reserved	Reserved.
[26:24]	ICTL_VCM	VCM reference voltage driving current control bits. 000 = 0 uA 001 = 0.25 uA 010 = 0.75 uA ⋯(Step size = 0.25 uA) 111 = 1.5 uA Default value : 0x101
[23]	Reserved	Reserved.
[22:20]	ICTL_VREF	2.4V reference voltage driving current control bits. 000 = 0 uA 001 = 0.25 uA 010 = 0.75 uA ⋯(Step size = 0.25 uA) 111 = 1.5 uA Default value : 0x101

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[19:18]	Reserved	Reserved.
[17]	SEL_VREF	Reference voltage selection. 1 = VDD is selected, VCM is equal to 1/2 VDD. 0 = 2V is selected, VCM is equal to 1V. Default value : 0x0
[16]	EN_BUFTST	Vtop output voltage test enable bit. 1 = Enable 0 = Disable Default value : 0
[15:14]	Reserved	Reserved.
[13:11]	CLK_DIV_DUTY	ADC Duty Divider Could not be set as 0. Default : 1
[10:8]	CLK_DIV	ADC Clock Divider Could not be set as 0. Default : 1
[7:3]	Reserved	Reserved.
[2]	DMA_EN	ADC DMA enable bit. 1 = Enable 0 = Disable Default value : 0
[1]	SEL_SH	1 = SH is SH. 0 = External Sample Hold (SH) width with HOLD2(Internal Signal) Default : 0
[0]	TEST_MODE	ADC Test enable bit. 1 = Enable 0 = Disable

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5 Electrical Characteristics

All the parameters are accurate to the one decimal place.

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Symbol	Description	Parameter			Unit
		Min	Typ	Max	
VDD	VDD1/VDD2	-0.3	-	3.6	V
V_I	Input Voltage	-0.3	-	VDD	V
V_O	Output Voltage	VSS	-	VDD	V
T_{OP}	Operating Temperature	-40	-	85	℃
T_{STG}	Storage Temperature	-40	-	125	℃

Note: Exceeding one or more of the limiting values may cause permanent damage to PAN2025.

Caution: Electrostatic sensitive device, comply with protection rules when operating.

5.2 DC Electrical Characteristics

Table 5-2 Voltage and Current

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VDD1/VDD2	Power Supply	2.2	3	3.6	V	TA=25℃
VSS	Ground	-	0	-	V	-
$I_{DP_SLP_RC}$	Deep sleep current	30	60	-	uA	MCU power down, SRAM maintain, HCLK off, 32K RC on
I_{ST_M0}	Standby Current	-	0.2	-	uA	External interrupts, CPU Power Down
I_{ST_M1}	Standby Current	-	1	-	uA	External interrupts, CPU Power Down, SRAM retention
I_{ST_M2}	Standby Current	-	2.5	-	uA	Sleep timer running, CPU Power Down
I_{ST_M3}	Standby Current	-	3.3	-	uA	Sleep timer running, CPU Sleep, SRAM retention
$I_{TX,0dBm}$	Operating Current of TX mode	-	50	-	mA	0dBm output power
$I_{TX,8dBm}$	Operating Current of TX mode	-	66	-	mA	8dBm output power
$I_{TX,10dBm}$	Operating Current of TX mode	-	68	-	mA	10dBm output power
I_{RX}	Operating Current of RX mode	-	40	-	mA	Maximum LNA gain
V_{OH}	Output High Level Voltage	VDD-0.3	-	VDD	V	-

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V_{OL}	Output Low Level Voltage	VSS	-	VSS+0.3	V	-
V_{IH}	Input High Level Voltage	2.0	3	3.6	V	-
V_{IL}	Input Low Level Voltage	VSS	-	VSS+0.3	V	-

5.3 16 MHz Crystal Oscillator Characteristics

Table 5-3 16M RC Oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{XTAL(16M)}$	Crystal Oscillator Frequency	-	-	16	-	MHz
ESR(16M)	Equivalent Series Resistance	-	-	-	80	Ω
$\Delta f_{XTAL(16M)}$	Crystal Frequency Tolerance	-	-20	-	20	ppm
$V_{CLK(EXT)(16M)}$	External Clock Voltage	-	0.1	0.8	-	V
φN(EXTERNAL)16M	Phase Noise	f_C = 50 kHz in case of an external reference clock	-	-	-130	dBc/Hz

5.4 Stable Low Frequency RCX Oscillator Characteristics

Table 5-4 Stable Low Frequency RCX Oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{RC(RCX)}$	RCX Oscillator Frequency	Default setting,	-	40	-	Khz

5.10 Digital Input/Output Characteristics

Table 5-5 Digital Input/Output Characteristics

Symbol	Paramter	Conditions	Min	Type	Max	Unit
RSTN pin						
V_{IH}	HIGH level input voltage	2.2≤VDD<3.6	0.6xVDD	-	VDD	V
V_{IL}	LOW level input voltage	2.2≤VDD<3.6	0	-	0.4xVDD	V
V_{hys}	Hysteresis voltage	2.2≤VDD<3.6	0.05xVDD	-	-	V
Standard I/O pins						
Input characteristics						
V_{IH}	HIGH level input voltage	2.2≤VDD<3.6	0.6xVDD	-	VDD	V
V_{IL}	LOW level input voltage	2.2≤VDD<3.6	0	-	0.4xVDD	V
V_{hys}	Hysteresis voltage	2.2≤VDD<3.6	0.05xVDD	-	-	V
Output characteristics						
V_O	Output voltage	Output active	0	-	VDD	V
V_{OH}	HIGH level output voltage	2.2≤VDD<3.6	VDD	-	-	V
V_{OL}	LOW level output voltage	2.2≤VDD<3.6	-	-	0	V
I_{OH}	HIGH level output current	VDD=3.3	-	20	-	mA
I_{OL}	LOW level output current	VDD=3.3	-	35	-	mA

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R_{PD}	Pull down resistor	2.2≤VDD<3.6	-	40	-	kΩ
R_{PU}	Pull up resistor	2.2≤VDD<3.6	-	40	-	kΩ

5.11 AC Electrical Characteristics

Table 5-6 RF

Symbol	Condition	Min	Typ	Max	Unit
General frequency					
Fop	Operating Frequency	2400	-	2483	MHz
PLL_{res}	PLL Programming Resolution	-	1	-	MHz
F_{xtal}	Crystal Frequency	-	16	-	MHz
DR	Data Rate	-	1	-	Mbps
Transmitter					
PRF	Output Power	2	8	10	dBm
PRFC	Output Power Range	-16	-	-10	dBm
PBW	20dB Bandwidth for Modulated Carrier at 1Mbps	950	-	1100	MHz
MDR	Maximum Drift Rate	-	-	13	KHz/50us
FD	Frequency Deviation	200	-	300	KHz
Receiver					
RXmax	Maximum Received Signal at <0.1% BER	-	0	-	dBm
RXSENS	Sensitivity (0.1%BER) @1Mbps, GFSK	-	-91	-	dBm
	Sensitivity (0.1%BER) @1Mbps, DSSS	-	-100	-	dBm
	Sensitivity (0.1%BER) @250Kbps, GFSK	-	-94	-	dBm
C/ICO	C/I Co-channel Interference	-	14	-	dBc
C/I1M	Adjacent 1MHz Interference	-	2	-	dBc
C/I2M	Adjacent 2MHz Interference	-	-16	-	dBc
C/I≥3M	Adjacent ≥ 3MHz Interference	-	-26	-	dBc
C/Iimage	Image Frequency Interference	-	-12	-	dBc
C/Iimage±1M	Adjacent（1MHz）Interference to In-band Image Frequency	-	-35	-	dBc
P_IMD	Intermodulation Interference	-	-45	-	dBm
P_Blocking	Out-of-band Blocking Interference	-30	-	-	dBm

Table 5-7 DPLL

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD2	Power Supply	2.2	-	3.6	V	-
T_A	Temperature	-40	-	85	℃	-
F_{in}	Input Clock Frequency	-	16	-	MHz	-
F_{DPLL}	Clock Frequency	-	48	72	MHz	-

Table 5-8 ADC

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Symbol	Parameter	Min	Typ	Max	Unit	Notes
-	Resolution	-	10	-	Bit	-
VDD2	Power Supply	2.5(for VTOP=2.4V) 2.2(for VTOP=1.4V)	-	3.6	VDDA	-
ITOT	Operation Current	880	-	1600	uA	-
INL	Integral Nonlinearity Error	-	-	±2	LSB	-
SYS_CLK	System Clock	-	-	48	MHz	-
Fadc	Clock Frequency	-	-	48	MHz	-
FS	Sample Rate	-	-	1.625	MHz	-
Ts	Sample Time	7	-	-	SYS_CLK	-
Th	Compare Time	25	-	-	SYS_CLK	-
TCONV	Data Output cycle	32	50	170	SYS_CLK	-
N	S-H counter	1	2	7	-	-
Vin	Analog input voltage	0 0	-	VDD 2.0	V	-
Cin	Input Capacitance	-	10	-	pF	-
Rin	Input resistance	14.6	-	-	KΩ	See Note1
Vref	ADC reference voltage	-	VBG	-	V	-
DATA	ADC Output	000	-	FFF	HEX	-
SFDR	Spurious Free Dynamic range	-	64	-	dB	-

Note:

Sample time formula:

Ts= (EXTSMPT+1) *(ADCDIV +1)*T0

Continuous mode period formula:

T=(EXTSMPT+14) *(ADCDIV +1)* T0+2T0

T0: System clock, the maximum to 1/52M, or chosen as 1/26M, 1/13M.

Maximum resistance formula:

$$Rin < \frac{Ts}{Csample \ x \ ln(2^{N+1})} - R_{adc}$$

Ts: Sample Time, see the Table 5-8 for specific ranges. It is required to be stable within the DAC establishment period.

Csample: Sample capacitance =10pF

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N：ADC bit defaults as 12. If the accuracy requirement is not high, it can be taken as 11,10,9,8, which can reduce the requirement of input impedance.

Radc：Sample switch resistance, 100Ω~300Ω.

Table 5-9 LVR

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD2	Power Supply	2.2	3	3.6	V	-
VLVR	Threshold Voltage	-	1.9	-	V	-

Table 5-10 BOD

Symbol	Parameter	Vout(V) 1→0	Vout(V) 0→1	Test Conditions	Notes
V_{BOD}	Brown-Out Detector	2.0	2.1	EN_BOD=1 BODVL<2:0>=000	-
		2.2	2.3	EN_BOD=1 BODVL<2:0>=001	-
		2.5	2.6	EN_BOD=1 BODVL<2:0>=010	-
		2.7	2.8	EN_BOD=1 BODVL<2:0>=011	-
		3.0	3.1	EN_BOD=1 BODVL<2:0>=101	-

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6 Application Reference Design

6.1 QFN32 Application Reference Design

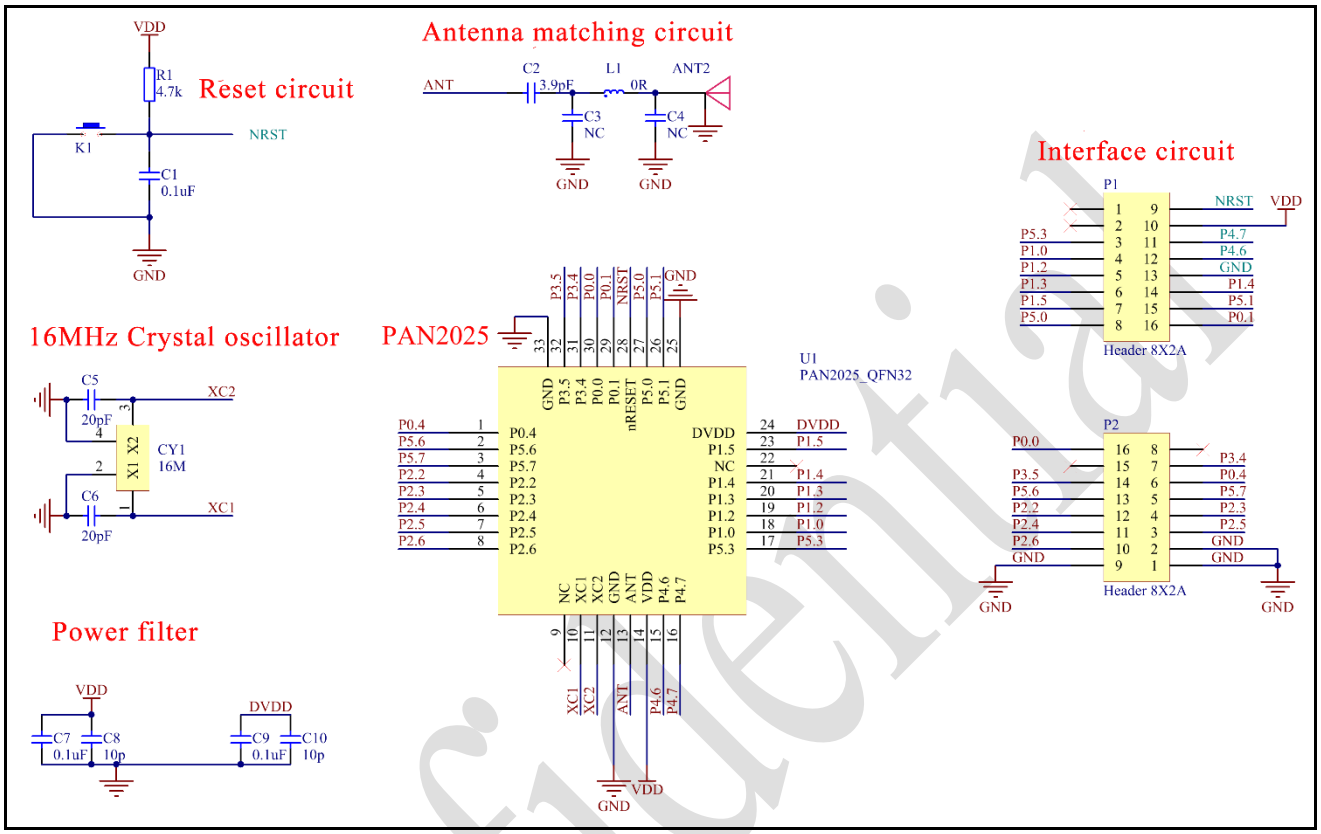

Figure 6-1 Application Reference Circuit for QFN32

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6.2 QFN40 Application Reference Design

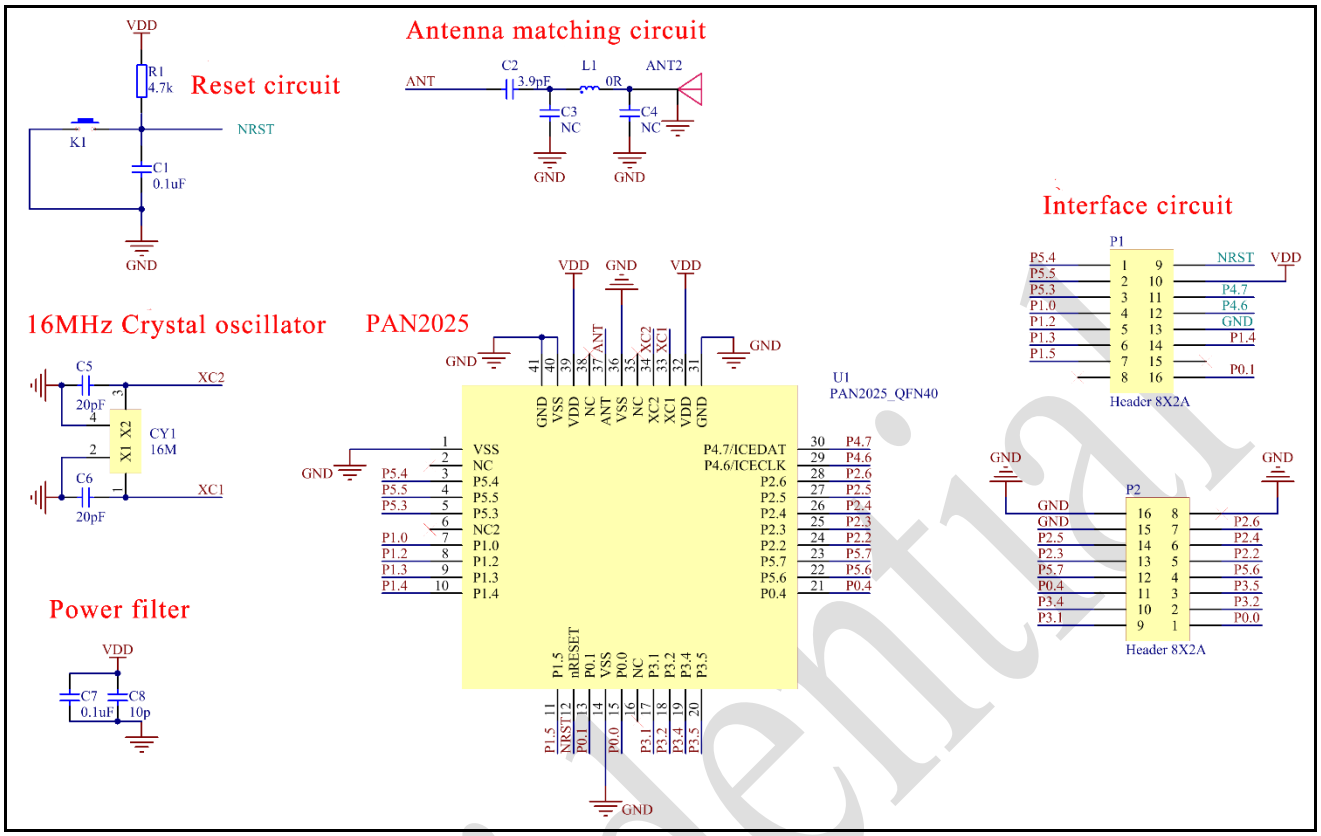

Figure 6-2 Application Reference Circuit for QFN40

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7 Pakage Dimensions

7.1 QFN32 Package Dimensions

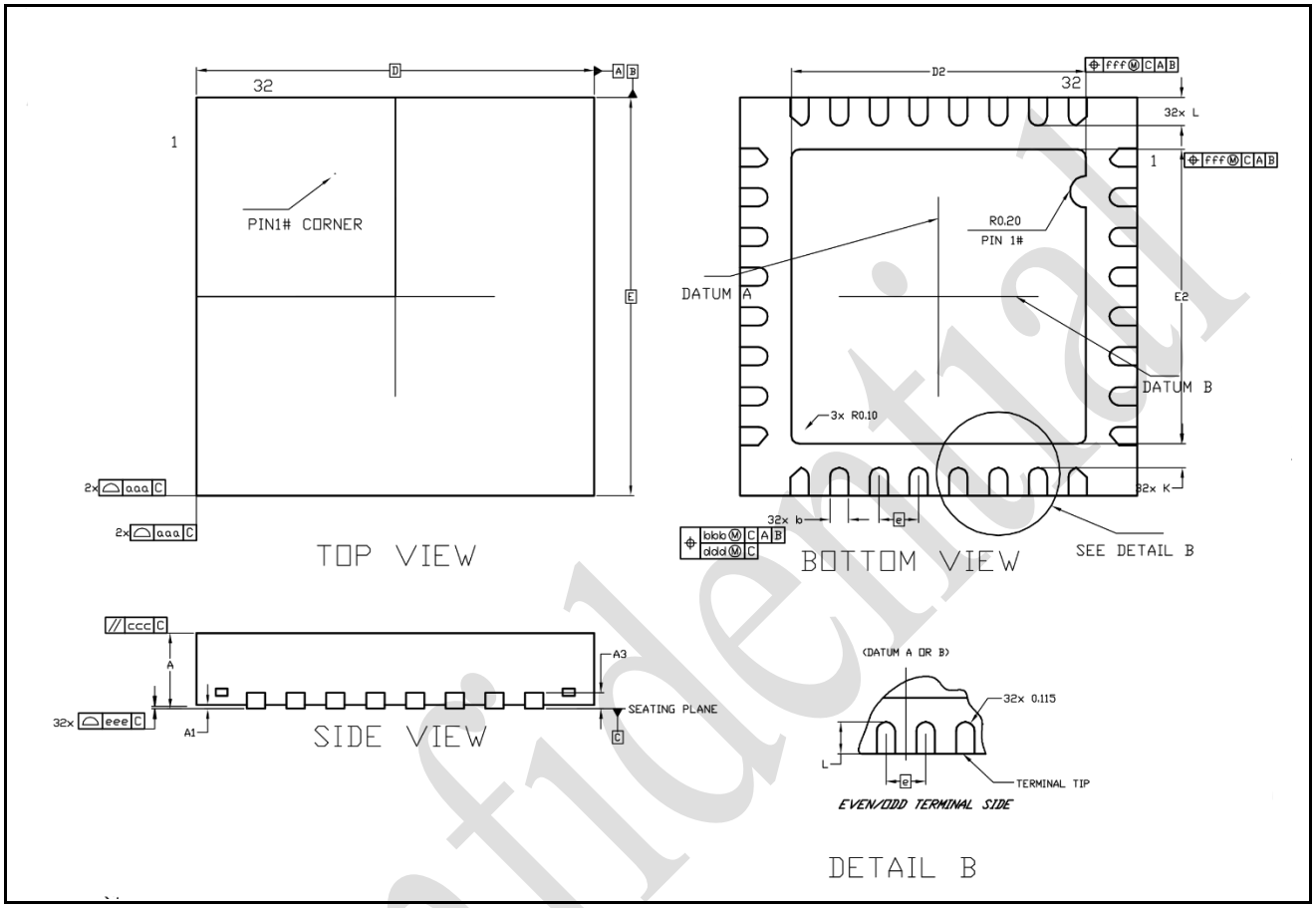

Figure 7-1 QFN32 Package Views

Table 7-1 Detailed Parameters of QFN32 Package

Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	0.70	0.75	0.80
	0.85	0.90	0.95
A1	0	0.02	0.05
A3	-	0.20 REF	-
b	0.18	0.23	0.28
D	5.00BSC		
E	5.00BSC		
D2	3.55	3.65	3.75
E2	3.55	3.65	3.75
e	0.50BSC		
L	0.30	0.35	0.40
K	0.20	-	-

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aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

7.2 QFN40 Package Dimensions

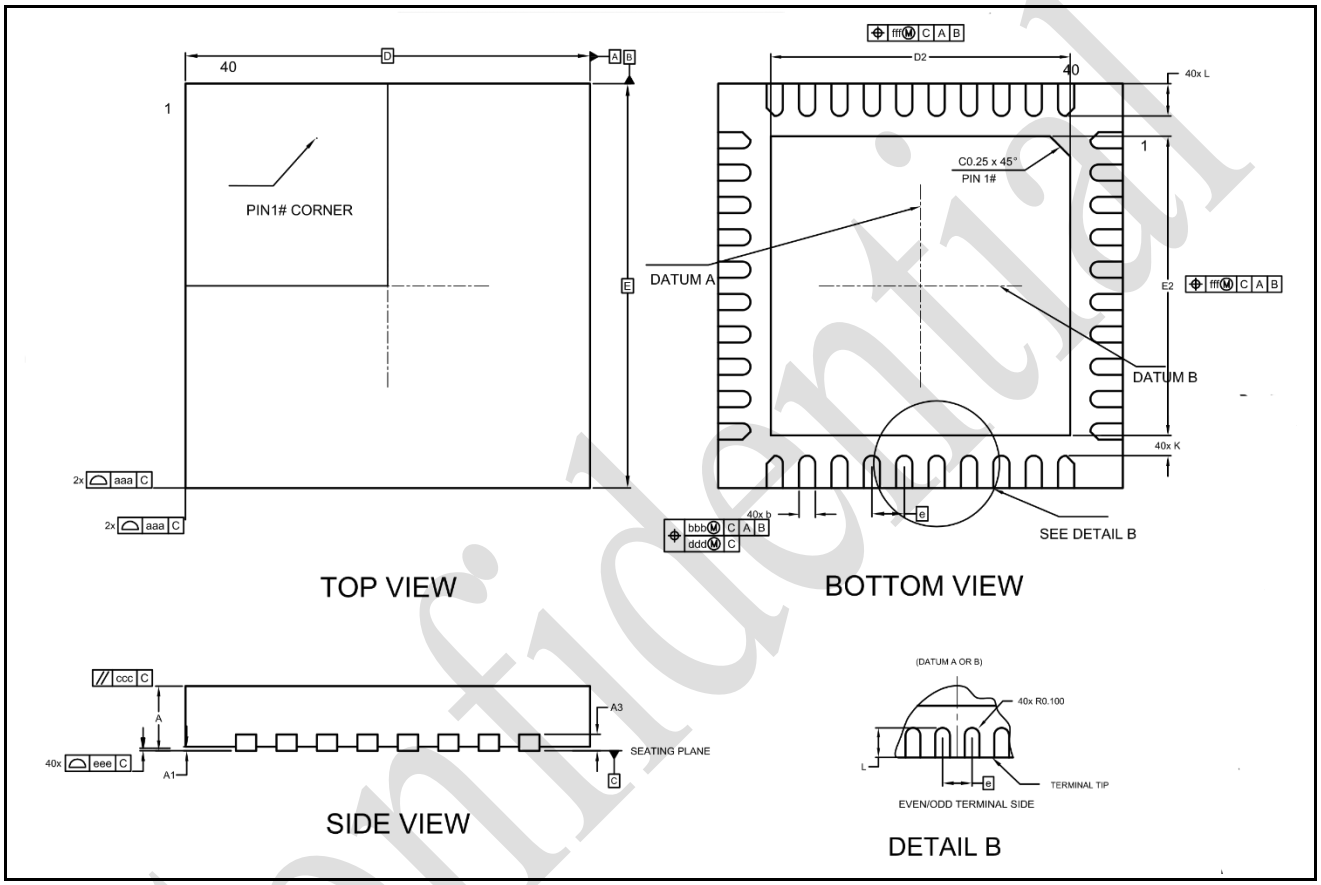

Figure 7-2 QFN40 Package Views

Table 7-2 Detailed Parameters of QFN40 Package

Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	0.70	0.75	0.80
	0.85	0.90	0.95
A1	0	0.02	0.05
A3	-	0.20REF	-
b	0.15	0.20	0.25
D	5.0BSC		
E	5.0BSC		
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.40BSC		

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L	0.35	0.40	0.45
K	0.20	-	-
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

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8 Precautions

1) This product is a CMOS device and should be protected against static electricity during storage, transportation and use.
2) Grounding when device is in use.
3) Reflow temperature can not exceed 260℃.

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9 Storage Conditions

1) Products should be stored in sealed packages: when the temperature is less than 30 degrees and the humidity is less than 90%, it can last for 12 months.
2) After the package is opened, the components will be used in the reflow process or other high-temperature processes. The following conditions must be met:
   a) Completed within 72 hours and the factory environment is less than 30℃≤ 60% RH.
   b) Stored in 10% RH environment.
   c) Exhaust at 125℃ for 24 hours to remove internal water vapor before used.

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