

absl::log_internal
::SyntheticBinary::Synthetic
Binary

absl::log_internal
::SyntheticBinary::
~SyntheticBinary

absl::log_internal
::SetVMModuleListHeadForTestOnly



```
graph LR; A["absl::log_internal::SyntheticBinary::Synthetic Binary"] --> C["absl::log_internal::SetVMModuleListHeadForTestOnly"]; B["absl::log_internal::SyntheticBinary::~~SyntheticBinary"] --> C;
```

The diagram illustrates a mapping or linking process. On the left, there are two white rectangular boxes. The top box contains the text 'absl::log_internal::SyntheticBinary::Synthetic Binary'. The bottom box contains 'absl::log_internal::SyntheticBinary::~~SyntheticBinary'. Blue arrows point from the right side of each of these boxes to a single gray rectangular box on the right. This gray box contains the text 'absl::log_internal::SetVMModuleListHeadForTestOnly'.