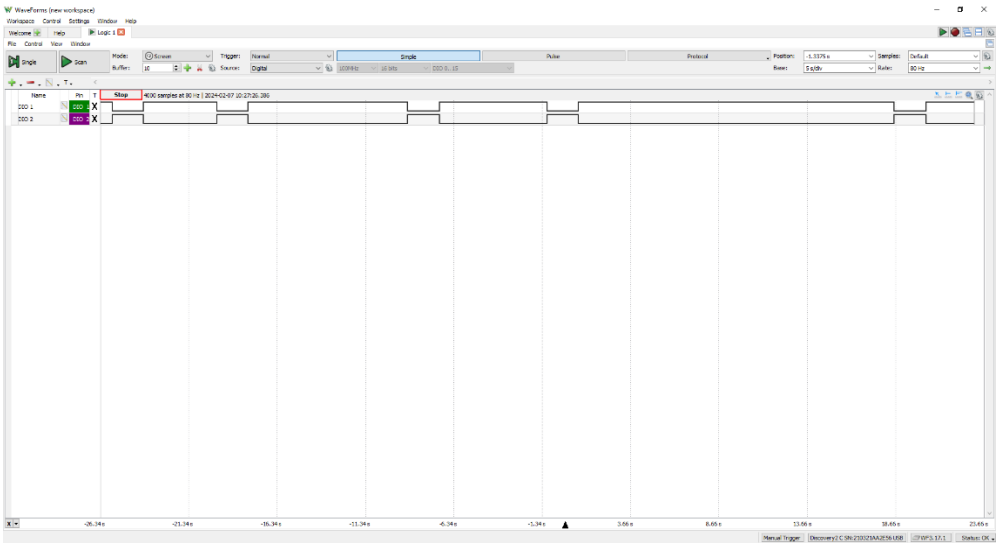
1. Why can't you use both pins PA0 and PC0 for external interrupts at the same time?
    - PA0 and PC0 are in the same group which is SYSCFG_EXTICR1, which is on a single multiplexer with the output routed to the EXTI0 input.
2. What software priority level gives the highest priority? What level gives the lowest?
    - 0 – 3 where 0 is the highest and 3 is the lowest.
3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?
    - 8 bits for each IPR, but only bits[7:6] are implemented.
4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.
    - 1.5 seconds.
    - 
5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?
    - It will cause the handler to loop since the interrupt request was never "acknowledged". Clearing the status flag will signify that the request was acknowledged.