Notes about the three types of pin-compatibility:

(1) STM32CubeMX listed as pin-compatible (with JTAG, USB, OSC, and OSC32 peripherals selected)

(2) STM32CubeMX listed as pin-compatible (with only SWD peripheral selected)

(3): Pinouts listed in the respective datasheets appeared to be pin-compatible (to me), with some notes

How to update this spreadsheet with the latest price and availability information:
(1) Download the latest JLCPCB SMT Parts Library spreadsheet from here: https://lipcbc.com/componentSearch/uploadComponentInfo
(2): Replace he tab in this spreadsheet called "JLCPCB SMT Parts Library" with the new spreadsheet. Ensure the title remains unchanged.

Sum: Part No	Manufactur	Din compatible (4)2	32	124		Dost state:	Dries @ Ot 1	Dries @ Ot. 12	Ctart	Ele-t-	DAM	1 10	Far -	Matri
Рап по	manutacturer	Fill compatible (1)?	Pin compatible (2)?	Fill compatible (3)?	OH JECPCB?	Part status	Price @ Uty: 1	Price @ Qty: 10	Stock	Flash	RAM	10	Freq.	Cortex-M23 instead of Cortex-M3
														Pin 1: "VBAT" on F103 becomes "VDD" (requires shorting resistor/solder blob on R2);
														Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO);
GD32E230C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 0.7985	\$ 0.6136	7159	64 kBytes	8 kBytes		72 MHz	No BOOT1; No USB; No JTAG; No SWO
														Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO);
GD32F130C6T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 0.8606	\$ 0.8606	1353	00 lvD: 4	4 kBytes		40 8411-	Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
GD32F130C616	GigaDevice	FALSE	FALSE	IRUE	IKUE	Extended	\$ 0.0000	\$ 0.0000	1353	32 KBytes	4 KBytes		46 WITIZ	Cortex-M23 instead of Cortex-M3
														Pin 1: "VBAT" on F103 becomes "OSC32-IN" (loss of VBAT functionality; loss of OSC32 functionality);
														Pin 2: "PC13" on F103 becomes "OSC32-OUT" (unusable as GPIO; loss of OSC32 functionality) Pin 3: "OSC32-IN" on F103 becomes "OSC-IN" (precludes use of 32 kHz oscillator input);
														Pin 4: "OSC32-0UT" on F103 becomes "OSC-0UT" (precludes use of 32 kHz oscillator input);
														Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO);
														Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIÓ); No BOOT1; No USB; No JTAG; No SWO
GD32E231C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 1.1485	\$ 0.8833	3 1294	64 kBytes	8 kBytes		72 MHz	Appears to have internal op-amps
														Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO);
GD32F130C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 0.8848	\$ 0.8848	3 15	64 kBytes	8 kBytes		48 MHz	Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
OD321 1300010	Olgabevice	TALOL	TALUL	INOL	TITOL	LXIGITGGG	9 0.0040	0.0040	, 13	04 KDytes	U KDytes		40 WII 12	Cortex-M4 instead of Cortex-M3
														Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO);
GD32F330C6T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 0.8997	s 0.8997	7 1492	32 kBytes	4 kBytes		84 MHz	Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
05021 0000010	Olgaboriac	TALGE	17100	mor	IIIOL	LAGIGOG	0.0007	0.000	1102	OE REYROO	- NDytoo		0 1 1111 12	Pin 1: "VBAT" on F103 becomes "PC0" on L010 (no degradation);
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L010 (loss of wake-up pin; no hardware changes required);
STM32L010C6T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$ 1.2455	\$ 0.9182	2 0	32 kBytes	8 kBytes	38	32 MHz	No BOOT1; No USB; No JTAG; No SWO Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G030C8T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 1.2606	\$ 0.9348	3 759	64 kBytes	8 kBytes	43	64 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
														Cortex-M4 instead of Cortex-M3 Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO);
														Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO);
GD32F330C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 0.9498	\$ 0.9498	3 546	64 kBytes	8 kBytes		84 MHz	No BOOT1; No USB; No JTAG; No SWO
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F031 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F031 (unusable as GPIO):
														Pin 36: "VDD" on F103 becomes "PF7" on F031 (unusable as GPIO);
STM32F031C6T6TR	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$ 1.2939	\$ 0.9727	7 153	32 kBytes	4 kBytes	39	48 MHz	
														Cortex-M4 instead of Cortex-M3 Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO);
														Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO);
GD32F330CBT6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 1.0182	\$ 1.0182	2 1212	128 kBytes	s 16 kBytes	;	84 MHz	No BOOT1; No USB; No JTAG; No SWO Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO);
														Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO);
														No BOOT1; No JTAG; No SWO
GD32F150C6T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 1.0255	\$ 1.0255	5 2007	32 kBytes	6 kBytes		72 MHz	Includes cap touch peripheral Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO);
														Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIÓ);
GD32F150C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 1.0439	\$ 1.0439	1468	64 kBytes	8 kBytes		70 MIL-	No BOOT1; No JTAG; No SWO Includes cap touch peripheral
GD32F130C610	GigaDevice	FALSE	FALSE	INUE	INUE	Exterided	9 1.0438	9 1.0438	1400	04 KBytes	o kbytes		72 WITH	Cortex-M4 instead of Cortex-M3
														Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO);
														Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No JTAG; No SWO
GD32F350C6T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 1.0448	\$ 1.0448	3 1497	32 kBytes	6 kBytes		108 MH	Includes cap touch peripheral
STM32G070CBT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 1.4152	\$ 1.0985	5 0	120 kButos	s 36 kBytes		64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
31W32G070CB10	31 MICOElectorics	FALSE	FALSE	FALSE	INUE	Exterided	9 1.4132	3 1.096	, ,	126 KBytes	S JU KDYIES	- 44	04 WITIZ	Cortex-M4 instead of Cortex-M3
														Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO);
														Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1: No JTAG: No SWO
GD32F350C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 1.1114				8 kBytes			z Includes cap touch peripheral
GD32E103CBT6	GigaDevice	FALSE FALSE	FALSE FALSE	TRUE TRUE	TRUE TRUE	Extended	\$ 1.4939				s 32 kBytes			z Cortex-M4 instead of Cortex-M3
GD32F101CBT6 GD32E103C8T6	GigaDevice GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended Extended	\$ 1.1742 \$ 1.2244			128 KBytes 64 kBytes	s 16 kBytes 20 kBytes	;		No USB Z Cortex-M4 instead of Cortex-M3
				-						7	. , ,			Cortex-M4 instead of Cortex-M3
Ì							1							Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO);
														No BOOT1; No JTAG; No SWO
GD32F350CBT6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$ 1.2338	\$ 1.2338	3 982	128 kBytes	s 16 kBytes	-	108 MH	Z Includes cap touch peripheral
STM32G031C6T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 1.7879	s 1.3015	5 0	32 kBytes	8 kBvtes	43	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
MOEGOO 100 10	Milor GOLGOLO III GO	TALOL	171202	171606		Lateracu	1.7078	1.3010	1	OL NO JIES	0 110 1100	1 43	J-7 1911 1Z	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F031 (loss of wake-up pin; no hardware changes required);
							1							Pin 35: "VSS on F103 becomes "PF6" on F031 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F031 (unusable as GPIO):
STM32F031C6T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$ 1.9258	\$ 1.4061	1 0	32 kBytes	4 kBytes	39	48 MHz	
														Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G031C8T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 1.9182	\$ 1.4076	3 0	64 kBytes	8 kBytes	43	64 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist). Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G071CBT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 2.1106	\$ 1.5606	6 0	128 kBytes	s 36 kBytes	44	64 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
				-	. —		. —			_				

														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F051 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F051 (unusable as GPIO); Pin 36: "VDIO on F103 becomes "PF6" on F051 (unusable as GPIO):
STM32F051C6T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	2.1621	1.604	5 0	32 kBytes	8 kBytes	39 48 MHz	No BOOT1; No USB; No JTAG; No SWO
														Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F302 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F302 (loss of wake-up pin; no hardware changes required);
STM32F302C8T6	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	\$	2.2242 \$	1.6076	1205	64 kBytes	16 kBytes	37 72 MHz	No BOOT1 Pin 1: "VBAT" on F103 becomes "VDD" on L052 (requires shorting resistor/solder blob on R2);
														Pin 10: "PAO-WKUP" on F103 becomes "VDD" on L032 (requires shorting resistor/societ blood on R2); Pin 10: "PAO-WKUP" on F103 becomes "PAO" on L052 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD" USB" on L052 (no degradation);
STM32L052C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	1.6506 \$	1.6506		64 kBytes	8 kBytes	37 32 MHz	No BOOT1; No JTAG; No SWO
STM32F103C6T6A	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	\$	1.6807 \$			32 kBytes		37 72 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G030C6T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$	1.7364 \$	1.6894	0	32 kBytes	8 kBytes	43 64 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist). Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F301 (unusable as VREF-);
STM32F301C8T6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	s	2.3121 \$	1.6909	0	64 kBytes	16 kBytes	37 72 MHz	
STM32F072CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	1.7271 \$	1.727	0	128 kBytes	16 kBytes	37 48 MHz	
														Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO);
GD32F190C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$	1.7795	1.779	1492	64 kBytes	8 kBytes	72 MHz	No BOOT1; No USB; No JTAG; No SWO Includes cap touch peripheral
STM32F101C8T6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	\$	1.7800 \$	1.7800) 2	64 kBytes		37 36 MHz	No USB
STM32F091CCT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	1.8136 \$	1.780	3 0	256 kBytes	32 kBytes	38 48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F091 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
														Pin 1: "VBAT" on F103 becomes "VDD" on F070 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F070 (loss of wake-up pin; no hardware changes required);
STM32F070CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	2.1364 \$	1.780	0	128 kBytes	16 kBytes	37 48 MHz	No BOOT1; No JTAG; No SWO Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F091 (loss of wake-up pin; no hardware changes required);
STM32F091CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	2.1076	1.801	5 0	128 kBytes	32 kBytes	38 48 MHz	No BOOT1; No USB; No JTAG; No SWO
														Pin 1: "VBAT" on F103 becomes "VDD" on L072 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L072 (loss of wake-up pin; no hardware changes required);
STM32L072CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	2.1318	1.822	0	128 kBytes	20 kBytes	37 32 MHz	Pin 36: "VDD" on F103 becomes "VDD_USB" on L072 (no degradation); No BOOT1; No JTAG; No SWO
STM32F071CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	s	2.5682	1.8576	3 0	128 kBytes	16 kBytes	37 48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F071 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
GD32F303CCT6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$	1.9250 \$	1.9250	0	256 kBytes	48 kBytes	120 MH;	z Cortex-M4 instead of Cortex-M3
STM32F100CBT6B	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	\$	2.6848 \$	1.9439	0	128 kBytes	8 kBytes	37 24 MHz	No USB Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F071 (loss of wake-up pin; no hardware changes required);
STM32F071C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	2.6621 \$	1.9500		64 kBytes	16 kBytes	37 48 MHz	No BOOT1; No USB; No JTAG; No SWO
STM32F101CBT6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	\$	2.3530 \$	2.0364	0	128 kBytes	16 kBytes	37 36 MHz	No USB Pin 1: "VBAT" on F103 becomes "VDD" on F030 (requires shorting resistor/solder blob on R2);
														Pint 10: "PAD-WKUP" on F103 becomes "PA0" on F030 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F030 (unusable as GPI0); Pin 36: "VD0" on F103 becomes "PF7" on F030 (unusable as GPI0);
STM32F030C8T6TR	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	2.0545 \$	2.0545	5 3	64 kBytes	8 kBytes	39 48 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L051 (requires shorting resistor/solder blob on R2);
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L051 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDDIO" on L051 (no degradation);
STM32L051C6T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	2.3955 \$	2.062	769	32 kBytes	8 kBytes	37 32 MHz	No BOOT1; No USB; No JTAG; No SWO
														Pin 10: "PA0-WKUP" on F103 becomes "PA0/CK_IN" on L412 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L412 (no degradation);
STM32L412C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	2.4348 \$	2.0924	0	64 kBytes	40 kBytes	38 80 MHz	No BOOT1 Pin 1: "VBAT" on F103 becomes "VDD" on L051 (requires shorting resistor/solder blob on R2);
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L051 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDDIO" on L051 (no degradation);
STM32L051C8T6 STM32F100C4T6B	ST Microelectonics ST Microelectonics	FALSE FALSE	FALSE TRUE	TRUE TRUE	TRUE	Extended Extended	S S	2.1591 \$	2.159		64 kBytes 16 kBytes		37 32 MHz 37 24 MHz	
											,			Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F303 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F303 (unusable as VREF+);
STM32F303C8T6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	_	2.9167	2.227		C4 I-D-4	16 kBytes	37 72 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F303 (loss of wake-up pin; no hardware changes required);
							\$				64 kBytes			Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function);
STM32L151C8T6A STM32F100C8T6B	ST Microelectonics ST Microelectonics	FALSE FALSE	FALSE TRUE	TRUE TRUE	TRUE	Extended Extended	\$	3.0045 \$ 2.2793 \$	2.2712		64 kBytes 64 kBytes	32 kBytes 8 kBytes	37 32 MHz 37 24 MHz	
														Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L431 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L431 (unusable as VREF+);
STM32L431CCT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	s	2.6303	2.280		256 bBs+0	64 kBytes	38 80 MH~	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L431 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
57M32E4310010	C. MICOGROCIO/IICS	TALUE	TALUL	INOL	IIIOL	LAIGHUGU		2.0000	2.200		200 KBytes	J- KDyles	30 00 WHZ	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L431 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L431 (unusable as VREF+);
STM32L431CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	s	2.3008 \$	2.3008	3 0	128 kBytes	64 kBytes	38 80 MHz	Pin 9: "VSS" on F103 becomes "VDI/VREF+" on L431 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L431 (loss of wake-up pin; no hardware changes required); No BOOT1: No USB
		111555				***************************************						,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		Pin 8: "VSS" on F103 becomes "VSS/VREF." on F303 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F303 (loss of wake-up pin; no hardware changes required);
STM32F303CCT6	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	\$	2.3798 \$	2.3798	0	256 kBytes	48 kBytes	37 72 MHz	
STM32F303CBT6	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	s	2.7879	2.4136		128 kButos	40 kBytes	37 72 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F303 (loss of wake-up pin; no hardware changes required);
5 7 M 521 3030 B 10	C. MICOGROCIO/IICS	INOL	INOL	INOL	IIIOL	LAIGHUGU		2.1010	2.4130	,	120 KBytes	- FO KDytes	37 72 WITZ	Pin 1: "VBAT" on F103 becomes "VDD" on F030 (requires shorting resistor/solder blob on R2);
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F030 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F030 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F030 (unusable as GPIO);
STM32F030C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Basic	\$	2.4223 \$	2.422	11476	64 kBytes	8 kBytes	39 48 MHz	No BOOT1; No USB; No JTAG; No SWO

														Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F334 (unusable as VREF-);
														Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F334 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F334 (loss of wake-up pin; no hardware changes required);
STM32F334C4T6 ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	s	3.4924	s	2.5970	0	16 kBytes	16 kBytes	37 72 MHz	No BOOT1; No USB
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F042 (loss of wake-up pin; no hardware changes required);
STM32F042C4T6 ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	S	2.8470	\$	2.7773	0	16 kBytes	6 kBytes	38 48 MHz	No BOOT1; No JTAG; No SWO Pin 1: "VBAT" on F103 becomes "VDD" on F030 (requires shorting resistor/solder blob on R2);
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F030 (loss of wake-up pin; no hardware changes required);
														Pin 35: "VSS on F103 becomes "PF6" on F030 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F030 (unusable as GPIO):
STM32F030C6T6 ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	s	2.9018	s	2.9018	3	32 kBytes	4 kBytes	39 48 MHz	No BOOT1; No USB; No JTAG; No SWO
					Exteriord									Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G071C8T6 ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$	3.0818	\$	2.9985	0	64 kBytes	36 kBytes	44 64 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
														Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F302 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F302 (loss of wake-up pin; no hardware changes required);
STM32F302CBT6 ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	\$	3.0021	\$	3.0021	685	128 kBytes	32 kBytes	37 72 MHz	No BOOT1
GD32F103CBT6 GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	\$	3.0545	\$	3.0545	0	128 kBytes	20 kBytes	108 MHz	Pin 35: "VSS on F103 becomes "PF6" on F031 (unusable as GPIO);
														Pin 36: "VDD" on F103 becomes "PF7" on F031 (unusable as GPIO);
STM32F031C4T6 ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	3.5212	\$	3.0591	0	16 kBytes	4 kBytes	39 48 MHz	
STM32G431CBT6 ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended		3.5742		3.0712	0	128 kBytes	32 kBytes	38 170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
31W32G431CB10 31 WILCOERCIONICS	FALSE	FALSE	FALSE	INUE	Exterided	•	3.3142	•	3.0712	0	120 KBytes	32 KByles	36 170 WH2	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F373 (unusable as VREF-);
														Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F373 (unusable as VREF+);
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F373 (loss of wake-up pin; no hardware changes required); Pin 17: "PA7" on F103 becomes "VDD" on F373 (possibly requires jumper wire);
														Pin 17: PAY on F103 becomes VDD on F373 (possibly requires jumper wire); Pin 23: "VSS" on F103 becomes "VSSSD/VREFSD-" on F373 (unusable as VREFSD-);
								1						Pin 24: "VDD" on F103 becomes "VDDSD" on F373 (VDDSD is tied to VDD);
														Pin 25: "PB12" on F103 becomes "VREFSD+" on F373 (no degradation); Pin 26: "PB13" on F103 becomes "PB14" on F373 (no degradation);
														Pin 27: "PB14" on F103 becomes "PB15" on F373 (no degradation);
														Pin 28: "PB15" on F103 becomes "PD8" on F373 (no degradation);
STM32F373C8T6 ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$	4.0424	\$	3.0864	0	64 kBytes	16 kBytes	37 72 MHz	No BOOT1 Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L433 (unusable as VREF-):
														Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L433 (unusable as VREF+);
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L433 (loss of wake-up pin; no hardware changes required);
STM32L433CBT6 ST Microelectonics	FAI SE	FALSE	TRUE	TRUE	Extended		3.7515		3.2076	0	128 kBytes	64 kBytes	38 80 MHz	Pin 36: "VDD" on F103 becomes "VDD_USB" on L433 (no degradation); No BOOT1
					Exterided	•				0				Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function):
STM32L151CBT6 ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	3.8591	\$	3.3333	0	128 kBytes	16 kBytes	37 32 MHz	No SWO
														Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F301 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F301 (loss of wake-up pin; no hardware changes required);
STM32F301C6T6 ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	s	3.9758	s	3.4288	0	32 kBytes	16 kBytes	37 72 MHz	No BOOT1; No USB
														Pin 1: "VBAT" on F103 becomes "VDD" on L071 (requires shorting resistor/solder blob on R2);
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L071 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDDIO" on L071 (no degradation):
STM32L071CBT6 ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	3.6227	\$	3.5288	0	128 kBytes	20 kBytes	37 32 MHz	No BOOT1; No USB; No JTAG; No SWO
														Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F334 (unusable as VREF-);
														Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F334 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F334 (loss of wake-up pin; no hardware changes required);
STM32F334C8T6 ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	\$	4.1000	\$	3.5727	1508	64 kBytes	16 kBytes	37 72 MHz	No BOOT1; No USB
														Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F334 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F334 (unusable as VREF+);
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F334 (loss of wake-up pin; no hardware changes required);
STM32F334C6T6 ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	\$	4.9424	\$	3.6758	1435	32 kBytes	16 kBytes	37 72 MHz	No BOOT1; No USB
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F051 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F051 (unusable as GPIO);
														Pin 35: VSS on F103 becomes "PF6" on F051 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F051 (unusable as GPIO):
STM32F051C8T6 ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	3.6852	\$	3.6852	0	64 kBytes	8 kBytes	39 48 MHz	No BOOT1; No USB; No JTAG; No SWO
STM32L152C8T6A ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended		3.8561		3.8561	0	64 kBytes	32 kBytes	37 32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
31W32E132C610A 31 WILCOBIECIONICS	FALSE	FALSE	INUE	INUE	Exterided	3	3.0301	•	3.0001	U	04 KBytes	32 KByles	37 32 WITZ	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L433 (unusable as VREF-);
														Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L433 (unusable as VREF+);
														Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L433 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD USB" on L433 (no degradation);
STM32L433CCT6 ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	4.6803	s	4.0227	3	256 kBytes	64 kBytes	38 80 MHz	No BOOT1
														Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function):
STM32L152CBT6A ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	4.2267	\$	4.2267	1248	128 kBytes	32 kBytes	37 32 MHz	No SWO
														Pin 10: "PA0-WKUP" on F103 becomes "PA0/CK_IN" on L412 (loss of wake-up pin; no hardware changes required);
						1		1.						Pin 36: "VDD" on F103 becomes "VDD_USB" on L412 (no degradation);
STM32L412CBT6 ST Microelectonics STM32F102CBT6 ST Microelectonics	FALSE TRUE	FALSE TRUE	TRUE TRUE	TRUE	Extended Extended	\$	4.5167 4.6758		4.3955 4.6758	0		40 kBytes 16 kBytes	38 80 MHz 37 48 MHz	
STWISE TOZOBTO STWICTORRECTORICS				INUE	Exteriued	3	4.0738	3		U	120 KByleS	10 KBytes		Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G431C6T6 ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$	5.0909	\$	4.9545	0	32 kBytes	32 kBytes	38 170 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
														Pin 1: "VBAT" on F103 becomes "VDD" on L072 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L072 (loss of wake-up pin; no hardware changes required);
														Pin 10: "PAU-WKUP" on F103 becomes "PAU" on L072 (loss of wake-up pin; no naroware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L072 (no degradation);
STM32L072CZT7 ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$	5.5348		5.3864	0	192 kBytes		37 32 MHz	No BOOT1; No JTAG; No SWO
STM32F103C8T6 ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Basic	\$	5.6138	\$	5.6138	32019	64 kBytes	20 kBytes	37 72 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G431C8T6 ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$	5.7258	\$	5.7258	0	64 kBytes	32 kBytes	38 170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32F103CBT6 ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Basic	\$	5.9794		5.9794	5240		20 kBytes	37 72 MHz	
STM32F042C6T6 ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended		6.0986		6.0986	0	32 kBytes	6 kBytes	38 48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F042 (loss of wake-up pin; no hardware changes required); No BOOT1: No JTAG: No SWO
3 I MIGCO HECTORICS	FALSE	FALSE	IRUE	IRUE	Exterided	3	0.0986	٥	0.0906	U	J3∠ KDytëS	o KDyteS	30 40 MHZ	IND BOOT I, NO STAO, NO ONTO

													Pin 1: "VBAT" on F103 becomes "VDD" on L071 (requires shorting resistor/solder blob on R2);
													Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L071 (loss of wake-up pin; no hardware changes required);
									_				Pin 36: "VDD" on F103 becomes "VDDIO" on L071 (no degradation);
STM32L071CZT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$ 7.1621 \$	6.1758	0	192 kBytes	20 kBytes	37 32 MHz	No BOOT1; No USB; No JTAG; No SWO Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F072 (loss of wake-up pin; no hardware changes required);
STM32F072C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	s 6.5780 S	6.5780	2	64 kBytes	16 kBytes	37 48 MHz	No BOOT1: No JTAG: No SWO
OTMOET OF EGGTO	O T WHO OCIOCIOTICO	TALGE	TALOL	mor	11102	LAtoridod	0.0700	0.0700		O-1 ND y LOO	TO KEYLOO	0. 10 1111 12	Pin 1: "VBAT" on F103 becomes "VDD" on F030 (requires shorting resistor/solder blob on R2);
													Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F030 (loss of wake-up pin; no hardware changes required);
STM32F030CCT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	\$ 6.8023 \$	6.8023	0	256 kBytes	32 kBytes	37 48 MHz	No BOOT1; No USB; No JTAG; No SWO
STM32G473CBT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 7.1879 \$	7.1879	0	128 kBytes	128 kBytes	20 470 1411-	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
S1M32G473CB16	S I Microelectorics	FALSE	FALSE	FALSE	IRUE	Extended	\$ 7.1079 \$	7.1079	U	120 KBytes	120 KBytes	36 170 MHZ	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G474CBT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 7.5000 \$	7.5000	0	128 kBytes	128 kBytes	38 170 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
													Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G473CCT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 8.1061 \$	8.1061	0	256 kBytes	128 kBytes	38 170 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
													Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F373 (unusable as VREF-);
													Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F373 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F373 (loss of wake-up pin; no hardware changes required);
													Pin 17: "PA7" on F103 becomes "VDD" on F373 (possibly requires jumper wire);
													Pin 23: "VSS" on F103 becomes "VSSSD/VREFSD-" on F373 (unusable as VREFSD-);
													Pin 24: "VDD" on F103 becomes "VDDSD" on F373 (VDDSD is tied to VDD);
													Pin 25: "PB12" on F103 becomes "VREFSD+" on F373 (no degradation);
													Pin 26: "PB13" on F103 becomes "PB14" on F373 (no degradation); Pin 27: "PB14" on F103 becomes "PB15" on F373 (no degradation);
													Pin 28: "PB15" on F103 becomes "PD8" on F373 (no degradation);
TM32F373CCT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 9.5348 \$	8.2924	0	256 kBytes	32 kBytes	37 72 MHz	No BOOT1
													Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
TM32G474CCT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 8.4182 \$	8.4182	0	256 kBytes	128 kBytes	38 170 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G473CET6	CT Migroolti	EALCE	EALOE	FALSE	TDUE	Euto-d-d	e 0.0000 °	9.6803	^	E40 I-D-4-	100 kD: 4	20 470 141	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
31W32G4/3GE16	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 9.6803 \$	9.0003	U	312 KDyleS	128 kBytes	36 170 MHZ	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist). Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G474CET6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 9.9939 \$	9.9939	0	512 kBytes	128 kBytes	38 170 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
									-				Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G484CET6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	\$ 10.3212 \$	10.3212	0	512 kBytes	128 kBytes	38 170 MHz	34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
													Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L452 (unusable as VREF-);
													Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L452 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L452 (loss of wake-up pin; no hardware changes required);
													Pin 36: "VDD" on F103 becomes "VDD_USB" on L452 (loss of wake-up pin; no naroware changes required);
TM32L452CET6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	160 kBytes	38 80 MHz	No BOOT1
										,	,		Pin 1: "VBAT" on F103 becomes "VLCD" on L053 (same hardware requirements, different function);
													Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L053 (loss of wake-up pin; no hardware changes required);
									_				Pin 36: "VDD" on F103 becomes "VDD_USB" on L053 (no degradation);
STM32L053C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	#VALUE!	#VALUE!	0	64 kBytes	8 kBytes	37 32 MHz	No BOOT1; No JTAG; No SWO
													Pin 20: "PB2" on F103 becomes "NPOR" on F038 (requires external device to manage power-on reset) Pin 35: "VSS on F103 becomes "PF6" on F038 (unusable as GPIO);
													Pin 36: "VDD" on F103 becomes "PF7" on F038 (unusable as GPIO);
STM32F038C6T6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	4 kBytes	38 48 MHz	No BOOT1; No USB; No JTAG; No SWO
													Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F051 (loss of wake-up pin; no hardware changes required);
													Pin 35: "VSS on F103 becomes "PF6" on F051 (unusable as GPIO);
STM32F051C4T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	40 lvD: 4	0.1.0.4	39 48 MHz	Pin 36: "VDD" on F103 becomes "PF7" on F051 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
S1M32F051C416	S1 Microelectonics	FALSE	FALSE	IRUE	FALSE	#N/A	#N/A	#N/A	#N/A	16 kBytes	8 KBytes	39 48 MHZ	Pin 1: "VBAT" on F103 becomes "VDD" on F070 (requires shorting resistor/solder blob on R2);
													Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F070 (loss of wake-up pin; no hardware changes required);
STM32F070C6T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	6 kBytes	37 48 MHz	No BOOT1; No JTAG; No SWO
													Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F078 (loss of wake-up pin; no hardware changes required);
													Pin 20: "PB2" on F103 becomes "NPOR" on F038 (requires external device to manage power-on reset);
TM32F078CBT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	16 kBytes	36 48 MHz	No BOOT1; No JTAG; No SWO Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F098 (loss of wake-up pin; no hardware changes required);
													Pin 20: "PB2" on F103 becomes "NPOR" on F038 (requires external device to manage power-on reset);
TM32F098CCT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	32 kBytes	37 48 MHz	No BOOT1; No USB; No JTAG; No SWO
TM32F100C6T6	ST Microelectonics	FALSE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	4 kBytes	37 24 MHz	No USB
	ST Microelectonics	FALSE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	16 kBytes		37 36 MHz	
TM32F101C6T6	ST Microelectonics	FALSE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes		37 36 MHz	No USB
TM32F102C4T6 TM32F102C6T6	ST Microelectonics ST Microelectonics	TRUE TRUE	TRUE TRUE	TRUE TRUE	FALSE	#N/A #N/A	#N/A #N/A	#N/A #N/A	#N/A #N/A		4 kBytes	37 48 MHz 37 48 MHz	
	ST Microelectonics ST Microelectonics	TRUE	TRUE	TRUE		#N/A #N/A	#N/A #N/A	#N/A #N/A	#N/A #N/A	32 kBytes			
TM32F102C8T6 TM32F103C4T6	ST Microelectonics	TRUE	TRUE	TRUE	FALSE	#N/A	#N/A #N/A	#N/A #N/A	#N/A	64 kBytes 16 kBytes	6 kBytes	37 48 MHz 37 72 MHz	
			0L		. ALOL	#139F3	11.51.3	27.87.5	11.3173	TO NOTICE	- 1107100	5, , 2 WII IZ	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F302 (unusable as VREF-);
										1			Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F302 (loss of wake-up pin; no hardware changes required);
STM32F302C6T6	ST Microelectonics	TRUE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	16 kBytes	37 72 MHz	No BOOT1
								1		1			Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F302 (unusable as VREF-);
TM32F302CCT6	ST Microelectonics	TRUE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	40 kByton	37 72 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F302 (loss of wake-up pin; no hardware changes required); No BOOT1
TW32F3U2CC16	S I Microelectorics	IRUE	IRUE	IRUE	FALSE	#IN/A	#IN/A	#IN/A	#N/A	200 KBytes	40 KBytes	37 72 NITIZ	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F303 (unusable as VREF-);
													Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F303 (unusable as VREF+);
						1				1	1	1	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F303 (loss of wake-up pin; no hardware changes required);
TM32F303C6T6	ST Microelectonics	FALSE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	16 kBytes	37 72 MHz	No BOOT1; No USB
											1 T		Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F318 (unusable as VREF-);
										1			Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F0318 (loss of wake-up pin; no hardware changes required);
	1	FALSE	TRUE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	16 kBytes	36 72 MHz	Pin 20: "PB2" on F103 becomes "NPOR" on F318 (requires external device to manage power-on reset); No BOOT1: No USB
CTM20E240COTC		FALSE	IKUE	FALSE	FALSE	#IN/A	#IN/A	#IN/A	#IN/A	04 KDyteS	10 KBytes	JD // WIHZ	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F328 (unusable as VREF-);
STM32F318C8T6	ST Microelectonics					1	1			1	1		,
STM32F318C8T6	ST Microelectonics							11			1		Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F328 (unusable as VREF+);
STM32F318C8T6	ST Microelectonics												Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F328 (loss of wake-up pin; no hardware changes required);
	ST Microelectonics ST Microelectonics	FAI SE	TRUE	FAI SE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes		36 72 MHz	Pin 9: "VSS" on F103 becomes "VDD/NREF+" on F328 (musable as VREF+); Pin 10: "PACWIKIP" on F103 becomes "PAO" on F328 (loss of wake-up pin; no hardware changes required); Pin 20: "PB2" on F103 becomes "NPOR" on F328 (requires external device to manage power-on reset); No BOOT1: No USB

											P P P	in 8: "VSS" on F103 becomes "VSS/VREF." on F358 (unusable as VREF-); in 9: "VSS" on F103 becomes "VDD/VREF+" on F358 (unusable as VREF+); in 0: "PSA-WKUP" on F103 becomes "PAO" on F358 (unusable as VREF+); in 10: "PAD-WKUP" on F103 becomes "PAO" on F358 (loss of wake-up pin; no hardware changes required); in 20: "PB2" on F103 becomes "NPOR" on F358 (requires external device to manage power-on reset);
STM32F358CCT6 ST Microelectonics	FALSE	TRUE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	48 kBytes		lo BOOT1; No USB in 8: "VSS" on F103 becomes "VSS/VREF-" on F373 (unusable as VREF-);
											P P P P P P	in 9: "\SS': on F103 becomes "\DD\NTEF+" on F373 (unusable as \NTEF+); in 10: "PAD\MVIP" on F103 becomes "\PAO" on F373 (loss of wake-up in; no hardware changes required); in 17: "\PAP" on F103 becomes "\DD" on F373 (possibly requires jumper wire); in 23: "\SS' on F103 becomes "\DDSD" on F373 (possibly requires jumper wire); in 24: "\DD" on F103 becomes "\DDSD" on F373 (\NDSD is ited to \VDD); in 24: "\DD" on F103 becomes "\NTEFSD+" on F373 (\NDSD is ited to \VDD); in 25: "\PB12" on F103 becomes "\PB14" on F373 (no degradation); in 26: "\PB13" on F103 becomes "\PB14" on F373 (no degradation); in 26: "\PB13" on F103 becomes "\PB14" on F373 (no degradation);
STM32F373CBT6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	24 kBytee	37 72 MHz N	in 28: "PB15" on F103 becomes "PD8" on F373 (no degradation); lo BOOT1
STM32F378CCT6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes		P P P P P P P P P P P P P P P P P P P	in 8: VSS' on F103 becomes VSS/VREF." on F378 (unusable as VREF-); in 9: VSS' on F103 becomes VDD/VREF+" on F378 (unusable as VREF-); in 10: "PAG-WKUP" on F103 becomes "PAD" on F378 (loss of wake-up pin: no hardware changes required); in 7: "PAT" on F103 becomes "PAD" on F378 (loss of wake-up pin: no hardware changes required); in 7: "PAT" on F103 becomes "VDD" on F378 (requires external device to manage power-on reset); in 12: "PB1" on F103 becomes "PE8" on F378 (no degradation); in 22: "PB1" on F103 becomes "PE8" on F378 (no degradation); in 23: "VSS" on F103 becomes "VDDSV en F378 (governed to the VDD); in 25: "PB12" on F103 becomes "VDDSV en F378 (governed to VDD); in 25: "PB12" on F103 becomes "VDDSV en F378 (governed to VDD); in 25: "PB12" on F103 becomes "PB15" on F378 (no degradation); in 27: "PB14" on F103 becomes "PB15" on F378 (no degradation); in 27: "PB14" on F103 becomes "PB15" on F378 (no degradation); in 32: "PB15" on F103 becomes "PB15" on F378 (no degradation); in 35: "YSS on F103 becomes "PF6" on F378 (unusable as GPIO); in 35: "YSS on F103 becomes "PF7" on F378 (unusable as GPIO); in 36: "YDS" on F103 becomes "PF7" on F378 (unusable as GPIO); in 8: "YSS" on F103 becomes "YSS/VREF-" on F410 (unusable as VREF-);
											P P P si	in 9: "\SS' on F103 becomes "\DD/\REF+" on F410 (unusable as \REF+); in 22: "BB10" on F103 becomes "\VCAP_1" on F410 (requires external capacitor); in 46: "PB9" on F103 becomes "\VCAP_1" on F410 (reposibly required jumper wire); in 47: "\VSS' on F103 becomes "\PDR_ON" on F410 (Power supply supervisor permanently turned off; requires external uppervisor);
STM32F410CBT6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	32 kBytes	35 100 MHz N	to USB lear as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G031C4T6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	16 kBytes	8 kBytes	43 64 MHz 3-	4/37, making them unsuitable for this breakout board (in addition to any other issues that might exist). lear as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G041C6T6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	8 kBytes	43 64 MHz 3-	4/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G041C8T6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	8 kBytes	43 64 MHz 3-	lear as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 4/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G071C6T6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	36 kBytes		lear as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 4/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G081CBT6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A		36 kBytes	N	lear as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 4/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G441CBT6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	32 kBytes	N	lear as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 4/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G471CCT6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	128 kBytes	N N	lear as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
											N	4/37, making them unsuitable for this breakout board (in addition to any other issues that might exist). lear as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G471CET6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	128 kBytes	N	4/37, making them unsuitable for this breakout board (in addition to any other issues that might exist). lear as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32G483CET6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	128 kBytes	38 170 MHz 3-	4/37, making them unsuitable for this breakout board (in addition to any other issues that might exist). lear as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins
STM32GBK1CBT6 ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	32 kBytes	42 170 MHz 3-	4/37, making them unsuitable for this breakout board (in addition to any other issues that might exist). in 1: "VBAT" on F103 becomes "PC0" on L031 (no degradation):
STM32L031C4T6 ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	16 kBytes	8 kBytes	38 32 MHz N	in 10: "PA0-WKUP" on F103 becomes "PA0" on L031 (loss of wake-up pin; no hardware changes required); lo BOOT1; No USB; No JTAG; No SWO
STM32L031C6T6 ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	8 kBytes	P P	in 1: "VBAT" on F103 becomes "PC0" on L031 (no degradation); in 10: "PA0-WKUP" on F103 becomes "PA0" on L031 (loss of wake-up pin; no hardware changes required); o BOOT1; No USB; No JTAG; No SWO
STM32L041C6T6 ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	8 kBytes	38 32 MHz N	in 1: "PABT" on F103 becomes "PC0" on L041 (no degradation); in 10: "PA0-WKUP" on F103 becomes "PA0" on L041 (loss of wake-up pin; no hardware changes required); o BOOT1; No USB; No JTAG; No SWO
STM32L052C6T6 ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	8 kBytes	9 P 9 P 37 32 MHz N	in 1: "VBAT" on F103 becomes "VDD" on L052 (requires shorting resistor/solder blob on R2); in 10: "PA0-WKUP" on F103 becomes "PA0" on L052 (loss of wake-up pin; no hardware changes required); in 36: "VDD" on F103 becomes "VDD_USB" on L052 (no degradation); lo BOOT1; No JTAG; No SWO
STM32L053C6T6 ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	8 kBytes	9 P 37 32 MHz N	in 1: "PAST" on F103 becomes "VLCO" on L053 (same hardware requirements, different function); in 10: "PAD-WMUP" on F103 becomes "PAO" on L053 (loss of wake-up ph; no hardware changes required); in 36: "VDD" on F103 becomes "VDD_USB" on L053 (no degradation); lo BOOT1: No JTAC; No SWO
STM32L063C8T6 ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	8 kBytes	P P P	in 1: "NAT" on F103 becomes "VLCD" on L083 (same hardware requirements, different function); in 10: "PAD-WKUP" on F103 becomes "PAD" on L083 (loss of wake-up pin; on hardware changes required); in 36: "VDD" on F103 becomes "VDD_USB" on L083 (no degradation); lo BOOT1: No JTAC; No SWO
											P P P	in 1: "VBAT" on F103 becomes "VDD" on L071 (requires shorting resistor/solder blob on R2); in 10: "PA0-WKUP" on F103 becomes "PA0" on L071 (loss of wake-up pin; no hardware changes required); in 36: "VDD" on F103 becomes "VDDIO" on L071 (no degradation);
STM32L071C8T6 ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	20 kBytes	37 32 MHz N	lo BOOT1; No USB; No JTAG; No SWO in 1: "VBAT" on F103 becomes "VLCD" on L073 (same hardware requirements, different function);
STM32L073CBT6 ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	20 kButo-	P P	in 10: "PAD-WKUP" on F103 becomes "PAD" on L073 (laser for wake-up pin; no hardware changes required); in 36: "VDD" on F103 becomes "VDD_USB" on L073 (no degradation); on S071: No TAG; No SWO
3 I MICTORIECTORICS	FALSE	FALSE	IKUE	FALSE	#IN/A	#IN/A	#IN/A	#N/A	1∠0 KDytes	ZU KDYIES	31 32 MITZ N	DOUTT, NO JINO 3000

												Pi Pi	n 1: "VBAT" on F103 becomes "VLCD" on L073 (same hardware requirements, different function); In 10: "PAO-WKLP" on I103 becomes "PAO" on L073 (loss of wake-up pir, no hardware changes required); In 36: "VDD" on F103 becomes "VDD_USB" on L073 (no degradation);
STM32L073CZT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	192 kBytes	20 kBytes		o BOOT1; No JTAG; No SWO in 1: "VBAT" on F103 becomes "VDD" on L081 (requires shorting resistor/solder blob on R2);
												Pi	in 10: "PA0-WKUP" on F103 becomes "PA0" on L081 (loss of wake-up pin; no hardware changes required); in 36: "VDD" on F103 becomes "VDDIO" on L081 (no degradation);
STM32L081CBT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	20 kBytes	37 32 MHz No	o BOOT1; No USB; No JTAG; No SWO
													in 1: "VBAT" on F103 becomes "VDD" on L081 (requires shorting resistor/solder blob on R2); in 10: "PA0-WKUP" on F103 becomes "PA0" on L081 (loss of wake-up pin; no hardware changes required);
STM32L081CZT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	192 kBytes	20 kButos	Pi	in 36: "VDD" on F103 becomes "VDDIO" on L081 (no degradation); o BOOT1; No USB; No JTAG; No SWO
31W32L081CZ10	31 Microelectorics	FALSE	PALSE	TRUE	FALSE	#IN/PS	#10//4	#19/A	#IN/A	192 KBytes	20 KBytes	Pi	in 1: "VBAT" on F103 becomes "VLCD" on L083 (same hardware requirements, different function);
												Pi Pi	in 10: "PA0-WKUP" on F103 becomes "PA0" on L083 (loss of wake-up pin; no hardware changes required); in 36: "VDD" on F103 becomes "VDD_USB" on L083 (no degradation);
STM32L083CBT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	20 kBytes	37 32 MHz No	o BOOT1; No JTAG; No SWO in 1: "VBAT" on F103 becomes "VLCD" on L083 (same hardware requirements, different function);
												Pi	in 10: "PA0-WKUP" on F103 becomes "PA0" on L083 (loss of wake-up pin; no hardware changes required); in 36: "VDD" on F103 becomes "VDD USB" on L083 (no degradation);
STM32L083CZT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	192 kBytes	20 kBytes	37 32 MHz No	o BOOT1; No JTAG; No SWO
STM32L151C6T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	10 kBytes		in 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); o SWO
STM32L151C6T6A	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	16 kBytes	Pi	in 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function);
												Pi	in 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function);
STM32L151C8T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	10 kBytes	Pi	in 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function);
STM32L151CBT6A	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	32 kBytes		o SWO in 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function);
STM32L151CCT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	32 kBytes	37 32 MHz No	o SWO
STM32L152C6T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	10 kBytes	37 32 MHz No	in 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); o SWO
STM32L152C6T6A	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	16 kBytes		in 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); o SWO
STM32L152C8T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	10 kBytes	Pi	in 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); o SWO
												Pi	in 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function);
STM32L152CBT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	16 kBytes	Pi	o SWO in 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function);
STM32L152CCT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	32 kBytes	37 32 MHz No	o SWO
												Pi	in 10: "PA0-WKUP" on F103 becomes "PA0/CK_IN" on L412 (loss of wake-up pin; no hardware changes required); in 36: "VDD" on F103 becomes "VDD_USB" on L412 (no degradation);
STM32L412CBT6P	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	40 kBytes	36 80 MHz No	
												Pi	in 10: "PA0-WKUP" on F103 becomes "PA0/CK_IN" on L412 (loss of wake-up pin; no hardware changes required);
STM32L422CBT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	40 kBytee	38 80 MHz No	in 36: "VDD" on F103 becomes "VDD_USB" on L412 (no degradation);
OTMOZE4ZZOBTO	OT WILL OBJECTORICS	TALUE	TALOL	INOL	TALOL	#IN/CS	#19/5	#19/5	TINES.	120 KDytes	40 KDytes	Pi	in 8: "VSS" on F103 becomes "VSS/VREF-" on L443 (unusable as VREF-);
												Pi	in 9: "VSS" on F103 becomes "VDD/VREF+" on L443 (unusable as VREF+); in 10: "PA0-WKUP" on F103 becomes "PA0" on L443 (loss of wake-up pin; no hardware changes required);
STM32L443CCT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	64 kBytes	38 80 MHz No	in 36: "VDD" on F103 becomes "VDD_USB" on L443 (no degradation); o BOOT1
											,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Pi	in 8: "VSS" on F103 becomes "VSS/VREF-" on L451 (unusable as VREF-); in 9: "VSS" on F103 becomes "VDD/VREF+" on L451 (unusable as VREF+);
												Pi	in 10: "PA0-WKUP" on F103 becomes "PA0" on L451 (loss of wake-up pin; no hardware changes required);
STM32L451CET6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	160 kBytes	38 80 MHz No	o BOOT1; No USB in 8: "VSS" on F103 becomes "VSS/VREF-" on L462 (unusable as VREF-);
												Pi	in 9: "VSS" on F103 becomes "VDD/VREF+" on L462 (unusable as VREF+); in 10: "PA0-WKUP" on F103 becomes "PA0" on L462 (loss of wake-up pin; no hardware changes required);
												Pi	in 36: "VDD" on F103 becomes "VDD_USB" on L462 (no degradation);
STM32L462CET6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	160 kBytes		o BOOT1 in 8: "VSS" on F103 becomes "VSS/VREF-" on L4P5 (unusable as VREF-);
													in 9: "VSS" on F103 becomes "VDD/VREF+" on L4P5 (unusable as VREF+); in 10: "PA0-WKUP" on F103 becomes "PA0" on L4P5 (loss of wake-up pin; no hardware changes required);
												Pi	in 36: "VDD" on F103 becomes "VDD_USB" on L4P5 (no degradation);
STM32L4P5CET6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	320 kBytes	Pi	o BOOT1; Only OTG-FS ("on-the-go, full speed") USB in 8: "VSS" on F103 becomes "VSS/VREF-" on L4P5 (unusable as VREF-);
												Pi Pi	in 9: "VSS" on F103 becomes "VDD/VREF+" on L4P5 (unusable as VREF+); in 10: "PA0-WKUP" on F103 becomes "PA0" on L4P5 (loss of wake-up pin; no hardware changes required);
STM32L4P5CGT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	1024 kBytes	220 kButoo	Pi	in 36: "VDD" on F103 becomes "VDD_USB" on L4P5 (no degradation); o BOOT1; Only OTG-FS ("on-the-go, full speed") USB
STWSZL4PSUGT6	o i microelectonics	FALSE	FALSE	INUE	FALSE	#IN/A	#IN/A	#IN/A	#N/A	1024 KDyleS	JZU KDYIES	Pi	in 8: "VSS" on F103 becomes "VSS/VREF-" on L4P5 (unusable as VREF-);
												Pi	in 9: "VSS" on F103 becomes "VDD/VREF+" on L4P5 (unusable as VREF+); in 10: "PA0-WKUP" on F103 becomes "PA0" on L4P5 (loss of wake-up pin; no hardware changes required);
												Pi	in 22: "PB11" on F103 becomes "VDD12" on L4P5 (no degradation); in 46: "PB9" on F103 becomes "VDD12" on L4P5 (no degradation);
OTHER 40505		541.05	541.05	TRUE	541.05		//h.//a	*****		400410	00015	Pi	in 36: "VDD" on F103 becomes "VDD_USB" on L4P5 (no degradation);
STM32L4P5CGT6P	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	1024 kBytes	320 kBytes	Pi	o BOOT1; Only OTG-FS ("on-the-go, full speed") USB in 8: "VSS" on F103 becomes "VSS/VREF-" on L4Q5 (unusable as VREF-);
												Pi Pi	in 9: "VSS" on F103 becomes "VDD/VREF+" on L4Q5 (unusable as VREF+); in 10: "PA0-WKUP" on F103 becomes "PA0" on L4Q5 (loss of wake-up pin; no hardware changes required);
CTM201 40500T0	OT Minro-1t	FAI SE	EALOE	TPUE	FALSE	46174	#81/A	44517A	ANTA.	1024 1-0-4	220 60-4-	Pi	in 36: "VDD" on F103 becomes "VDD_USB" on L4Q5 (no degradation);
STM32L4Q5CGT6	o i Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	1024 kBytes	320 KBytes	38 120 MHz No	o BOOT1; Only OTG-FS ("on-the-go, full speed") USB

			1			1								n 8: "VSS" on F103 becomes "VSS/VREF-" on L4Q5 (unusable as VREF-);
						1 '								n 9: "VSS" on F103 becomes "VDD/VREF+" on L4Q5 (unusable as VREF+);
					1	. '					1	1		n 10: "PA0-WKUP" on F103 becomes "PA0" on L4Q5 (loss of wake-up pin; no hardware changes required);
					1	. '					1	1		n 36: "VDD" on F103 becomes "VDD_USB" on L4Q5 (no degradation);
M32L4Q5CGT6P	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	1024 kBytes	320 kBytes	36 1		BOOT1; Only OTG-FS ("on-the-go, full speed") USB
					1	. '					1	1		n 8: "VSS" on F103 becomes "VSS/VREF-" on L552 (unusable as VREF-);
					1	. '					1	1		n 9: "VSS" on F103 becomes "VDD/VREF+" on L552 (unusable as VREF+);
					1	1 '						1		n 10: "PA0-WKUP" on F103 becomes "PA0" on L552 (loss of wake-up pin; no hardware changes required);
M32L552CCT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	256 kBytes	38 1	110 MHz No E	
						,								n 8: "VSS" on F103 becomes "VSS/VREF-" on L552 (unusable as VREF-);
					1	. '					1	1	Pin ^r	n 9: "VSS" on F103 becomes "VDD/VREF+" on L552 (unusable as VREF+);
					1	. '					1	1		n 10: "PA0-WKUP" on F103 becomes "PA0" on L552 (loss of wake-up pin; no hardware changes required);
TM32L552CET6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	256 kBytes	38 1	110 MHz No E	BOOT1
			1		1	1								n 8: "VSS" on F103 becomes "VSS/VREF-" on L552 (unusable as VREF-);
					1	. '					1	1	Pin ^r	n 9: "VSS" on F103 becomes "VDD/VREF+" on L552 (unusable as VREF+);
					1	. '					1	1	Pin	n 10: "PA0-WKUP" on F103 becomes "PA0" on L552 (loss of wake-up pin; no hardware changes required);
					1	. '					1	1	Pin	n 22: "PB11" on F103 becomes "VDD12 1" on L562 (no degradation);
					1	. '					1	1		n 46: "PB9" on F103 becomes "VDD12 2" on L462 (no degradation);
TM32L552CET6P	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	256 kBytes	36 1	110 MHz No E	BOOT1
					1	1							Pin	n 8: "VSS" on F103 becomes "VSS/VREF-" on L562 (unusable as VREF-);
					1	. '					1	1		n 9: "VSS" on F103 becomes "VDD/VREF+" on L562 (unusable as VREF+);
					1	. '					1	1	Pin	n 10: "PA0-WKUP" on F103 becomes "PA0" on L562 (loss of wake-up pin: no hardware changes required):
TM32L562CET6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	256 kBytes	38 1	110 MHz No E	
													Pin	n 8: "VSS" on F103 becomes "VSS/VREF-" on L562 (unusable as VREF-);
					1	. '					1	1		n 9: "VSS" on F103 becomes "VDD/VREF+" on L562 (unusable as VREF+);
					1	. '					1	1		n 10: "PA0-WKUP" on F103 becomes "PA0" on L562 (loss of wake-up pin; no hardware changes required):
					1	. '					1	1		n 22: "PB11" on F103 becomes "VDD12 1" on L562 (no degradation);
					1	. '					1	1		n 46: "PB9" on F103 becomes "VDD12 2" on L462 (no degradation);
TM201 FEOCETED	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/Δ	#N/A	#N/A	512 kBytes	256 kBytes	36 1	110 MHz No E	