Notes about the three types of pin-compatibility:	How to update this spreadsheet with the latest price and availability information:
(1): STM32CubeMX listed as pin-compatible (with JTAG, USB, OSC, and OSC32 peripherals selected)	(1): Download the latest JLCPCB SMT Parts Library spreadsheet from here: https://jlcpcb.com/componentSearch/uploadComponentInfo
(2): STM32CubeMX listed as pin-compatible (with only SWD peripheral selected)	(2): Replace the tab in this spreadsheet called "JLCPCB SMT Parts Library" with the new spreadsheet. Ensure the title remains unchanged.
(3): Pinouts listed in the respective datasheets appeared to be pin-compatible (to me), with some notes	

Sum:		14	32	124	74									
Part No	**Manufacturer**	**Pin compatible (1)?**	**Pin compatible (2)?**	**Pin compatible (3)?**	**On JLCPCB?**	**Part status**	**Price @ Qty: 1**	**Price @ Qty: 10**	**Stock**	**Flash**	**RAM**	**IO**	**Freq.**	**Notes**
GD32E230C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 0.7985	$ 0.6136	7159	64 kBytes	8 kBytes		72 MHz	Cortex-M23 instead of Cortex-M3 Pin 1: "VBAT" on F103 becomes "VDD" (requires shorting resistor/solder blob on R2); Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
GD32F130C6T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 0.8606	$ 0.8606	1353	32 kBytes	4 kBytes		48 MHz	Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
GD32E231C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.1485	$ 0.8833	1294	64 kBytes	8 kBytes		72 MHz	Cortex-M23 instead of Cortex-M3 Pin 1: "VBAT" on F103 becomes "OSC32-IN" (loss of VBAT functionality; loss of OSC32 functionality); Pin 2: "PC13" on F103 becomes "OSC32-OUT" (unusable as GPIO; loss of OSC32 functionality) Pin 3: "OSC32-IN" on F103 becomes "OSC-IN" (precludes use of 32 kHz oscillator input); Pin 4: "OSC32-OUT" on F103 becomes "OSC-OUT" (precludes use of 32 kHz oscillator input); Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO Appears to have internal op-amps
GD32F130C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 0.8848	$ 0.8848	15	64 kBytes	8 kBytes		48 MHz	Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
GD32F330C6T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 0.8997	$ 0.8997	1492	32 kBytes	4 kBytes		84 MHz	Cortex-M4 instead of Cortex-M3 Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
STM32L010C6T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.2455	$ 0.9182	0	32 kBytes	8 kBytes	38	32 MHz	Pin 1: "VBAT" on F103 becomes "PC0" on L010 (no degradation); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L010 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
STM32G030C8T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 1.2606	$ 0.9348	759	64 kBytes	8 kBytes	43	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
GD32F330C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 0.9498	$ 0.9498	546	64 kBytes	8 kBytes		84 MHz	Cortex-M4 instead of Cortex-M3 Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
STM32F031C6T6TR	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.2939	$ 0.9727	153	32 kBytes	4 kBytes	39	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F031 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F031 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F031 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
GD32F330CBT6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.0182	$ 1.0182	1212	128 kBytes	16 kBytes		84 MHz	Cortex-M4 instead of Cortex-M3 Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
GD32F150C6T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.0255	$ 1.0255	2007	32 kBytes	6 kBytes		72 MHz	Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No JTAG; No SWO Includes cap touch peripheral
GD32F150C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.0439	$ 1.0439	1468	64 kBytes	8 kBytes		72 MHz	Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No JTAG; No SWO Includes cap touch peripheral
GD32F350C6T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.0448	$ 1.0448	1497	32 kBytes	6 kBytes		108 MHz	Cortex-M4 instead of Cortex-M3 Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No JTAG; No SWO Includes cap touch peripheral
STM32G070CBT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 1.4152	$ 1.0985	0	128 kBytes	36 kBytes	44	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
GD32F350C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.1114	$ 1.1114	1358	64 kBytes	8 kBytes		108 MHz	Cortex-M4 instead of Cortex-M3 Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No JTAG; No SWO Includes cap touch peripheral
GD32E103CBT6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.4939	$ 1.1485	0	128 kBytes	32 kBytes		108 MHz	Cortex-M4 instead of Cortex-M3
GD32F101CBT6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.1742	$ 1.1742	1267	128 kBytes	16 kBytes		56 Mhz	No USB
GD32E103C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.2244	$ 1.2244	0	64 kBytes	20 kBytes		120 MHz	Cortex-M4 instead of Cortex-M3
GD32F350CBT6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.2338	$ 1.2338	982	128 kBytes	16 kBytes		108 MHz	Cortex-M4 instead of Cortex-M3 Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No JTAG; No SWO Includes cap touch peripheral
STM32G031C6T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 1.7879	$ 1.3015	0	32 kBytes	8 kBytes	43	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32F031C6T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.9258	$ 1.4061	0	32 kBytes	4 kBytes	39	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F031 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F031 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F031 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
STM32G031C8T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 1.9182	$ 1.4076	0	64 kBytes	8 kBytes	43	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G071CBT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 2.1106	$ 1.5606	0	128 kBytes	36 kBytes	44	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).

STM32F051C6T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.1621	$ 1.6045	0	32 kBytes	8 kBytes	39	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F051 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F051 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F051 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
STM32F302C8T6	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	$ 2.2242	$ 1.6076	1205	64 kBytes	16 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F302 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F302 (loss of wake-up pin; no hardware changes required); No BOOT1
STM32L052C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.6506	$ 1.6506	551	64 kBytes	8 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L052 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L052 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L052 (no degradation); No BOOT1; No JTAG; No SWO
STM32F103C6T6A	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	$ 1.6807	$ 1.6807	1	32 kBytes	10 kBytes	37	72 MHz	
STM32G030C6T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 1.7364	$ 1.6894	0	32 kBytes	8 kBytes	43	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32F301C8T6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 2.3121	$ 1.6909	0	64 kBytes	16 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F301 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F301 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
STM32F072CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.7271	$ 1.7271	0	128 kBytes	16 kBytes	37	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F072 (loss of wake-up pin; no hardware changes required); No BOOT1; No JTAG; No SWO
GD32F190C8T6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.7795	$ 1.7795	1492	64 kBytes	8 kBytes		72 MHz	Pin 35: "VSS on F103 becomes "PF6" (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO Includes cap touch peripheral
STM32F101C8T6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 1.7800	$ 1.7800	2	64 kBytes	10 kBytes	37	36 MHz	No USB
STM32F091CCT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.8136	$ 1.7803	0	256 kBytes	32 kBytes	38	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F091 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
STM32F070CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.1364	$ 1.7803	0	128 kBytes	16 kBytes	37	48 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on F070 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F070 (loss of wake-up pin; no hardware changes required); No BOOT1; No JTAG; No SWO
STM32F091CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.1076	$ 1.8015	0	128 kBytes	32 kBytes	38	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F091 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
STM32L072CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.1318	$ 1.8227	0	128 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L072 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L072 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L072 (no degradation); No BOOT1; No JTAG; No SWO
STM32F071CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.5682	$ 1.8576	0	128 kBytes	16 kBytes	37	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F071 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
GD32F303CCT6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 1.9250	$ 1.9250	0	256 kBytes	48 kBytes		120 MHz	Cortex-M4 instead of Cortex-M3
STM32F100CBT6B	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 2.6848	$ 1.9439	0	128 kBytes	8 kBytes	37	24 MHz	No USB
STM32F071C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.6621	$ 1.9500	0	64 kBytes	16 kBytes	37	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F071 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
STM32F101CBT6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 2.3530	$ 2.0364	0	128 kBytes	16 kBytes	37	36 MHz	No USB
STM32F030C8T6TR	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.0545	$ 2.0545	3	64 kBytes	8 kBytes	39	48 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on F030 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F030 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F030 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F030 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
STM32L051C6T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.3955	$ 2.0621	769	32 kBytes	8 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L051 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L051 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDDIO" on L051 (no degradation); No BOOT1; No USB; No JTAG; No SWO
STM32L412C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.4348	$ 2.0924	0	64 kBytes	40 kBytes	38	80 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0/CK_IN" on L412 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L412 (no degradation); No BOOT1
STM32L051C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.1591	$ 2.1591	0	64 kBytes	8 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L051 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L051 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDDIO" on L051 (no degradation); No BOOT1; No USB; No JTAG; No SWO
STM32F100C4T6B	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 2.5258	$ 2.1621	0	16 kBytes	4 kBytes	37	24 MHz	No USB
STM32F303C8T6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 2.9167	$ 2.2273	0	64 kBytes	16 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F303 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F303 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F303 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
STM32L151C8T6A	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 3.0045	$ 2.2712	2	64 kBytes	32 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32F100C8T6B	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 2.2793	$ 2.2793	0	64 kBytes	8 kBytes	37	24 MHz	No USB
STM32L431CCT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.6303	$ 2.2803	0	256 kBytes	64 kBytes	38	80 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L431 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L431 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L431 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
STM32L431CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.3008	$ 2.3008	0	128 kBytes	64 kBytes	38	80 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L431 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L431 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L431 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
STM32F303CCT6	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	$ 2.3798	$ 2.3798	0	256 kBytes	48 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F303 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F303 (loss of wake-up pin; no hardware changes required); No BOOT1
STM32F303CBT6	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	$ 2.7879	$ 2.4136	0	128 kBytes	40 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F303 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F303 (loss of wake-up pin; no hardware changes required); No BOOT1
STM32F030C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Basic	$ 2.4223	$ 2.4223	11476	64 kBytes	8 kBytes	39	48 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on F030 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F030 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F030 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F030 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO

STM32F334C4T6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 3.4924	$ 2.5970	0	16 kBytes	16 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F334 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F334 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F334 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
STM32F042C4T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.8470	$ 2.7773	0	16 kBytes	6 kBytes	38	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F042 (loss of wake-up pin; no hardware changes required); No BOOT1; No JTAG; No SWO
STM32F030C6T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 2.9018	$ 2.9018	3	32 kBytes	4 kBytes	39	48 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on F030 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F030 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F030 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F030 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
STM32G071C8T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 3.0818	$ 2.9985	0	64 kBytes	36 kBytes	44	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32F302CBT6	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	$ 3.0021	$ 3.0021	685	128 kBytes	32 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F302 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F302 (loss of wake-up pin; no hardware changes required); No BOOT1
GD32F103CBT6	GigaDevice	FALSE	FALSE	TRUE	TRUE	Extended	$ 3.0545	$ 3.0545	0	128 kBytes	20 kBytes		108 MHz	
STM32F031C4T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 3.5212	$ 3.0591	0	16 kBytes	4 kBytes	39	48 MHz	Pin 35: "VSS on F103 becomes "PF6" on F031 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F031 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
STM32G431CBT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 3.5742	$ 3.0712	0	128 kBytes	32 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32F373C8T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 4.0424	$ 3.0864	0	64 kBytes	16 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F373 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F373 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F373 (loss of wake-up pin; no hardware changes required); Pin 17: "PA7" on F103 becomes "VDD" on F373 (possibly requires jumper wire); Pin 23: "VSS" on F103 becomes "VSSSD/VREFSD-" on F373 (unusable as VREFSD-); Pin 24: "VDD" on F103 becomes "VDDSD" on F373 (VDDSD is tied to VDD); Pin 25: "PB12" on F103 becomes "VREFSD+" on F373 (no degradation); Pin 26: "PB13" on F103 becomes "PB14" on F373 (no degradation); Pin 27: "PB14" on F103 becomes "PB15" on F373 (no degradation); Pin 28: "PB15" on F103 becomes "PD8" on F373 (no degradation); No BOOT1
STM32L433CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 3.7515	$ 3.2076	0	128 kBytes	64 kBytes	38	80 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L433 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L433 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L433 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L433 (no degradation); No BOOT1
STM32L151CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 3.8591	$ 3.3333	0	128 kBytes	16 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32F301C6T6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 3.9758	$ 3.4288	0	32 kBytes	16 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F301 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F301 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
STM32L071CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 3.6227	$ 3.5288	0	128 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L071 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L071 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDDIO" on L071 (no degradation); No BOOT1; No USB; No JTAG; No SWO
STM32F334C8T6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 4.1000	$ 3.5727	1508	64 kBytes	16 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F334 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F334 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F334 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
STM32F334C6T6	ST Microelectonics	FALSE	TRUE	TRUE	TRUE	Extended	$ 4.9424	$ 3.6758	1435	32 kBytes	16 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F334 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F334 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F334 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
STM32F051C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 3.6852	$ 3.6852	0	64 kBytes	8 kBytes	39	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F051 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F051 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F051 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
STM32L152C8T6A	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 3.8561	$ 3.8561	0	64 kBytes	32 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L433CCT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 4.6803	$ 4.0227	3	256 kBytes	64 kBytes	38	80 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L433 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L433 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L433 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L433 (no degradation); No BOOT1
STM32L152CBT6A	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 4.2267	$ 4.2267	1248	128 kBytes	32 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L412CBT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 4.5167	$ 4.3955	0	128 kBytes	40 kBytes	38	80 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0/CK_IN" on L412 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L412 (no degradation); No BOOT1
STM32F102CBT6	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Extended	$ 4.6758	$ 4.6758	0	128 kBytes	16 kBytes	37	48 MHz	
STM32G431C6T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 5.0909	$ 4.9545	0	32 kBytes	32 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32L072CZT7	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 5.5348	$ 5.3864	0	192 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L072 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L072 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L072 (no degradation); No BOOT1; No JTAG; No SWO
STM32F103C8T6	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Basic	$ 5.6138	$ 5.6138	32019	64 kBytes	20 kBytes	37	72 MHz	
STM32G431C8T6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 5.7258	$ 5.7258	0	64 kBytes	32 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32F103CBT6	ST Microelectonics	TRUE	TRUE	TRUE	TRUE	Basic	$ 5.9794	$ 5.9794	5240	128 kBytes	20 kBytes	37	72 MHz	
STM32F042C6T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 6.0986	$ 6.0986	0	32 kBytes	6 kBytes	38	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F042 (loss of wake-up pin; no hardware changes required); No BOOT1; No JTAG; No SWO

STM32L071CZT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 7.1621	$ 6.1758	0	192 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L071 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L071 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDDIO" on L071 (no degradation); No BOOT1; No USB; No JTAG; No SWO
STM32F072C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 6.5780	$ 6.5780	2	64 kBytes	16 kBytes	37	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F072 (loss of wake-up pin; no hardware changes required); No BOOT1; No JTAG; No SWO
STM32F030CCT6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	$ 6.8023	$ 6.8023	0	256 kBytes	32 kBytes	37	48 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on F030 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F030 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
STM32G473CBT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 7.1879	$ 7.1879	0	128 kBytes	128 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G474CBT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 7.5000	$ 7.5000	0	128 kBytes	128 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G473CCT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 8.1061	$ 8.1061	0	256 kBytes	128 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32F373CCT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 9.5348	$ 8.2924	0	256 kBytes	32 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F373 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F373 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F373 (loss of wake-up pin; no hardware changes required); Pin 17: "PA7" on F103 becomes "VDD" on F373 (possibly requires jumper wire); Pin 23: "VSS" on F103 becomes "VSSSD/VREFSD-" on F373 (unusable as VREFSD-); Pin 24: "VDD" on F103 becomes "VDDSD" on F373 (VDDSD is tied to VDD); Pin 25: "PB12" on F103 becomes "VREFSD+" on F373 (no degradation); Pin 26: "PB13" on F103 becomes "PB14" on F373 (no degradation); Pin 27: "PB14" on F103 becomes "PB15" on F373 (no degradation); Pin 28: "PB15" on F103 becomes "PD8" on F373 (no degradation); No BOOT1
STM32G474CCT6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 8.4182	$ 8.4182	0	256 kBytes	128 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G473CET6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 9.6803	$ 9.6803	0	512 kBytes	128 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G474CET6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 9.9939	$ 9.9939	0	512 kBytes	128 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G484CET6	ST Microelectonics	FALSE	FALSE	FALSE	TRUE	Extended	$ 10.3212	$ 10.3212	0	512 kBytes	128 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32L452CET6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	160 kBytes	38	80 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L452 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L452 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L452 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L452 (no degradation); No BOOT1
STM32L053C8T6	ST Microelectonics	FALSE	FALSE	TRUE	TRUE	Extended	#VALUE!	#VALUE!	0	64 kBytes	8 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L053 (same hardware requirements, different function); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L053 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L053 (no degradation); No BOOT1; No JTAG; No SWO
STM32F038C6T6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	4 kBytes	38	48 MHz	Pin 20: "PB2" on F103 becomes "NPOR" on F038 (requires external device to manage power-on reset) Pin 35: "VSS on F103 becomes "PF6" on F038 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F038 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
STM32F051C4T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	16 kBytes	8 kBytes	39	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F051 (loss of wake-up pin; no hardware changes required); Pin 35: "VSS on F103 becomes "PF6" on F051 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F051 (unusable as GPIO); No BOOT1; No USB; No JTAG; No SWO
STM32F070C6T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	6 kBytes	37	48 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on F070 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F070 (loss of wake-up pin; no hardware changes required); No BOOT1; No JTAG; No SWO
STM32F078CBT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	16 kBytes	36	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F078 (loss of wake-up pin; no hardware changes required); Pin 20: "PB2" on F103 becomes "NPOR" on F038 (requires external device to manage power-on reset); No BOOT1; No JTAG; No SWO
STM32F098CCT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	32 kBytes	37	48 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F098 (loss of wake-up pin; no hardware changes required); Pin 20: "PB2" on F103 becomes "NPOR" on F038 (requires external device to manage power-on reset); No BOOT1; No USB; No JTAG; No SWO
STM32F100C6T6	ST Microelectonics	FALSE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	4 kBytes	37	24 MHz	No USB
STM32F101C4T6	ST Microelectonics	FALSE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	16 kBytes	4 kBytes	37	36 MHz	No USB
STM32F101C6T6	ST Microelectonics	FALSE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	6 kBytes	37	36 MHz	No USB
STM32F102C4T6	ST Microelectonics	TRUE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	16 kBytes	4 kBytes	37	48 MHz	
STM32F102C6T6	ST Microelectonics	TRUE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	6 kBytes	37	48 MHz	
STM32F102C8T6	ST Microelectonics	TRUE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	10 kBytes	37	48 MHz	
STM32F103C4T6	ST Microelectonics	TRUE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	16 kBytes	6 kBytes	37	72 MHz	
STM32F302C6T6	ST Microelectonics	TRUE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	16 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F302 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F302 (loss of wake-up pin; no hardware changes required); No BOOT1
STM32F302CCT6	ST Microelectonics	TRUE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	40 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F302 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F302 (loss of wake-up pin; no hardware changes required); No BOOT1
STM32F303C6T6	ST Microelectonics	FALSE	TRUE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	16 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F303 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F303 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F303 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
STM32F318C8T6	ST Microelectonics	FALSE	TRUE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	16 kBytes	36	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F318 (unusable as VREF-); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F0318 (loss of wake-up pin; no hardware changes required); Pin 20: "PB2" on F103 becomes "NPOR" on F318 (requires external device to manage power-on reset); No BOOT1; No USB
STM32F328C8T6	ST Microelectonics	FALSE	TRUE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	16 kBytes	36	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F328 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F328 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F328 (loss of wake-up pin; no hardware changes required); Pin 20: "PB2" on F103 becomes "NPOR" on F328 (requires external device to manage power-on reset); No BOOT1; No USB

STM32F358CCT6	ST Microelectonics	FALSE	TRUE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	48 kBytes	36	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F358 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F358 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F358 (loss of wake-up pin; no hardware changes required); Pin 20: "PB2" on F103 becomes "NPOR" on F358 (requires external device to manage power-on reset); No BOOT1; No USB
STM32F373CBT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	24 kBytes	37	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F373 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F373 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F373 (loss of wake-up pin; no hardware changes required); Pin 17: "PA7" on F103 becomes "VDD" on F373 (possibly requires jumper wire); Pin 23: "VSS" on F103 becomes "VSSSD/VREFSD-" on F373 (unusable as VREFSD-); Pin 24: "VDD" on F103 becomes "VDDSD" on F373 (VDDSD is tied to VDD); Pin 25: "PB12" on F103 becomes "VREFSD+" on F373 (no degradation); Pin 26: "PB13" on F103 becomes "PB14" on F373 (no degradation); Pin 27: "PB14" on F103 becomes "PB15" on F373 (no degradation); Pin 28: "PB15" on F103 becomes "PD8" on F373 (no degradation); No BOOT1
STM32F378CCT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	32 kBytes	36	72 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F378 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F378 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on F378 (loss of wake-up pin; no hardware changes required); Pin 17: "PA7" on F103 becomes "VDD" on F373 (possibly requires jumper wire); Pin 20: "PB2" on F103 becomes "NPOR" on F378 (requires external device to manage power-on reset); Pin 21: "PB10" on F103 becomes "PE8" on F378 (no degradation); Pin 22: "PB11" on F103 becomes "PE9" on F378 (no degradation); Pin 23: "VSS" on F103 becomes "VSSSD/VREFSD-" on F378 (unusable as VREFSD-); Pin 24: "VDD" on F103 becomes "VDDSD" on F378 (VDDSD is tied to VDD); Pin 25: "PB12" on F103 becomes "VREFSD+" on F378 (no degradation); Pin 26: "PB13" on F103 becomes "PB14" on F378 (no degradation); Pin 27: "PB14" on F103 becomes "PB15" on F378 (no degradation); Pin 28: "PB15" on F103 becomes "PD8" on F378 (no degradation); Pin 35: "VSS on F103 becomes "PF6" on F378 (unusable as GPIO); Pin 36: "VDD" on F103 becomes "PF7" on F378 (unusable as GPIO); No BOOT1; No USB
STM32F410CBT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	32 kBytes	35	100 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on F410 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on F410 (unusable as VREF+); Pin 22: "PB10" on F103 becomes "VCAP_1" on F410 (requires external capacitor); Pin 46: "PB9" on F103 becomes "VSS" on F410 (possibly required jumper wire); Pin 47: "VSS" on F103 becomes "PDR_ON" on F410 (Power supply supervisor permanently turned off; requires external supervisor); No USB
STM32G031C4T6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	16 kBytes	8 kBytes	43	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G041C6T6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	8 kBytes	43	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G041C8T6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	8 kBytes	43	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G071C6T6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	36 kBytes	44	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G081CBT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	36 kBytes	44	64 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G441CBT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	32 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G471CCT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	128 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G471CET6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	128 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32G483CET6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	128 kBytes	38	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32GBK1CBT6	ST Microelectonics	FALSE	FALSE	FALSE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	32 kBytes	42	170 MHz	Near as I can tell, all of the STM32G-series MCUs map the SWD pins (SWDIO/SWCLK) to pins 35/36 instead of pins 34/37, making them unsuitable for this breakout board (in addition to any other issues that might exist).
STM32L031C4T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	16 kBytes	8 kBytes	38	32 MHz	Pin 1: "VBAT" on F103 becomes "PC0" on L031 (no degradation); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L031 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
STM32L031C6T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	8 kBytes	38	32 MHz	Pin 1: "VBAT" on F103 becomes "PC0" on L031 (no degradation); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L031 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
STM32L041C6T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	8 kBytes	38	32 MHz	Pin 1: "VBAT" on F103 becomes "PC0" on L041 (no degradation); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L041 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB; No JTAG; No SWO
STM32L052C6T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	8 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L052 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L052 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L052 (no degradation); No BOOT1; No JTAG; No SWO
STM32L053C6T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	8 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L053 (same hardware requirements, different function); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L053 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L053 (no degradation); No BOOT1; No JTAG; No SWO
STM32L063C8T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	8 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L063 (same hardware requirements, different function); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L063 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L063 (no degradation); No BOOT1; No JTAG; No SWO
STM32L071C8T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L071 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L071 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDDIO" on L071 (no degradation); No BOOT1; No USB; No JTAG; No SWO
STM32L073CBT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L073 (same hardware requirements, different function); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L073 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L073 (no degradation); No BOOT1; No JTAG; No SWO

STM32L073CZT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	192 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L073 (same hardware requirements, different function); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L073 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L073 (no degradation); No BOOT1; No JTAG; No SWO
STM32L081CBT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L081 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L081 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDDIO" on L081 (no degradation); No BOOT1; No USB; No JTAG; No SWO
STM32L081CZT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	192 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VDD" on L081 (requires shorting resistor/solder blob on R2); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L081 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDDIO" on L081 (no degradation); No BOOT1; No USB; No JTAG; No SWO
STM32L083CBT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L083 (same hardware requirements, different function); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L083 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L083 (no degradation); No BOOT1; No JTAG; No SWO
STM32L083CZT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	192 kBytes	20 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L083 (same hardware requirements, different function); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L083 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L083 (no degradation); No BOOT1; No JTAG; No SWO
STM32L151C6T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	10 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L151C6T6A	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	16 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L151C8T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	10 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L151CBT6A	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	32 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L151CCT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	32 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L152C6T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	10 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L152C6T6A	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	32 kBytes	16 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L152C8T6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	64 kBytes	10 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L152CBT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	16 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L152CCT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	32 kBytes	37	32 MHz	Pin 1: "VBAT" on F103 becomes "VLCD" on L151 (same hardware requirements, different function); No SWO
STM32L412CBT6P	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	40 kBytes	36	80 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0/CK_IN" on L412 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L412 (no degradation); No BOOT1
STM32L422CBT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	128 kBytes	40 kBytes	38	80 MHz	Pin 10: "PA0-WKUP" on F103 becomes "PA0/CK_IN" on L412 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L412 (no degradation); No BOOT1
STM32L443CCT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	64 kBytes	38	80 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L443 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L443 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L443 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L443 (no degradation); No BOOT1
STM32L451CET6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	160 kBytes	38	80 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L451 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L451 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L451 (loss of wake-up pin; no hardware changes required); No BOOT1; No USB
STM32L462CET6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	160 kBytes	38	80 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L462 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L462 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L462 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L462 (no degradation); No BOOT1
STM32L4P5CET6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	320 kBytes	38	120 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L4P5 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L4P5 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L4P5 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L4P5 (no degradation); No BOOT1; Only OTG-FS ("on-the-go, full speed") USB
STM32L4P5CGT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	1024 kBytes	320 kBytes	38	120 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L4P5 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L4P5 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L4P5 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L4P5 (no degradation); No BOOT1; Only OTG-FS ("on-the-go, full speed") USB
STM32L4P5CGT6P	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	1024 kBytes	320 kBytes	36	120 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L4P5 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L4P5 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L4P5 (loss of wake-up pin; no hardware changes required); Pin 22: "PB11" on F103 becomes "VDD12" on L4P5 (no degradation); Pin 46: "PB9" on F103 becomes "VDD12" on L4P5 (no degradation); Pin 36: "VDD" on F103 becomes "VDD_USB" on L4P5 (no degradation); No BOOT1; Only OTG-FS ("on-the-go, full speed") USB
STM32L4Q5CGT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	1024 kBytes	320 kBytes	38	120 MHz	Pin 8: "VSS" on F103 becomes "VSS/VREF-" on L4Q5 (unusable as VREF-); Pin 9: "VSS" on F103 becomes "VDD/VREF+" on L4Q5 (unusable as VREF+); Pin 10: "PA0-WKUP" on F103 becomes "PA0" on L4Q5 (loss of wake-up pin; no hardware changes required); Pin 36: "VDD" on F103 becomes "VDD_USB" on L4Q5 (no degradation); No BOOT1; Only OTG-FS ("on-the-go, full speed") USB

STM32L4Q5CGT6P	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	1024 kBytes	320 kBytes	36	120 MHz	Pin 8: “VSS” on F103 becomes “VSS/VREF-” on L4Q5 (unusable as VREF-); Pin 9: “VSS” on F103 becomes “VDD/VREF+” on L4Q5 (unusable as VREF+); Pin 10: “PA0-WKUP” on F103 becomes “PA0” on L4Q5 (loss of wake-up pin; no hardware changes required); Pin 36: “VDD” on F103 becomes “VDD_USB” on L4Q5 (no degradation); No BOOT1; Only OTG-FS (“on-the-go, full speed”) USB
STM32L552CCT6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	256 kBytes	256 kBytes	38	110 MHz	Pin 8: “VSS” on F103 becomes “VSS/VREF-” on L552 (unusable as VREF-); Pin 9: “VSS” on F103 becomes “VDD/VREF+” on L552 (unusable as VREF+); Pin 10: “PA0-WKUP” on F103 becomes “PA0” on L552 (loss of wake-up pin; no hardware changes required); No BOOT1
STM32L552CET6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	256 kBytes	38	110 MHz	Pin 8: “VSS” on F103 becomes “VSS/VREF-” on L552 (unusable as VREF-); Pin 9: “VSS” on F103 becomes “VDD/VREF+” on L552 (unusable as VREF+); Pin 10: “PA0-WKUP” on F103 becomes “PA0” on L552 (loss of wake-up pin; no hardware changes required); No BOOT1
STM32L552CET6P	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	256 kBytes	36	110 MHz	Pin 8: “VSS” on F103 becomes “VSS/VREF-” on L552 (unusable as VREF-); Pin 9: “VSS” on F103 becomes “VDD/VREF+” on L552 (unusable as VREF+); Pin 10: “PA0-WKUP” on F103 becomes “PA0” on L552 (loss of wake-up pin; no hardware changes required); Pin 22: “PB11” on F103 becomes “VDD12_1” on L562 (no degradation); Pin 46: “PB9” on F103 becomes “VDD12_2” on L462 (no degradation); No BOOT1
STM32L562CET6	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	256 kBytes	38	110 MHz	Pin 8: “VSS” on F103 becomes “VSS/VREF-” on L562 (unusable as VREF-); Pin 9: “VSS” on F103 becomes “VDD/VREF+” on L562 (unusable as VREF+); Pin 10: “PA0-WKUP” on F103 becomes “PA0” on L562 (loss of wake-up pin; no hardware changes required); No BOOT1
STM32L562CET6P	ST Microelectonics	FALSE	FALSE	TRUE	FALSE	#N/A	#N/A	#N/A	#N/A	512 kBytes	256 kBytes	36	110 MHz	Pin 8: “VSS” on F103 becomes “VSS/VREF-” on L562 (unusable as VREF-); Pin 9: “VSS” on F103 becomes “VDD/VREF+” on L562 (unusable as VREF+); Pin 10: “PA0-WKUP” on F103 becomes “PA0” on L562 (loss of wake-up pin; no hardware changes required); Pin 22: “PB11” on F103 becomes “VDD12_1” on L562 (no degradation); Pin 46: “PB9” on F103 becomes “VDD12_2” on L462 (no degradation); No BOOT1