ECE 3700 Lab 02: Adder Circuitry

September 12, 2024

Rubric

Tasks	Point value
Full adder code	0
Ripple-carry code, schematic, synthesis and timing info	4
Look-ahead code, schematic, synthesis and timing info	4
8-bit adder	2
Good explanation of carry logic for look-ahead adders	2.5
Testbench and Simulation of all the code you wrote except the full adder	10
Reasonable conclusion	2.5
Checkoff	5
Total	30

Objectives

- Learn/practice instantiating submodules to create ripple-carry adders.
- Understand the math behind how look-ahead adders work.
- More practice writing and simulating testbenches.
- Use a variety of the quartus tools to observe the area/performance trade-off between the look-ahead and ripple-carry designs.
    i. The timing analyzer
    ii. RTL schematic (RTL viewer)
    iii. Map report (technology map viewer)

iv Synthesis Report

v Place route report.

- Practice looking in a manual for information (pin assignments).

Things I expect to see in your reports

1. Your code for:

   i Full adder

   ii Look-ahead adder

   iii Look-ahead testbench

   iv ripple-carry adder

   v ripple-carry testbench

   vi 8-bit adder

   vii 8-bit testbench

   (If you want to write the same testbench to test all your adders, that is okay. As always, the goal of these reports is not to make you work hard. I just want to see that you worked through each task and learned the objectives.)

2. Pictures of all the waveforms you simulated including the console output.

3. Description of how you got the equations for the look-ahead carries.

4. Some kind of conclusion about the area-performance trade-offs between the two adder designs. Do your observations match what you expected? If not, take a guess why. Unexpected results do not always mean your implementation was wrong.

5. Include screenshots of the timing analyzer and schematics you generated.