2020 IEEE International Conference for Innovation in Technology (INOCON)
Bengaluru, India. Nov 6-8, 2020

Low Power SoC for Mil-Std 1553 Cable Fault Detection

Sowmya Madhavan
Dept.of Electronics and Communication Engineering
Nitte Meenakshi Institute of Technology
Bangalore, India
sowmya.madhavan@nmit.ac.in

Dr S Sandya
Dept.of Electronics and Communication Engineering
Nitte Meenakshi Institute of Technology
Bangalore, India
sandya9prasad@gmail.com

***Abstract*—The safety of aircraft operation has always been the major need across globe. Faults on the aircraft system wiring have led to disasters, causing loss to human life and nation's economy. To avoid such incidents, early detection of faults like Opens or Shorts on cables play a very important role in preventing catastrophic failure and ensuring safety of flight. Any fault like Open or Short occurring on the Mil-Std 1553 cable used in aircraft systems is addressed by introducing redundancy having 1:1 or 1:2 channels instead of only one. A fault detection solution comprises of a Test Signal generation method and a processing method. From the literature survey, the author infers that Spread Spectrum Time Domain Reflectometry (SSTDR) is the Test Signal generation method used for avoiding interference between Test Signal and the actual Data Signal on Mil-Std 1553 cable. Continuous Wavelet Transform (CWT) can be used for statistical feature extraction and Probabilistic Neural Network (PNN) can be used for fault type localization and classification. So CWT-PNN algorithm is the processing method. In this research, the author has proposed and implemented a fault detection solution which is the combination of SSTDR, CWT and PNN. The test set-up inclusive of this combination has been simulated for three different scenarios, namely No Fault, Open Circuit Fault and Short Circuit Fault in MATLAB environment with the modeling of Mil-Std 1553 cable in SIMULINK. A prototype of the Mil-Std 1553 cable fault detection system is implemented on Artix 7 Nexys DDR Field Programmable Gate Array (FPGA) as a System on Chip (SoC) design. It is observed that for both open circuit and short circuit cases, the simulated faults in MATLAB-SIMULINK environment are conforming to the simulated faults from the FPGA prototype with an accuracy of less than 1mm cable length. The FPGA prototype power consumption is16mW.**

Keywords—Aircraft systems, Open Faults, Short Faults, Redundancy, Spread Spectrum Time Domain Reflectometry, Continuous Wavelet Transform, Probabilistic Neural Network, FPGA Prototype.

I. INTRODUCTION

An aircraft system is formed by the integration of a number of sub-systems such as propulsion sub-system, structure sub-system, electrical power distribution sub-system etc [1]. The interconnections between these sub-systems are realized through bundles of different type of cables which are varying in size, electrical properties etc. Mil-Std 1553 is one of these special types of cables. It is a military standard data bus used for data communication between the sub-systems of an aircraft. Though special care, regular monitoring and inspection of these cables are done, still several disturbances occur at the system level due to prevalence of faults in the cables.

Fault detection in aircrafts holds prime significance in order to optimize the different aspects such as availability, reliability, maintenance and finally life span. Though the protection for the core conductor part of the cable is achieved by the insulator layer, but the insulator layer itself is prone to wear and tear, with the passage of time due to the impact of certain environmental conditions such as moisture, radiations, mechanical vibration, chemical corrosion, temperature, electric field etc [2]. This wear and tear causes unfavorable effects on the electrical material which further causes failures that might lead to rupture and electrical discharges in aircraft sub-systems, leading to catastrophic failures. Hence there is a need of an automatic fault detection system which has to be developed by using advanced technologies that enables detection of faults prior to the failure of system, avoiding human intervention [3].

The predominant focus of this research work is on intermittent fault detection and localization on MILITARY STANDARD 1553, wired systems, from now onwards termed as "Mil-Std 1553 cable". Hence, a background study has been done to understand functional characteristics of the Mil-Std 1553 wire system, reflectometry concepts and different machine learning methods, that as a result could enable a suitable solution for the fault detection and localization. Considering the critical safety as well as set-up complexity of the aircraft system, it requires automated and highly precise wire fault detection system. Considering the need for real time and efficient automated System-On-Chip (SOC) fault detection, localization and classification system, it becomes imperative to assess hardware suitability and efficiency of the developed SoC [4]. With these motivations, in this thesis, the prime focus is made on developing a robust, low power SOC fault detection, localization and classification system, which can detect intermittent faults on Mil-Std 1553 cable.

II. LITERATURE SURVEY

Review of earlier work is divided into sub-topics which are as follows:

- Rudimentary methods of detection
- Types of reflectometry
- Processing methods for fault detection and localization.

A. Rudimentary Methods of Detection

Rudimentary methods are those where classical testing concepts are applied. These fault detection methods comprise identifying fault manually through multi-meters and through Arc Fault Circuit Interrupters (AFCI).

In aircrafts, there are hundreds of kilometers of wires running from one sub- system to another and hence the classical manual detection through multi-meters seems

978-1-7281-9744-9/20/$31.00 ©2020 IEEE

inefficient. In AFCI approach, electric arcing takes place when electric current flows via an air gap between conductors. Generally, arcing takes place due to frayed wiring, infiltration of metallic protests through power lines, corrupted or cut wiring protection or debased electrical associations [5]. However the arc fault circuit breakers have two main hurdles: first, they can identify only arcing or short circuits i.e. open circuit faults cannot be detected. Second, the arc fault circuit breakers isolate the lines even though the amount of current caused by the arc is less compared to the upper limiting current of the AFCB.

B. Types of Reflectometry

Practically, it has been observed that reflectometry methods provide much more efficacy in comparison with rudimentary techniques. The reflectometry methods transmit signal through the line which is reflected back from points such as open or short circuits where there are variations in impedances. The known reference input signal transmitted on the cable is the 'Test Signal' and the type of test signal transmitted is used to identify each type of reflectometry.

To detect cable faults, reflectometry methods have been found as promising solutions. The concept of reflectometry methods is to transmit a test signal on a wire, which is later tested for any reflected signal. If the incident test signal reaches the load end, then the Wire Under Test (WUT) does not have any fault. However, in case of any short circuit or open circuit fault, the load impedance is unequal to the characteristic impedance of the transmission line and thus the transmitted signal will not reach its destined point [6]. However, it gets reflected. Computing the characteristics of reflected transmitted signal will be helpful in finding out the location of fault.

Some of the standard reflectometry methods are **Time Domain Reflectometry (TDR), Frequency Domain Reflectometry (FDR), Noise Domain Reflectometry (NDR), Mixed Signal Reflectometry (MSR), Multiple Carrier Reflectometry (MCR), Time Reversal Reflectometry (TRR), Sequence Time Domain Reflectometry (STDR), Spread Spectrum Time Domain Reflectometry (SSTDR).**

In the process of TDR, a square wave pulse or step function is transmitted on the cable and the reflections are measured as per the changes in power, generally in picoseconds [7]. These reflections notify the variation in impedance in the wires along with connectors and the distance to the fault, which may be an open circuit or a short circuit. The parameters used for calculating distance to the fault are the time taken by the reflected signal to reach the source of the incident signal, speed of propagation and length of the cable. In addition, the phase or sign of the reflected wave also varies for open or short circuit faults. Apart from the square wave as a test signal, Gaussian pulses can also be used. Though TDR is a very commonly and most exploited technique, its results are very difficult to compute.

In FDR, broadcasting a group of stepped-frequency sinusoidal waves to reach the cable's end point and back to the injection point is the procedure carried out, unlike the square pulse transmission used in TDR. Both the incident and the reflected waves are observed by using the electronic equipment employed at the source end.

FDR is generally classified into three types, namely Frequency Modulated Continuous Wave (FMCW) systems, Standing Wave Reflectometry (SWR), and Phase Detection Frequency Domain Reflectometry (PDFDR) systems [8]. Cable fault detection in radar applications employs all above three FDR systems. However, the type of wire faults cannot be detected.

In **FMCW** systems, sinusoidal signals which are of high frequency, which are linearly ramped up in time, are used. By exploiting a directional coupler, the reflecting signal is distinguished from the incident signal. Length of the cable as well as the elapsed time is obtained from the difference between the reflected signal and the increased frequency of the incident signal. In **SWR** systems, a sinusoidal wave of high frequency is sent on the cable. Here, a standing wave is generated by superimposing incident and reflected waves. Separation of the incident and the reflected wave is not done in this fault location technique. The frequency thus transmitted is varied from KHz to MHz range and continued until a null is detected at source. This huge range of frequency transmission increases the complexity of separating the test signal from the aircraft data signal. It also makes it difficult to identify the null in the injected signal, thus making the method noise sensitive, sensitive to line losses and to frequency dependent loads. In **PDFDR** systems, a group of sine waves is transmitted on the cable. Once the signals are transmitted successfully, directional couplers are employed to separate the incident wave from the reflected wave and then the latter is mixed with the former. After mixing, a DC voltage which is proportional to the phase shift is generated which varies in a sinusoidal form with the linear sweep of frequency. Directional couplers installed both in FMCW and PDFDR cannot be combined in a circuit package or Field Programmable Gate Array (FPGA) prototype at the specified frequencies.

Noise Domain Reflectometry (NDR) technique exploits the noise signals and examines associated reflections rather than injecting a known impulse [9]. In this method, an existing noise signal is considered as the test signal, thus eliminating the need to produce an extra test signal. In this way this technique is helpful in locating wire faults without using an external signal. Obtaining the information about fault becomes extremely difficult through NDR if the reflected signal is found to be over corrupted due to noise. This is the limitation of NDR that confines its suitability for fault detection on Mil-Std 1553 wire system.

MSR concept follows PDFDR concept, except that it does not need directional couplers for the separation of test signal and reflected signal. Such feature enables it to be applied on a Field Programmable Gate Array (FPGA). MSR outperforms PDFDR where it exhibits better performance and also is cost-effective [10]. Additionally, the distortion in the sinusoid observed and error during translation to Fourier Transform and eventually to the length of the wire is lesser when MSR is implemented. But the error value becomes high during low frequency response because of the lower magnitude of the signal sent down the wire. Also, the undeniable disadvantage of MSR is that it cannot be applied on aircraft wires such as Mil-Std 1553 because the wide range of frequencies employed in MSR can cause interference with the aircraft wire's signals.

Pseudo Noise (PN) sequence which exhibits better self-correlation is used as the test signal for (STDR) [11].

Represented by set of precisely designed zeros and ones, PN code is deterministic and a Recursive Linear Sequence (RLS). The test signal along with the existing data signal is transmitted on the wire under study. PN sequence will be a lengthy sequence, even though the magnitude is less. The pattern of the PN sequence will be decided by the designer. Since STDR requires less power consuming circuits, it is generally implemented for low power devices. However STDR cannot be exploited for wires carrying digital data like Mil-Std 1553 since it can interfere with the actual data signal on the cable. The accuracy to which the fault is detected on the wire is defined as the resolution of fault detection and the observed resolution for STDR is around 1 foot which is not sufficient for an aircraft wiring.

Spread Spectrum Time Domain Reflectometry (SSTDR) has proven its efficacy in detecting intermittent faults on aircraft wires that carry typical aircraft signals [12]. The uniqueness of SSTDR lies in the fact that it can detect the reflected signal even when it is corrupted by noise. This unique feature of SSTDR is due to an attribute known as 'Processing Gain'. The processing gain for a DSSS-SSTDR is given as:

$$PG = \frac{T_s}{T_c} = \frac{R_C}{R_S} = \frac{W_{ss}}{2R_S} \quad (1)$$

In the above equation, the parameter WSS refers to the bandwidth of the spread-spectrum signal, T_S refers to the period taken by one complete SSTDR sequence, T_C signifies the period of a PN code chip, R_C refers to the chip rate of the PN sequence (chips per second) and R_S refers to the symbol rate (number of full sequences per second). The processing gain signifies that a spread spectrum test perform appropriately even in noisy environments.

C. *Processing methods for Fault Detection and Localization.*

The process of fault diagnosis has been divided into three major parts:

- System modeling in which fault has to be found. The system may be any cable, electrical machine or robot where the fault has to be found out.
- Extraction of the statistical features or indices with suitable sensitivity to the fault.
- Classifying and differentiating the different faults on the basis of the obtained values of the attributes.

The feature extraction process can be of paramount significance, as without it, a large number of methods cannot be implemented precisely [13]. One of the most commonly used feature extraction technique is the Wavelet Transform (WT). This technique is implemented in several fault detection systems. Most of the works have implemented Discrete Wavelet Transform (DWT) as compared to Continuous Wavelet Transform (CWT). But, applying DWT produces some errors in fault type and fault location.. Hence while applying any type of WT, the selection of mother wavelet has to be decided by the researcher, before actually creating the features.

A Probabilistic Neural Network (PNN) is a feed forward neural network, which is extensively used in classification and pattern recognition problems. A feed forward neural network is one in which the interconnections between the nodes do not form a cycle [14]. It is a type of Artificial Neural Network (ANN). A Parzen window technique and a non-parametric function are employed in the PNN algorithm for the estimation of the parent Probability Distribution Function (PDF) of each class. The class probability of a new set of input data is approximated by making use of each class and then the Bayes' rule is utilized to assign the class with maximum succeeding probability to new set of input data. The main advantage of the above method is that the probability of mis-classification is reduced.

From the detailed literature survey, it can be inferred that SSTDR is the best method for test signal generation and CWT- PNN techniques can be used to locate the type of fault and fault distance with high accuracy for Mil-Std 1553 cable. From the survey, there is no evidence of work being done with the combination of SSTDR, CWT and PNN for fault detection, localization and classification. Hence in this research paper, the author proposes a solution for fault detection, localization and classification with the combination of SSTDR, CWT and PNN on Mil-Std 1553 cable.

III. TEST SETUP

All the electrical characteristics of Mil-Std 1553 cable are considered and the cable is modeled in SIMULINK. The Resistance (R), Inductance (L) and Capacitance (C) of the cable are incorporated into the PI section model. The characteristic impedance of the cable is 75Ω [15]. A fault simulator is designed to operate in either of the three cases, namely (i) Normal Cable (ii) Open Circuit Cable (iii) Short Circuit Cable. Mil-Std-1553 data signal is generated at 1MHz frequency and 6V peak-to-peak amplitude. SSTDR Test Signal is generated at 30MHz frequency and 0.02V peak-to-peak amplitude. Data Signal and Test Signal are combined in the adder. The test signal is superimposed on the data signal after combining. The Controlled Voltage Source block converts the output of the adder into differential physical voltage levels and places the differential signal onto the actual Mil-Std 1553 cable. Analysis block captures the reflected signal for further processing for fault detection and localization. The test- setup for fault detection, localization and classification is as shown in Fig 1.

IV. FAULT ANALYSIS SYSTEM USING CWT-PNN

Although, wavelet analysis and machine learning based approaches have been found as a potential solution for fault detection and localization and its suitability for Mil-Std 1553 wire-system has not been assessed till now. With this motivation, in this research paper, a robust Continuous Wavelet Transform (CWT) and Probabilistic Neural Network (PNN) based fault detection and localization scheme is developed. The implementation details of this algorithm in which the fault location is detected by using the intelligent technique PNN assisted by the feature extraction method of Morlet Wavelet Transform and its signal characteristics as the input to the network that is trained is presented here. The signal characteristics or statistical features include Power Spectral Density (PSD), Wavelet Coherence and Cross Wavelet Transform .All these signal characteristics of the reflected wave are considered for accurate prediction of the fault in the transmission system.

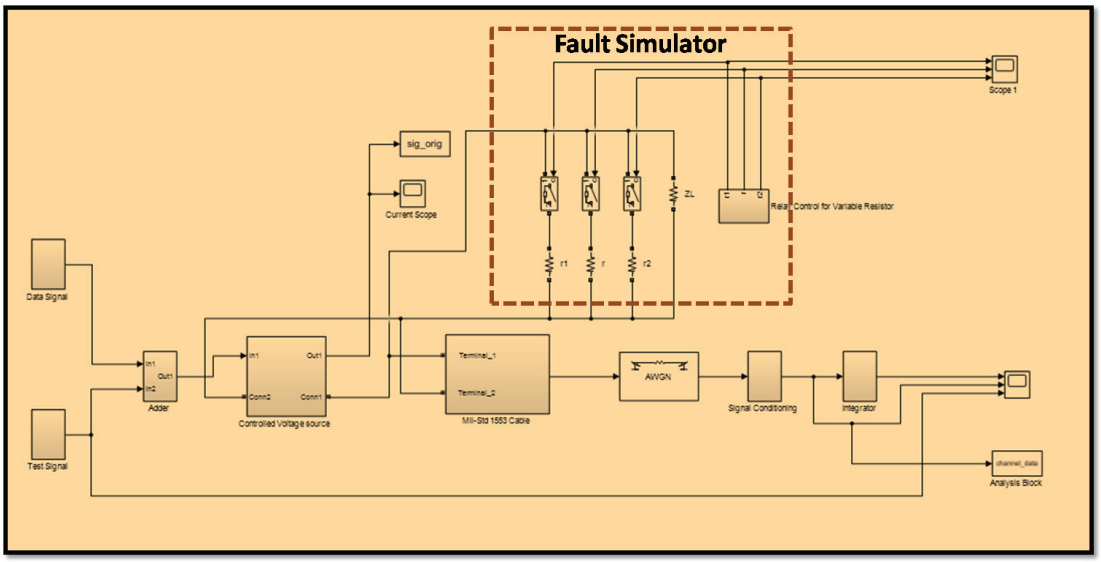

Fig. 1. MATLAB/SIMULINK Model of Mil-Std 1553 Cable with Test Signal and Data Signal

The implementation models for the CWT-PNN algorithm is presented below. Once estimating the features is done, all the features along with the co-efficients obtained from CWT are fed as input to the PNN for further classification and fault localization. The overall implementation model for the CWT-PNN based fault detection and localization scheme is presented below.

The overall implementation model can be divided into two modes, namely the Training Mode and the Testing Mode.

- Training Mode Implementation: This is the first and the most important step in fault detection and localization. Training mode involves training the PNN for finding the values of weights which are connected to each node. The result of training mode implementation is saved as a .mat file. The flow chart for the training mode implementation is as shown in Fig 2.
- **Testing Mode Implementation:** This is the next step in fault detection and localization. Testing mode involves testing the PNN for real inputs. The flow chart for the training mode implementation is as shown in Fig. 3.

To perform CWT based feature extraction, Morlet wavelet was applied that enabled retrieval of the wavelet coefficients and the statistical features. The statistical features extracted are Power Spectral Density (PSD), Cross Wavelet Power and Wavelet Transform Coherence. After obtaining the statistical features, these features and the values of current during different conditions are given to PNN classifier that eventually gives type of fault and its location. Noticeably, in this simulation has been performed for three-class classification (i.e., open-circuit fault and short-circuit fault), which has been obtained for the different reference fault locations.

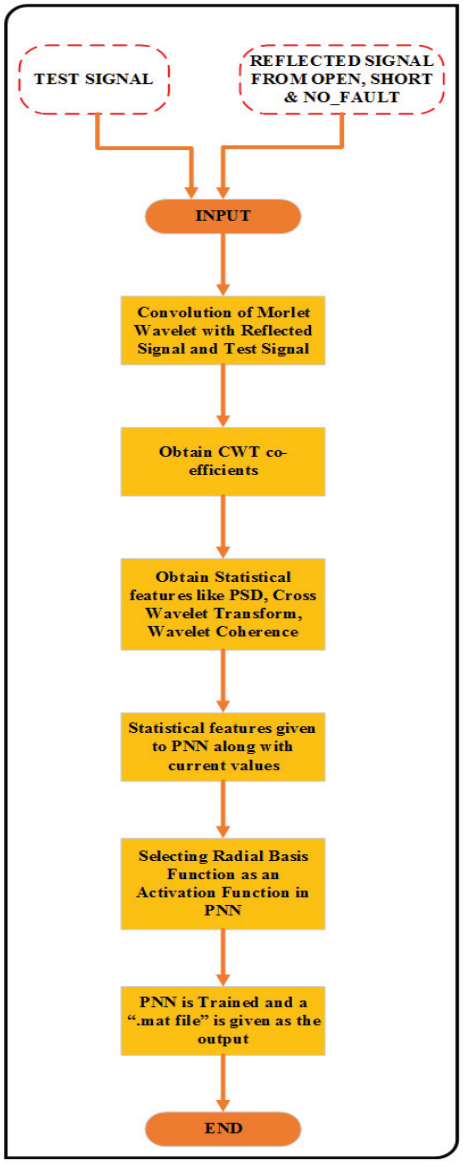

Fig. 2. Training Mode Implementation Flow Chart

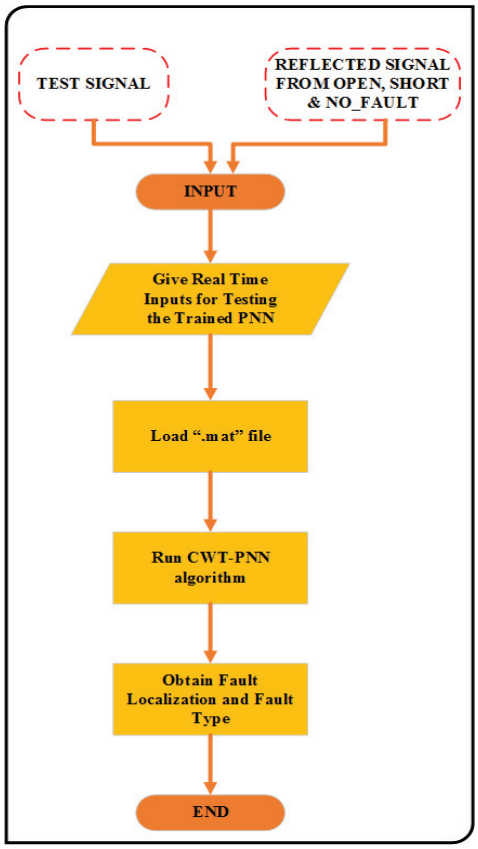

Fig. 3. Testing Mode Implementation Flow Chart

V. RESULTS FROM MATLAB SIMULATION

The MATLAB-SIMULINK simulated test setup is designed for three different scenarios, namely: No Fault Case, Open Fault Case and Short Fault Case.

A. No Fault Case

The fault simulator selects the resistor r, having a value of 75Ω so that characteristic impedance of the cable is equal to the load impedance. Hence no reflection of the Test Signal is observed. In this case, the statistical features are extracted only for the Test Signal since the reflected signal is zero. Power spectral density of the Test Signal is as shown in Fig. 4.

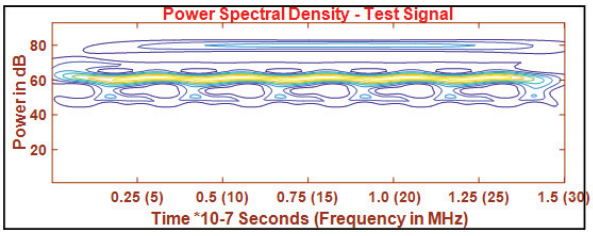

Fig. 4. Power Spectral Density of the Test Signal

From the above figure, it can be inferred that the power is uniformly distributed across all the samples and output signal is same as the input Test Signal.

Reflection co-efficient versus distance along the length of the cable plot is as shown in the Fig.5.

Plot shows the reflection co-efficient as zero because the reflected signal is zero. It is inferred that the cable is healthy and hence No fault on the cable.

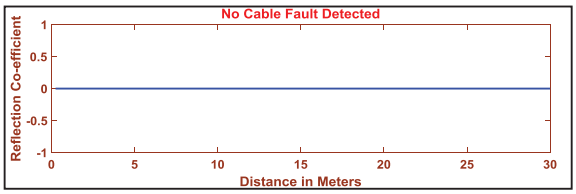

Fig. 5. Correlation Plot for No_Fault Case

B. Open Circuit Fault Case

The fault simulator selects the resistor r1, having a value of 100MΩ so that characteristic impedance of the cable is unequal to the load impedance and open circuit faults can be introduced on the cable at a definite distance. As an example, the authors have taken the fault induced distance as 10 meters. However, the algorithm works for any distance lesser than or equal to 30 meters.

- Power Spectral Density of the reflected signal is as shown in Fig.6.
- Cross Wavelet Power between input Test Signal and the reflected signal for fault induced at 10 meters is as shown in the Fig.7.
- Wavelet Transform Coherence is the coherence of the cross wavelet transform, that is, it checks whether the Test Signal and the reflected signal are having the same phase difference or not. The wavelet transform coherence is as shown in Fig.8.
- **Distance to Fault** plot is as shown in Fig.9.

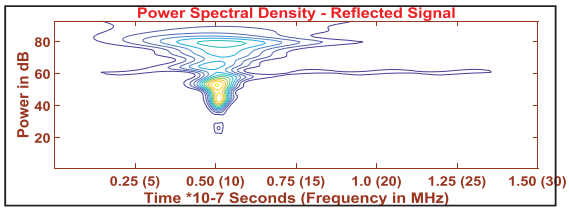

Fig. 6. PSD Of Reflected Signal at 10m Open Fault

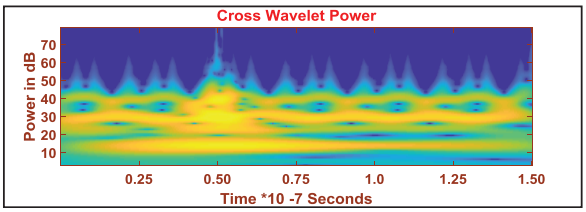

Fig. 7. Cross Wavelet Power for Open Fault Induced at 10m

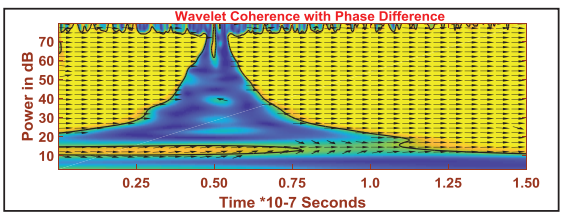

Fig. 8. Wavelet Coherence for Open Fault Induced at 10m

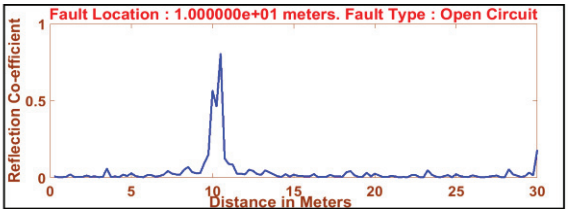

Fig. 9. Distance to Fault for 10m Open

- From Fig.6, it can be inferred that the power spectral density is concentrated at around 0.5x10-7 seconds and a kink is seen at 0.5x10-7 seconds which maps onto the open location of 10 meters on the cable.
- From Fig.7, it can be inferred that the contour of the cross wavelet power has a sudden change at around 0.5x10-7 seconds which maps onto the location of 10 meters on the cable. The importance of this cross wavelet power distribution is that regions of large power can be determined. Regions of large power can deduce the portions of the signal which are important and the portions which can be ignored.
- From Fig.8, it can be inferred that the Test Signal and reflected signal are highly uncorrelated in phase and has high uncorrelated power at 0.5*10-7 seconds which maps onto the location of 10 meters on the cable. The rightward pointing arrows indicates that the test signal and the reflected signals are in phase, that is, 0 phase lag, a bottom-right arrow indicates a small lead of Test Signal and a left pointing arrow indicates that Test Signal and reflected signals are anti-correlated.

From the figures 6,7 & 8, it can be inferred that at 0.5*10-7 seconds, where fault is induced, there is a huge change in the coherence contour. Contour is an outline which represents an irregular shape. Even though Power Spectral Density, Cross Wavelet Power and Wavelet Coherence infer almost the same, all of these parameters are given to the Probabilistic Neural Network so that it can predict the fault localization accurately.

Fig.9 shows the value of the reflection co-efficient on Y-axis and the distance on X - axis. From this figure, the exact distance on the cable where the open fault has occurred is shown by a positive peak at that point. The distance value is 1.000000 x 10, that is, has six digits of accuracy and the type of fault is Open.

C. Short Circuit Fault Case

The fault simulator selects the resistor r2, having a value of 1Ω so that characteristic impedance of the cable is unequal to the load impedance, current takes a high value and short circuit fault can be introduced on the cable at a definite distance. As an example, the authors have taken the fault induced distance as 10 meters. However, the algorithm works for any distance lesser than or equal to 30 meters.

- Power Spectral Density of the reflected signal is as shown in Fig.10.
- Cross Wavelet Power between input Test Signal and the reflected signal for fault induced at 10 meters is as shown in the Fig.11.
- Wavelet Transform Coherence is the coherence of the cross wavelet transform, that is, it checks whether the Test Signal and the reflected signal are having the same phase difference or not. The wavelet transform coherence is as shown in Fig.12.
- **Distance to Fault** plot is as shown in Fig.13.

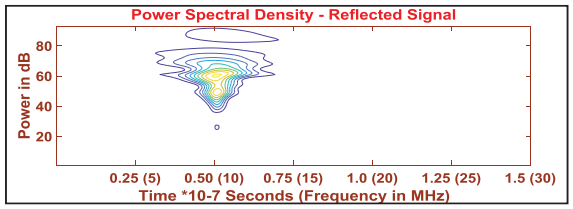

Fig. 10. PSD of Reflected Signal at 10m Short Fault

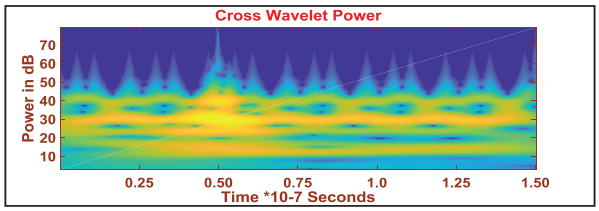

Fig. 11. Cross Wavelet Power for Short Fault Induced at 10m

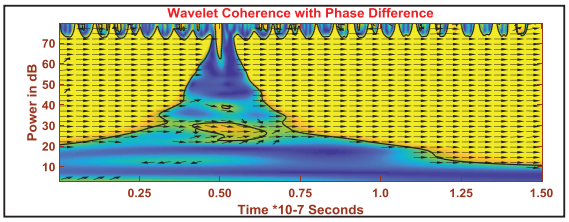

Fig. 12. Wavelet Coherence for Short Fault Induced at 10m

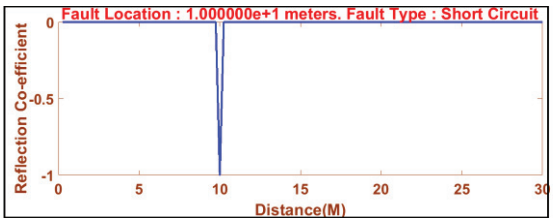

Fig. 13. Distance to Fault for 10m Short

- From Fig.10, it can be inferred that the power spectral density is concentrated at around 0.5x10-7 seconds and a kink is seen at 0.5x10-7 seconds which maps onto the short location of 10 meters on the cable.
- From Fig.11, it can be inferred that the contour of the cross wavelet power has a sudden change at around 0.5x10-7 seconds which maps onto the location of 10 meters on the cable. The importance of this cross wavelet power distribution is that regions of large power can be determined. Regions of large power can deduce the portions of the signal which are important and the portions which can be ignored.
- From Fig.12, it can be inferred that the Test Signal and reflected signal are highly uncorrelated in phase and has high uncorrelated power at 0.5*10-7 seconds which maps onto the location of 10 meters on the cable. The rightward pointing arrows indicates that the test signal and the reflected signals are in phase, that is, 0 phase lag, a bottom-right arrow indicates a small lead of Test Signal and a left pointing arrow indicates that Test Signal and reflected signals are anti-correlated.

From the figures 10,11 & 12, it can be inferred that at 0.5*10-7 seconds, where fault is induced, there is a huge change in the coherence contour. Contour is an outline which represents an irregular shape. Even though Power Spectral Density, Cross Wavelet Power and Wavelet Coherence infer almost the same, all of these parameters are given to the Probabilistic Neural Network so that it can predict the fault localization accurately.

Fig.13 shows the value of the reflection co-efficient on Y- axis and the distance on X - axis. From this figure, the exact distance on the cable where the short fault has occurred is shown by a negative peak at that point. The distance value is 1.000000 x 10, that is, has six digits of accuracy and the type of fault is Short.

VI. RESULTS FROM FPGA IMPLEMENTATION

Fault analysis and detection system using CWT equivalent has been implemented on FPGA for realizing a hardware prototype and is discussed in this section. System on Chip (SOC) prototyping is done on FPGA (Field Programmable Gate Array) for hardware testing and verification and rapid software growth. Before taping out an IC, it is always preferable to bring out a FPGA prototype, for ensuring its functional correctness. It is estimated that fault free percentage of SoC designs is just 33.33% during first silicon pass 0. FPGA prototyping offers a single platform solution for testing and verification of hardware, firmware and application software designs, well before the initial silicon pass happens. FPGA resources include Look-Up-Tables (LUTs), D Flip-Flops, block RAMs, digital signal processors (DSPs), clock buffers, etc.

The FPGA implementation block diagram is shown below in Fig.14.

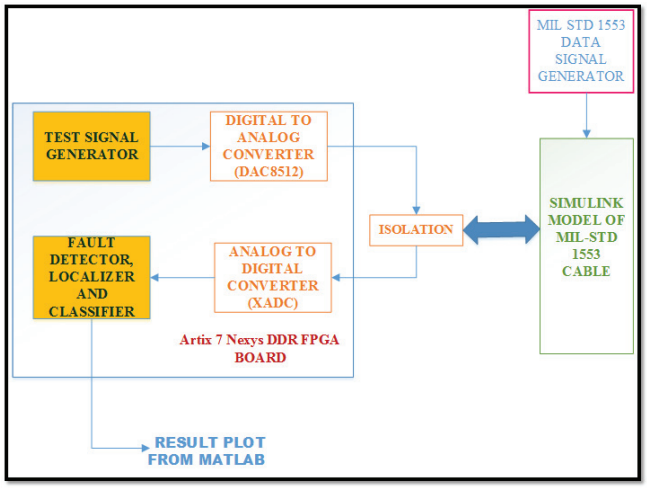

Fig. 14. Cable Fault Detection Implementation Block Diagram

In this research, the Test Signal generator block and the fault detector, localizer and classifier block are designed and developed using Verilog. Test signal is generated in the FPGA and is input to Digital to Analog Converter (DAC). Analog signal from DAC is passed through the isolation capacitor to the Mil-Std 1553 model on SIMULINK. The reflected signal from the Mil-Std 1553 model forms input to the Analog to Digital Converter (ADC) of FPGA. The output of ADC is the input to the fault analyzer and detector block. The fault detector, localizer and classifier block generates a bit stream which gives the location and type of fault. The bit stream output from chipscope debugger of FPGA is plotted as a continuous function from MATLAB.

The FPGA prototype is also tested for three different test scenarios namely: No Fault Case, Open Fault Case and Short Fault Case. Fault detection system for all the above scenarios is realized in hardware and debugged from the chipscope debugger. The output from the chipscope debugger will be a set of binary/signed decimal numbers at a corresponding address. The output file generated by chipscope should be read by MATLAB for getting the final distance to fault plot.

A. No Fault Case

In the no fault case, there is no fault induced on the cable. The output from the chipscope debugger of FPGA is as shown in Fig.15.

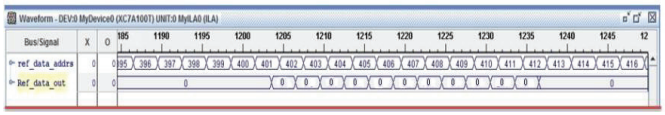

Fig. 15. Zero Chipscope Output for No Fault Case

As shown in the above Fig, the FPGA processing result is zero since the reflected signal is zero. The distance to fault plot is as shown in Fig.16.

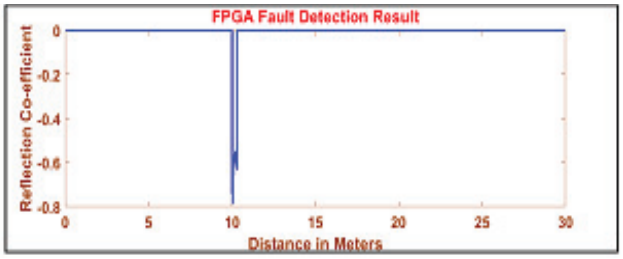

Fig. 16. No Fault

Plot shows the reflection co-efficient as zero because the reflected signal is zero. It is inferred that the cable is healthy and hence No fault on the cable.

B. Open Circuit Fault Case

Fault is induced at 10 metres, type of fault is **OPEN.** The output from the chipscope debugger of FPGA is as shown in Fig.17.

Fig. 17. Chipscope output for OPEN fault at 10 meters

From the above figure, it can be inferred that the FPGA output is non-zero and it is positive, starting from the 400th address. The distance to fault plot is as shown in Fig.18.

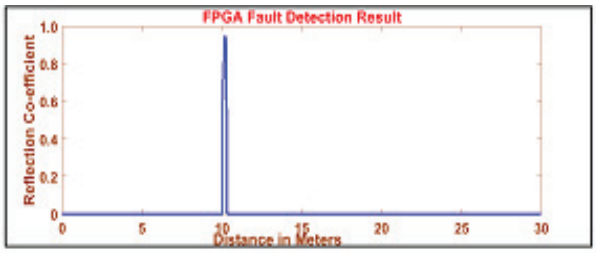

Fig. 18. 10m OPEN Fault

Plot shows a positive peak at 10 meters which gives the location of the fault, fault type being Open Circuit.

C. *Short Circuit Fault Case*

Fault is induced at 10 metres, type of fault is **SHORT.** The output from the chipscope debugger of FPGA is as shown in Fig.19.

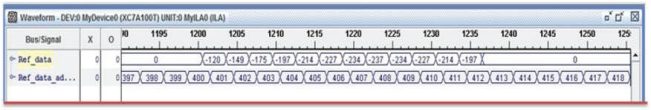

Fig. 19. Chipscope output for SHORT fault at 10 meters

From the above figure, it can be inferred that the FPGA output is non-zero and it is negative, starting from the 400th address. The distance to fault plot as shown in Fig.20.

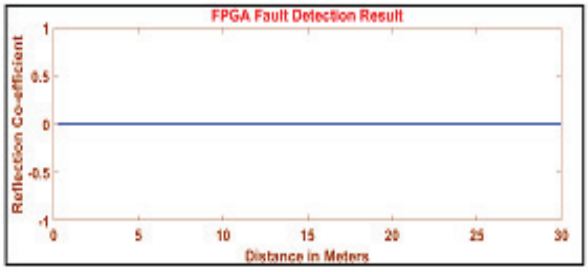

Fig. 20. 10m SHORT Fault after MATLAB read

Plot shows a negative peak at 10 meters which gives the location of the fault, fault type being Short Circuit.

VII. POWER REPORT

TABLE I. SUMMARY OF XILINX XPOWER ANALYZER

Xilinx XPower Analyzer- mil_std_1553_synth_tb.ncd- [Table_View]				
Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
VCCint	1.000	0.003	0.002 (A_1)	0.003 (A_{11})
Vacaux	1.800	0.005	0.001 (A_2)	0.002 (A_{22})
VCC033	3.300	0.005	0.001 (A_3)	0.001 (A_{33})
VCCbram	1.000	0.000	0.000 (A_4)	0.000 (A_{44})

Dynamic Power Consumption = (VCCint) (A_1) + (Vacaux) (A_2) + (VCC033) (A_3) + (VCCbram) (A_4)

Quiescent Power Consumption = (VCCint) (A11) + (Vacaux) (A22) + (VCC033) (A33) + (VCCbram) (A44)

Where

VCCint is the power supply for the internal Configurable Logic Blocks (CLBs), clock trees, Block RAMs, input buffers and routing.

Vacaux is the power supply for clock managers.

VCC033 is the power supply for all output buffers.

The power report for 10m OPEN is as shown in Table II . However, it is seen that for all the test scenarios, the power consumption remains the same. From the power report, the dynamic power consumption is 0.007W and the quiescent power consumption is 0.009W. Dynamic power is the power consumed while the inputs are active. Quiescent power, also called static power is the power consumed by the device when it is powered on, configured with user logic and there is no switching activity. The total power consumption is 0.016W.

VIII. CONCLUSION

TABLE II. COMPARISON OF FAULT DETECTION DEVICES

Reflectometry Type	Accuracy	Power Consumption	Type Of Processing Method
Sequence Time Domain Reflectometry	1 foot	39.9mW	Time Domain Vernier
Spread Spectrum Time Domain Reflectometry	3 centimeters	4W for complete handheld device	Curve Fitting Algorithm
Spread Spectrum Time Domain Reflectometry (SSTDR) (Present Research Paper)	0.001millimeters	16mW	CWT for feature extraction and PNN for classification

REFERENCES

[1] Integrated System Health Management (ISHM) Technology Demonstration Project Final Report, NASA TM 2006-213432, December 15, 2005.

[2] Understanding Wire Chafing: Model Development and Optimal Diagnostics Using TDR, S. Schuet K, Wheeler D, Timucin M. Kowalski, P. Wysocki, Intelligent Systems Division, NASA Ames Research Center, Aviation Safety Technical Conference 2008.

[3] http://www.commercialventvac.com/fear.html.

[4] ASIC/SOC Functional Design Verification, A Comprehensive Guide To Technologies and Methodologies, Ashok B Mehta, Springer Publications.

[5] Paul W. Brazis Jr, and Fan He, "Effectiveness of Circuit Breakers in Mitigating Parallel Arcing Faults in the Home Run", Underwriters Laboratories Inc, 2011.

[6] Chirag R Sharma, Cynthia Furse, "Low Power CMOS Sensor For Detecting Faults in Aircraft Wiring", A thesis submitted to the Faculty of The University of Utah, 2007.

[7] Shi, Qinghai & Kanoun, Olfa. (2013). A New Algorithm for Wire Fault Location Using Time-Domain Reflectometry. IEEE Sensors Journal. 14. 10.1109/JSEN.2013.2294193.

[8] Cynthia Furse, Senior Member, IEEE, You Chung Chung, Member, IEEE, Rakesh Dangol, Marc Nielsen, Member, IEEE, Glen Mabey, and Raymond Woodward "Frequency Domain Reflectometry for on board testing of aging aircraft wiring", IEEE Transactions on Electromagnetic Compatibility, VOL. 45, NO. 2, MAY 2003.

[9] Chet Lo, Member, IEEE, and Cynthia Furse, Senior Member, IEEE, "Noise Domain Reflectometry for Locating Wiring Faults", IEEE Transactions on Electromagnetic compatibility, VOL. 47, NO. 1, FEBRUARY 2005.

[10] Peijung Tsai, Student Member, Chet Lo, Member, You Chung Chung, Senior Member, and Cynthia Furse, Senior Member, "Mixed Signal Reflectometer for location of faults on Aging Wiring", IEEE Sensors Journal, VOL. 5, NO. 6, DECEMBER 2005.

[11] Chirag R. Sharma, Student Member, IEEE, Cynthia Furse Low-Power STDR CMOS Sensor for Locating Faults in Aging Aircraft Wiring, , IEEE SENSORS JOURNAL, VOL. 7, NO. 1, JANUARY 2007 43.

[12] Paul Smith, Cynthia Furse, "Analysis of Spread Spectrum Time Domain Reflectometry for Wire Fault Location", IEEE SENSORS JOURNAL, VOL. 5, NO. 6, DECEMBER 2005 1469.

[13] Jawad Faiz, H. Nejadi-Koti and Z. Valipour," Comprehensive Review on Inter-Turn Fault Indexes in Permanent Magnet Motors", IET Electric Power Applications, August 2016.

[14] Mohamed H.Hassoun, "Fundamentals of Artificial Neural Networks", The MIT Press, Cambridge, London, England.

[15] MIL-STD 1553 Tutorial (1600100-0028), Condour Engineering, Document Revised on June 5th, 2000, Document Version 3.41, Software Revision 4.0.
https://www.techdesignforums.com/practice/guides/fpga-prototyping/