

**ENHANCED SCINTILLATING TRACKER FOR EVALUATING THE 2ND
GENERATION BOREHOLE MUON DETECTOR AT THE HAWAII MUON
BEAMLINE**

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By
Khanh Le

Thesis Committee:

Gary S. Varner, Chairperson
Victor M. Lubecke
David G. Garmire

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The work it took to take the beginning stages of the 2nd generation Borehole Muon Detector (BMD) from concept to a physical reality has taken countless hours and setbacks. Each step to the most recent version of the BMD utilizes many disciplines: Mechanical, computer, and electrical engineering were integral for the testing structures, firmware, software, and electronics, while physics laid the foundation for the underlying theory of operation. Much of the work wouldn't have been possible without the help of many people. I would like to thank all those who took the time from their busy schedules to help a long the way.

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ABSTRACT

Muon tomography generates three-dimensional volume images from measuring the flux and angular distribution of cosmic ray muons [1]. When comparing the imaging capability to X-rays, muons can penetrate much thicker materials. The muons ability to penetrate deep into materials, like rock and metal, makes muon detectors ideal for subsurface geological feature reconstruction. In the past, muon detectors have been used by Luis Alvarez in an attempt to discover hidden chambers in the Second Pyramid of Chephren in Giza and successfully image the displacement of magma in active volcanoes [2–4]. In the early days of muon tomography, detectors were very large and had very low resolution. Early detectors used large drift tubes and Photo-Multiplier Tubes to measure muon flux attenuation. With advancements in readout electronics and Silicon Photo Multipliers, modern detectors are much smaller in size, have higher resolution, and come at a lower cost.

The Borehole Muon Detector (BMD) project intends to greatly reduce the size, power expenditure, and operational cost of current muon detection technology [5]. Muon detection starts when a muon passes through the detector's scintillating planes, exciting scintillating materials, and resulting in a flash of light. The flash of light, consisting of only a few dozen photons, is then measured in units of photoelectrons, is then converted to an electrical pulse by photosensors and saved in the TARGETX ASIC. Information from the TARGETX is read out using a Spartan 6 FPGA and sent back to the PC via standard fiber optic Ethernet link for analysis and reconstruction. When fully realized, the BMD will be approximately 1 m long with a diameter of 15.24 cm (6 in). The full detector encloses all readout electronics, scintillating planes, and an integrated Thermo-Electric Cooler. The design is intended for deployment in subsurface boreholes with diameters greater than 17.78 cm (7 in), up to a depth of 914 m (3000 ft) [5], and has the capability to collect data for long periods of time.

This document focuses on the design of the 2nd generation center daughter cards, development of the readout firmware and software, and construction of the tracker planes to be used in the Hawai'i Muon Beamline. The initial results from calibration, pedestal subtraction, sine wave reconstruction, LED pulsar test, and RC gain circuit evaluation of the 2nd generation BMD center daughter cards are also included.

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CHAPTER 1

INTRODUCTION

When comparing the imaging capability to X-rays, muons can penetrate much thicker materials, making muon detectors ideal for determining density distributions of materials in the earth's subsurface. Most atmospheric muons are the result of the interaction between cosmic rays and the outer edge of the earth's atmosphere. The result of these interactions are showers of various High Energy Particles (HEP) that are sent towards the earth surface (ref. Fig. 1.1). Muons, having a lifetime of $2.2 \mu\text{s}$ and a small cross section for interactions, enable the particle to travel long distances and penetrate dense materials before decaying. The muons ability to penetrate deep into materials like rock and metal makes muon detectors ideal for subsurface geological feature reconstruction.

Muon Tomography is a technique that uses naturally occurring muons to image the interior of large-scale geological structures. This variation of proton radiography was first developed in the mid-1990s by the Los Alamos National Laboratory [1]. In these early days of muon tomography, detectors were very large and had very low resolution. The early detectors used large drift tubes and Photo-Multiplier Tubes (PMT) to measure muon flux attenuation. With advancements in readout electronics and the miniaturization of Silicon PhotoMultipliers (SiPM), modern detectors are smaller in size, have higher resolution, and come at a lower cost.

Recent developments and applications of muon tomography have been made by Luis Alvarez in an attempt to discover hidden chambers in the Second Pyramid of Chephren in Giza and successfully image the displacement of magma in active volcanoes [2–4]. Luis Alvarez's experiment resulted in the discovery two possible new chambers in the pyramid. His research brought much attention to the usefulness of cosmic-ray muon attenuation radiography and later became muon tomography. Other areas of application for muon tomography are field-scale displacement of reservoir fluid induced by injection or production of liquids or gases. This technique could enable detection of geological carbon storage, natural gas storage, compressed air storage, enhanced oil recovery, aquifer storage and recovery, waste water storage, and oil and gas production.

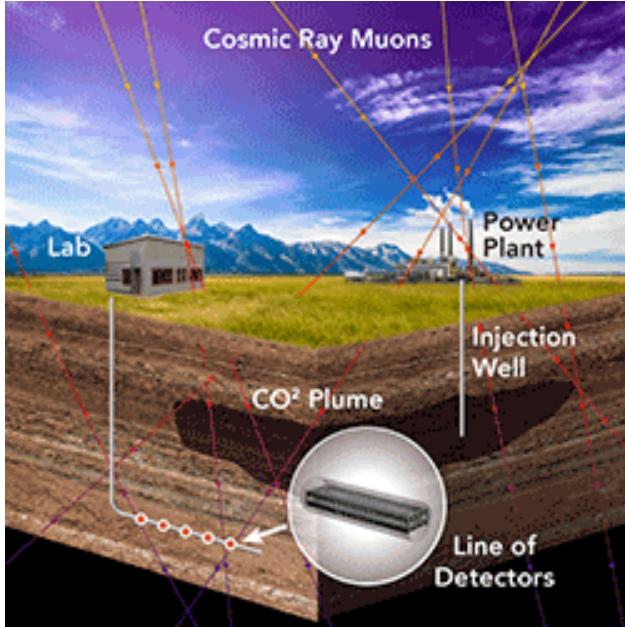


Figure 1.1: In this illustration a series of five BMD are deployed in a horizontail well below a CO₂ reservoir [7]

1.1 Borehole Muon Detector (BMD)

The Borehole Muon Detector (BMD) intends to greatly reduce the size, power expenditure, and operational cost of current muon detection technology [5]. The 1st Gen BMD was a joint venture between U.S. DOE crosscut program SubTER, Pacific Northwest National Laboratory (PNNL), the Lawrence Livermore National Laboratory, Los Alamos National Laboratory (LANL), Sandia National Laboratory, University of Utah, University of Hawai'i, and Paulsson Inc. The readout electronics, readout firmware, and software were developed at the Instrumentation Development Laboratory (IDLab) at the University of Hawai'i at Manoa (UHM). The BMD was then deployed in a shallow, underground, laboratory at PNNL and in a underground tunnel at LANL.

The BMD detects, records, and saves the light produced by HEPs, such as muons, as it passes through the detector. Detection starts when a muon passes through the detector's scintillating planes, exciting scintillating materials, and resulting in a flash of light. The flash of light is then converted to an electrical pulse by arrays of SiPM, which is then sampled and saved in the memory of the Application Specific Integrated Circuits (ASIC). Information from the ASIC is readout using the Spartan 6 Field Programmable Gate Array (FPGA) and sent back to the PC via standard fiber optic Ethernet link for analysis and reconstruction. The design is intended for borehole deployment for a depth of up to 914 m (3000 ft) [5], and has the capability to collect data for long periods of time.

The 1st Gen BMD used scintillating planes based on scintillating rods with embedded Wave-length Shifting Fibers (WSF), along with Hamamatsu Multi-Pixel Photon Counter (MPPC), and 10 TARGETX ASICs that were developed in the IDLab at the UHM [5]. It was a proof of concept that muon detectors can be developed to be compact and low power, setting the foundation for future generations.

The 2nd generation BMD, or the “Next Gen” endeavors to meet the next milestone in the BMD project. The Next Gen BMD seeks to reconstruct detector components such that the fully visualized detector, includes all readout electronics and scintillating planes, and will be cylindrical in shape with an approximate diameter of 15.24 cm (6 in). Figure 1.2 shows a 3D rendering of the purposed final shape of the Next Gen BMD. In the figure, the center Daughter Card (DC) is highlighted in blue and the scintillating planes are left out to exhibit the electronics. The Next Gen BMD is made up of three different Printed Circuit Boards (PCB): the center DC, the end-cap DC, and the interface board. The center and end-cap DCs will share the same circuitry, with the exception that the end-cap DC is equivalent to two center DCs. The interface board will house the SCROD, Thermo-Electric Cooling (TEC) system, and the fist power distribution stage.

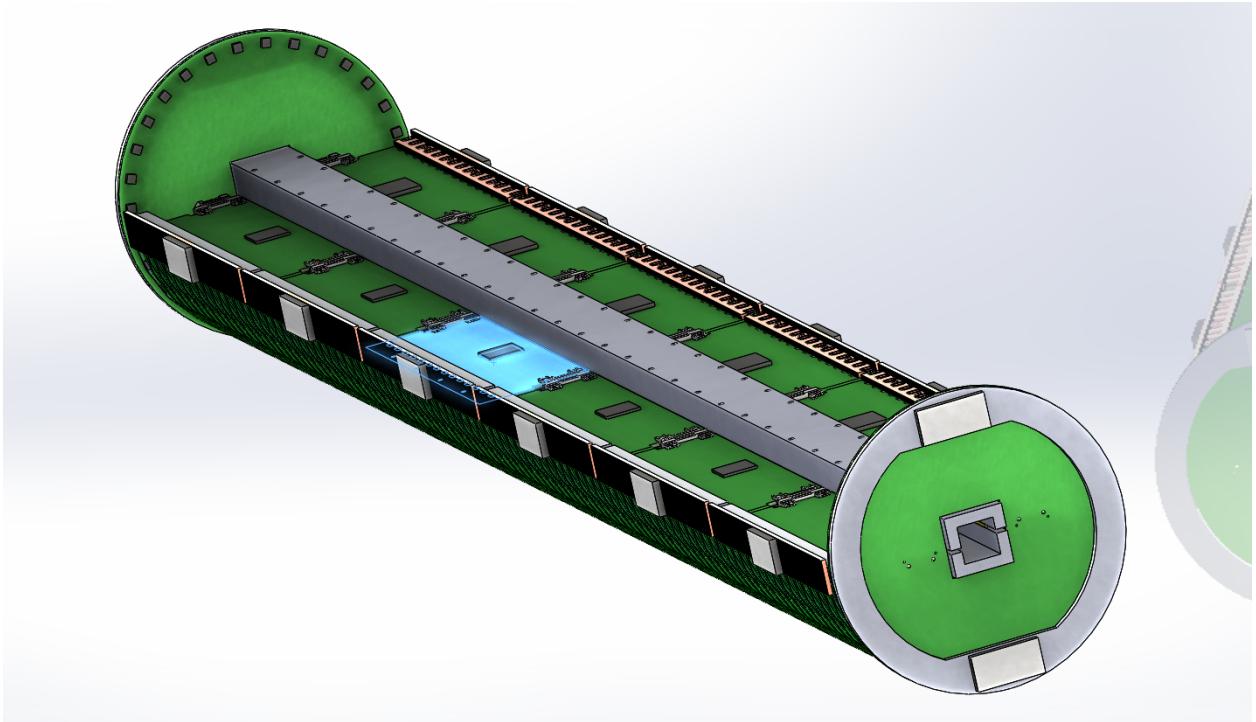


Figure 1.2: 3D rendering of final BMD without scintillating planes designed by Julien Cercillieux.

The Next Gen BMD center DC is the first of a series of new readout electronics designed to be high speed, mixed signal, low power, enabling the Next Gen BMD to be scalable. In order to achieve these goals, design and development of the Next Gen BMD prototype DC began with redesigning the BMD DCs to combine the readout electronics and MPPC sensors on to the same PCB. Along with the consolidation, the interface between the DCs and the Standard Controls and Read Out Device (SCROD) have also changed; such that the DCs are now linked together in a serial chain with the SCROD, acting as the master unit at the top of the chain. By combining the readout electronics and MPPC sensors, and changing the interface between SCROD and DCs, the need for long CAT5 cables, the large motherboard, and the interface boards were eliminated.

1.2 Hawai'i Muon Beamline (HMB)

The Hawai'i Muon Beamline was initially constructed by James Bynes with the help of Marissa Kuwabara and Zj Lin for his graduate thesis studies in the IDLab at UHM. The HMB allows for verification of detectors which are still in the development stages. It consists of three different detectors: the Momentum Spectrometer, Sodium Iodide (NaI) Calorimeter, and two tracker planes that make up the total system. As a HEP, passes through the HMB, the three detectors comprising the HMB will sample, save, and digitize the event. These events are then used to verify the performance of the device under test while placed at the center of the HMB (ref. Fig.1.3).

The HMB from the bottom up, is comprised of the momentum spectrometer, the NaI Calorimeter, and the tracker planes. The momentum spectrometer, consisting of two sets of Dual-sided Silicon Strip detectors (DSSD) above and below a 0.5 T permanent magnet, curving the trajectory of a particle as it passes through the magnet. The change in trajectory is then measured by the DSSD, and the resulting radius of the curved path is related to the momentum of the particle. The NaI Calorimeter, is made up of 4 NaI scintillation detectors placed at the base of the tracker plane tower inside a light tight enclosure. The NaI calorimeter will act as a incident angle cross reference between the top and bottom tracker planes, as well as collect any additional information on the incident muon as it passes through the HMB.

The final detector in the HMB are the tracker planes. The tracker planes are comprised of 4 scintillating planes. Each scintillating plane has Wavelength Shifting Fibers (WSF) embedded into the top and bottom surfaces in a orthogonal pattern making a X and Y coordinate grid for one detector plane. The readout electronics and sensors of the tracker planes are made up of a SCROD and 4 Next Gen center DCs. The data collected from both planes can be used to reconstruct the muon positioning and angle of incidence. As well as estimating muon flux density over a given angular region by observing many individual events.

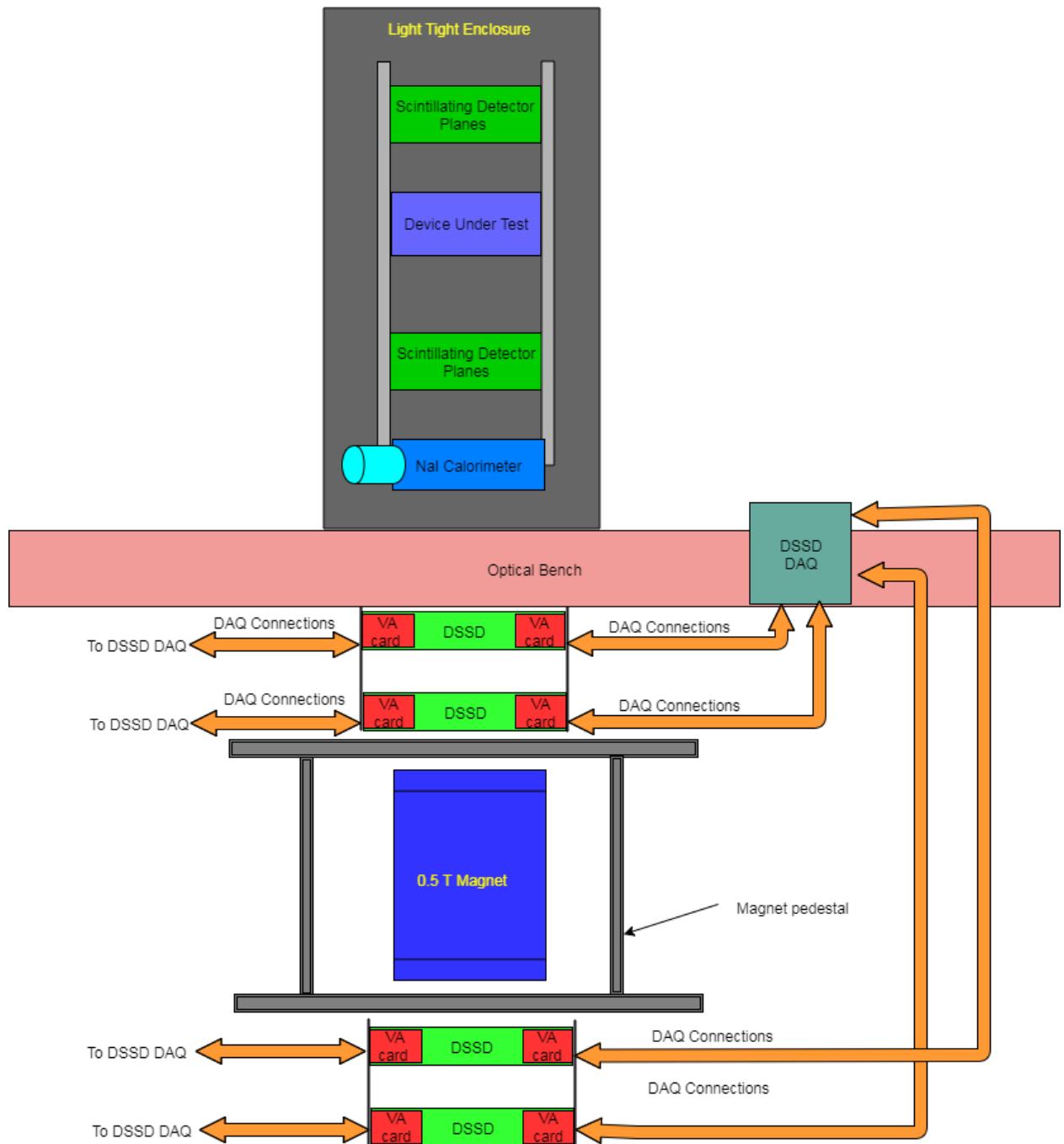


Figure 1.3: Block Diagram of the full HMB system to include the Momentum Spectrometer, NaI Calorimeter, and two tracker planes designed by James Bynes.

1.3 Research Objective

This report introduces the 2nd Generation BMD while focusing on the development of the 2nd Gen center DCs. The report also compares the major differences between the 1st Gen and the 2nd Gen electronics. Daughter card development consists of four major stages: Readout electronic design, mechanical design, data acquisition firmware, and software development. In the following chapters a brief summary of the 1st Gen results will be followed by a detailed description of the 2nd Gen BMD, adaptation of the 2nd Gen center DC to be used as the electronics for the tracker planes in the HMB, and finally the initial readout results of the 2nd Gen BMD center DCs.

The BMD is an ongoing project that will require many milestones to be met before its full completion. For the purposes of this paper, the Next Gen BMD will be in stage one of prototyping. By the end of this stage the center DC, tracker scintillating plate, and tacker housing will be fabricated and assembled along with first versions of the readout firmware and software. The first versions of the firmware and software will include the following features detector calibration scripts, TARGETX readout, pedestal subtraction, event trigger system, and proprietary communication link.

CHAPTER 2

1ST GENERATION BMD

The 1st Gen BMD utilizes 1 cm square polystyrene scintillator rods coated with TiO₂ reflector (provided by Fermi National Laboratory). Each rod includes a 2 mm diameter wavelength shifting fiber from Saint Gobain (Hiram, OH) glued in the center of the rod. The rods then lead to a SiPM to pick up the scintillation light generated by muon transit. Placing the rods in an alternating orthogonal pattern from top to bottom creates a detector layer with an internal coordinate system; using two of these layers, the incident angle of the muon can be later calculated.

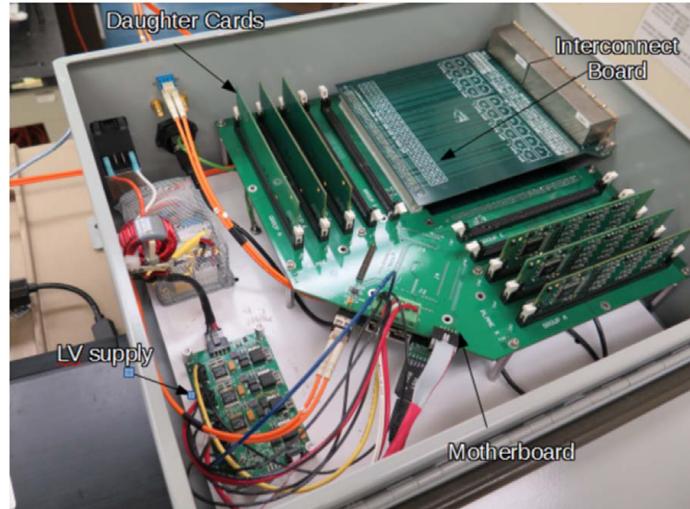
The rods that make up the top layers are 68 cm long while the rods that make up the bottom layers are 15 cm. Fully populated, each top layer is comprised of 15 rods, with the bottom 30 rods centered on the two layers. There are a total of 90 rods. The fully assembled 1st Gen BMD planes are 15 cm wide, 68 cm long, and 8 cm high (ref. Fig.2.1).



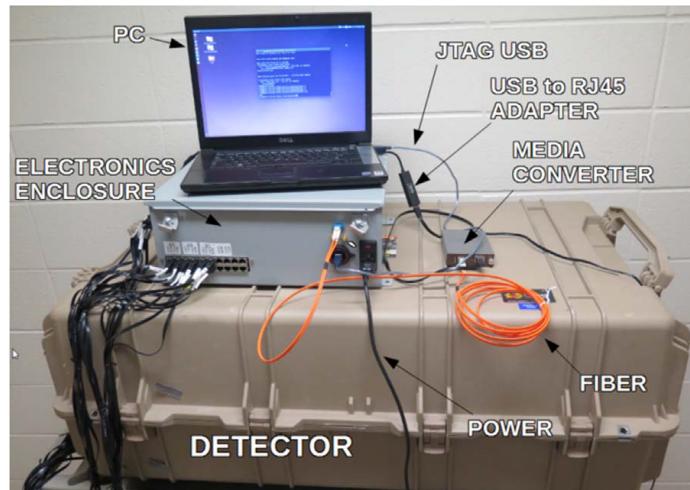
Figure 2.1: Prototype assembly of 1st generation BMD showing rows of scintillating rods [5].

The 1st Gen prototype has the capability to utilize up to 10 TARGETX ASICs. Each TARGETX ASIC contains 15 data-taking channels and a calibration/testing channel. Each data-taking channel also has dedicated SiPMs from Hamamatsu MPPC (S12572-050) and trim DACs for fine HV bias tuning. A DC-to-DC booster from EMCO (SIP 90) provides the course HV bias that is

common for all channels. The Spartan 6 LX150T FPGA on the SCROD handles all of the timing, clock distributions, readout, and TARGETX operations for the detector. FPGA programming uses JTAG protocol, the SCROD transmitted data via standard fiber-optic Ethernet link to a PC. The assembled 1st Gen electronics includes an interconnect board, motherboard, low voltage power supply, and digitizer daughter cards (ref. Fig.2.2).



(a)



(b)

Figure 2.2: (a) Prototype electronics assembly of 1st Gen BMD and (b) complete data acquisition system. Labeled in the box is [5].

2.1 PNNL data Results

During testing at PNNL, the BMD was tested above ground, approximately 100 m above sea level, and underground, approximately 35 m-water-equivalent deep. Projecting the histogram of the data onto a plane 30 m above the BMD is useful in approximating spatial density variations (ref. Fig.2.3). Assuming that the muon spectrum's were uniform in intensity the plot from the above ground test (ref. Fig.2.3a) would be homogeneous, showing no muon intensity pass the detectors maximum acceptance angle. Because cosmic muon spectrum strongly favors vertical muon flux, all projection plots exhibit the same intensity pattern (ref. Fig.2.3).

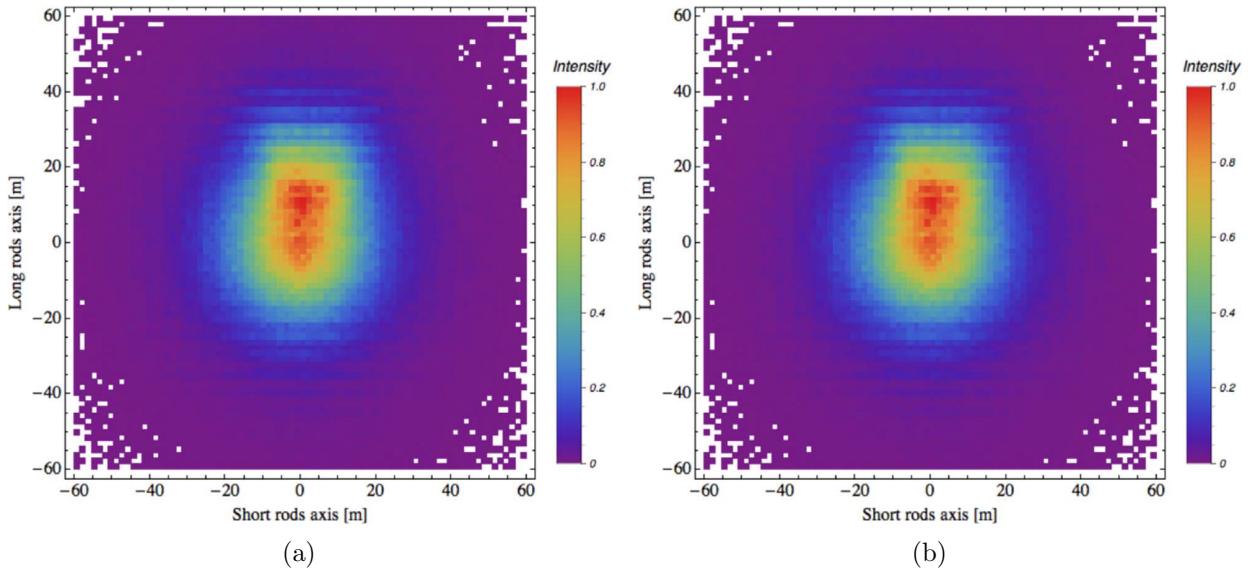


Figure 2.3: (a) Histogram of about 128k event from above ground test at PNNL and (b) 560k events from the underground test. Data is projected onto a plane 30 m above the BMD, each bin is categorized with respect to muon flux intensity [5].

In the underground test, the BMD was placed near a stairway to allow for variations in muon flux, depending on the angle. During the span of the test, the BMD took 57 data sets equating to 560,000 events; the average event rate was 1 event per second [5]. Due to the presence of the stairway, the underground test data also seems to display a somewhat broader total angular distribution (ref. Fig.2.4). It is suggested the projection of muon flux is asymmetric due to the difference in overburden of the stairway and the overburden of the fill material above the tunnel. This observation may also correspond to the angular muon flux simulation models done prior to BMD deployment. The plots suggest a clear increase in muon flux on the side of the BMD that was facing the stairway (ref. Fig.2.4).

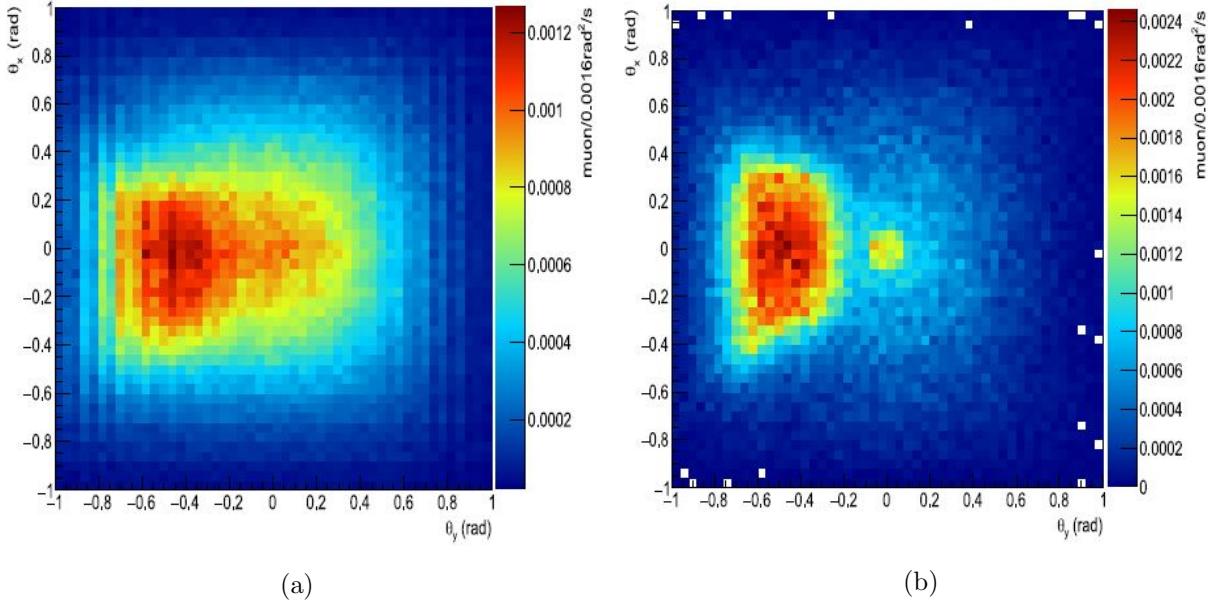


Figure 2.4: (a) The data taken at the underground laboratory and (b) the comparison of the simulated angular muon flux. Data was obtained at PNNL underground laboratory. Stairway data is on the left [5].

2.2 LANL data Results

LANL testing was performed in the laboratory building and in various locations in the TA41 tunnel (ref. Table 2.1). As a comparison, a reference detector named the Mini Muon Tracker (MMT) was also used in the same locations as the BMD. The MMT uses 12 layers of drift tubes and has a detection area about 1.2 m^2 [5]. Since the MMT has a much greater detection area, approximately 32 times that of the BMD, the event rate of the BMD and MMT ranged from 11:1 to 14:1 [5] depending on location. Differences in the active detector area and event rates the MMT yielded a resolution higher muon flux density than the flux density of the BMD. The MMT data was normalized by a factor of 15 so that its data can be directly comparable to that of the BMD (ref. Fig. 2.5). Each plot in Figure 2.5 shows the projection of the muon track on a plane 100 m above the detector surface.

Table 2.1: BMD result from tunnel TA41 at LANL by tunnel location relative to the doorway [5].

Distance Form Door (m)	Position In Tunnel	Approx. Depth (m)	Estimated Count Rate (Hz)	Measured Count Rate (Hz)	Measured Time (days)	Total Events Obtained
Lab Room C101	N/A	0	10	9.8	1	128k
-1.7	Outside	0	9.0	8.0	1	87k
10	3	14	2.8	3.2	1.5	179k
35	2	40	0.8	0.88	4	339k
62	0	59	0.2	0.30	16	401k
78	0	74	0.14	0.19	20	240k

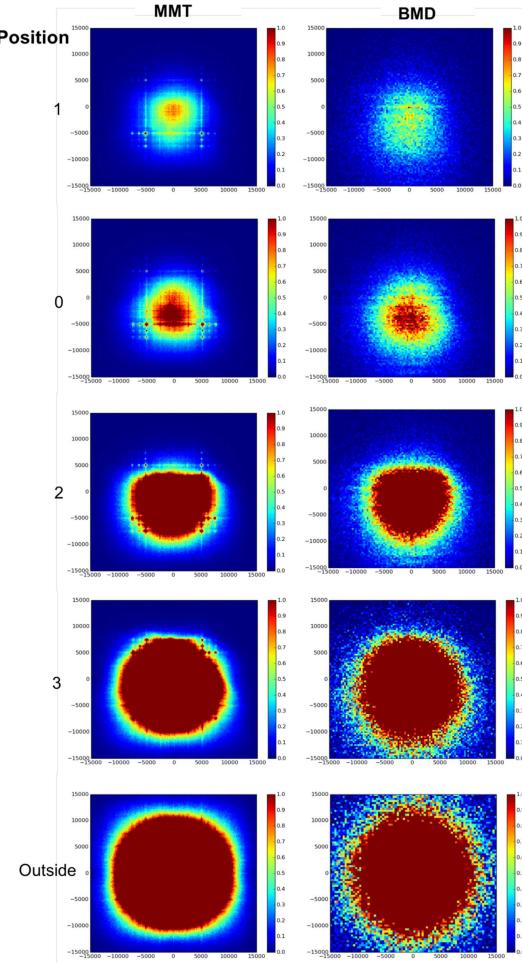


Figure 2.5: Comparison of BMD data versus MMT measured at 5 locations in the TA41 tunnel at LANL [5].

2.3 Next Generation BMD

The Next Gen BMD inherited the potential to provide a sensitive, cost-effective, and precise monitoring technique from the 1st Gen predecessor. The objective for the Next Gen, however, is to redesign the overall shape of the system to allow all of the electronics, scintillator planes, and power distribution components to be enclosed in a cylinder with dimensions approximately 15.24 cm (6 in) by 1 m long. In order to achieve this goal, the readout electronics of the BMD needed to be redesigned. The reconstruction of the readout electronics started with the integration of readout electronics and MPPC sensors onto the same PCB. The integration of the readout electronics and the MPPC sensors eliminated the need for large amounts of CAT5 cables (ref. Fig.2.6a) and interface boards (ref. Fig. 2.2a) used in the previous version to connect the MPPC sensors to the TARGETX ASIC. Along with the integration, the interface between the SCROD and DCs was also changed, linking the Next Gen DCs in a serial chain with the SCROD at the top of the chain as the master unit. With the change in interface, it was possible to eliminate the large motherboard (ref. Fig.2.2a), enabling all of the readout electronics to fit inside the cylindrical shape of the Next Gen BMD. Figure 2.6 shows the comparison between the two generations of BMD.

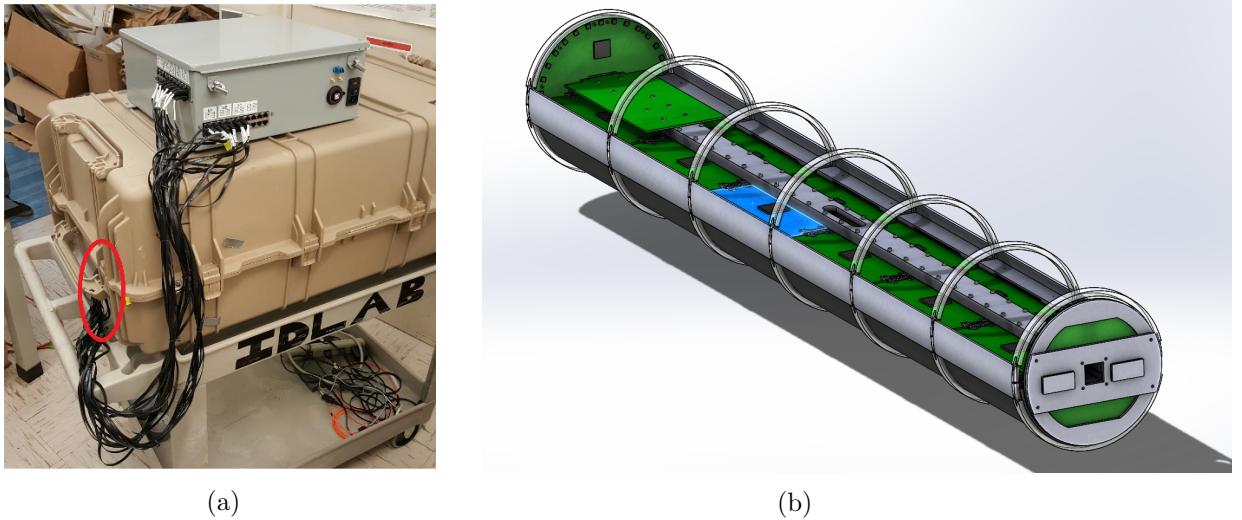


Figure 2.6: (a) 1st Gen BMD showing CAT5 cables connecting readout electronics and MPPC sensors on detector planes inside of light tight case and (b) Cad model of 2nd generation BMD not including the scintillating planes designed by Julien Cercillieux.

The Next Gen BMD readout electronics is made up of three different PCBs (ref. Fig.2.6b): the center DC highlighted in blue, the round end-cap DC at each end, and the interface board at the center of the detector. The center DC and the end-cap DC uses similar schematics, with the exception that the end-cap cards hold two sets of readout electronics. The interface board houses the SCROD, TEC system and the first power distribution stage. With the interface change between

the SCROD and the DCs, new firmware and software was also developed. The new firmware and software enabled readout of the ASICS and command supporting Integrated Circuits (IC) on each DC, serial communication for the detector, and the triggering protocol.

The final BMD scintillator plane consists of two individual semi-circular planes which form a hollow cylinder, approximately 1 m long, 15.24 cm in diameter, and 1 cm thick (ref. Fig.2.7). To accommodate the cylindrical shape, the new planes will be cut from a large piece of Polyvinyl Toluene (PVT) scintillating material and have single-clad round 2 mm WSF provided by Saint-Gobain epoxied into grooves along the inner surface and across the outer surface of the plane. Embedding the WSF along the interior and across the exterior creates the grid pattern needed for muon reconstruction. Unlike the planes from the previous generation, the Next Gens planes exhibit light sharing since it does not have the reflective shielding that covered the scintillating rods used in the last revision. During a muon event, light sharing could cause multiple channels to trigger or cause multiple channels to record the same muon event; this will make it difficult to determine the triggering MPPC. The intrinsic properties of the PVT material causes light generated by the muon event to dissipate as it travels away from the source. Like a ripple, the dissipation will make the muon pulse of the MPPC channel closest to the point of intersection the largest. Pulse strength is then determined by taking the integral of the muon pluses on each channel. Comparing the pulse strength of each MPPC channels with the TARGETX trigger bits at the time of trigger the effects of light sharing can be overcome. Due to the difficulty in fabricating the Next Gen detector planes, the Next Gen center DCs were be reconfigured to be used as the readout electronics for the tracking planes in the HMB. Using the Next Gen DC as the readout electronics for the tracker planes, provides an opportunity to test the Next Gen DCs, firmware, and software.

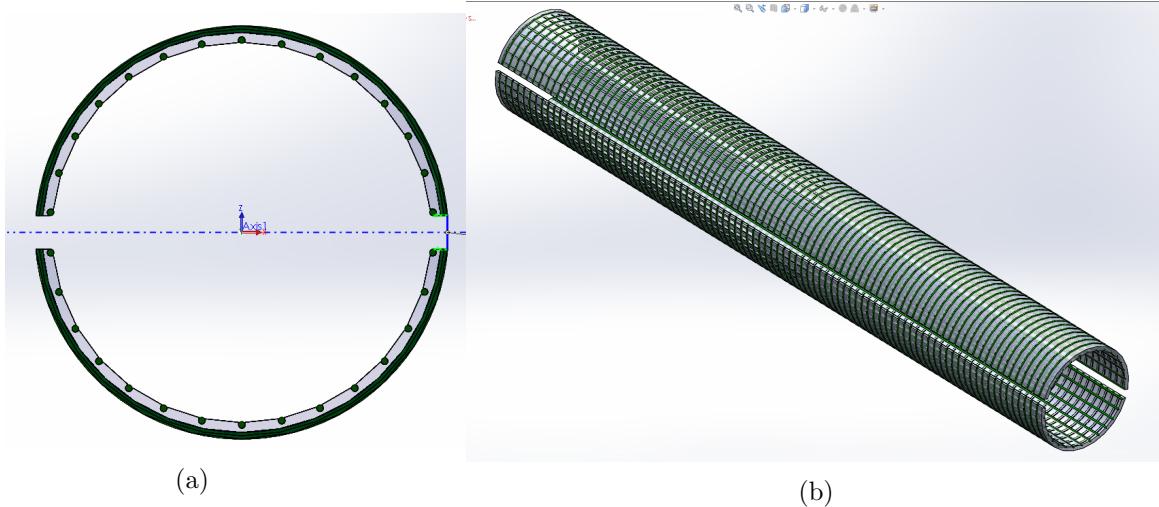


Figure 2.7: (a)Cross section and (b)side view of purposed final BMD scintillator planes with wavelength shifting fibers epoxied to planes designed by Julien Cercillieux

CHAPTER 3

TRACKER CONSTRUCTION “THE ENTERPRISE”

The HMB tracker planes, nicknamed “The Enterprise”, is a set of 4 scintillating detector planes that is used to capture the positioning of a particle as it travels through the HMB. The data from the planes will be used as a reference for detectors that are still in prototyping stages. Each tracker plane consists of 2 Next Gen BMD center DCs; while each pair of planes are readout and controlled by a SCROD. The scintillating detector planes are made of the same PVT material, but with embedded WSF as the planes for the BMD. By building The Enterprise, future studies can be done to determine the optimal plane thickness that will yield maximum light with minimum amount of light sharing between channels. The final thickness of the scintillating planes for the BMD can be determined from this study. The Enterprise also allows for the debugging the new firmware and software, evaluating the RC gain circuit (Fig.3.8), and gaining better insight on the performance of the PVT material with the 2 mm WSF epoxied into the planes. The fully assembled tracker plane houses a SCROD, 4 Next Gen BMD DC, and two scintillating planes (ref. Fig.3.1).

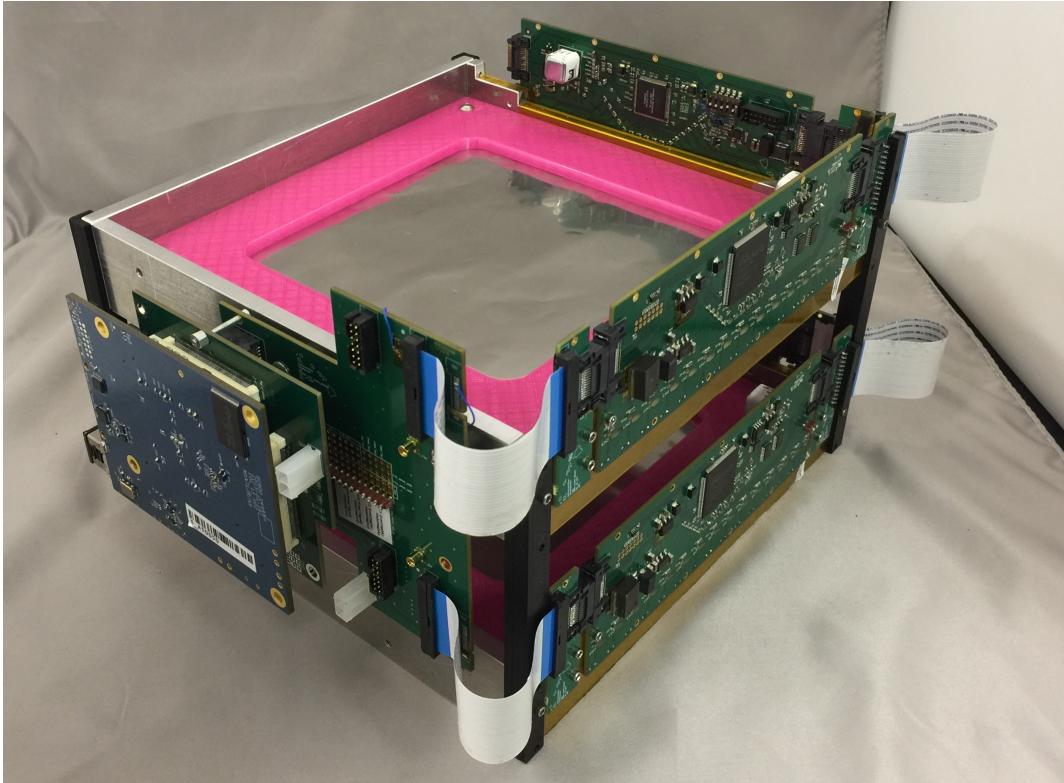


Figure 3.1: Fully assembled tracker plane, with sheets of stainless steel covering the scintillating planes to improve light yield .

3.1 Tracker Housing

The HMB tracker housing consists of 3 major components: the frame (ref. Fig. 3.2), cover plates (ref. Fig.3.1, in pink), and the standoff legs (ref. Fig.3.1, in black). All components of the tracker housing, with the scintillating planes were designed and fabricated in the machine shop and IDLab at the UHM. The frame of the tracker was designed to house 2 Next Gen DC and one scintillating plane. It features slots on the interior of frame allowing for 0.5 mm compression of optical cookie when installed with the scintillating plane. It also has precision slots milled out to align each WSF on the scintillating planes to the center of the MPPC sensor. Figure 3.2 shows an empty frame showing the slot for the scintillating plane and the alignment slots cut for the MPPC sensors.

Cover plates were 3D printed to hold stainless steel sheets that covered the top and bottom of each plane. The stainless steel sheets were added to reflect any light produced by passing HEP to increase the efficiency of each event. To mate the top and bottom frames together, standoff legs were also 3D printed and added such that the center of the scintillating planes are spaced 10 cm apart. Using this distance and the approximate location at which the particle intersected the scintillating planes will enable reconstruction of the path of the particle.

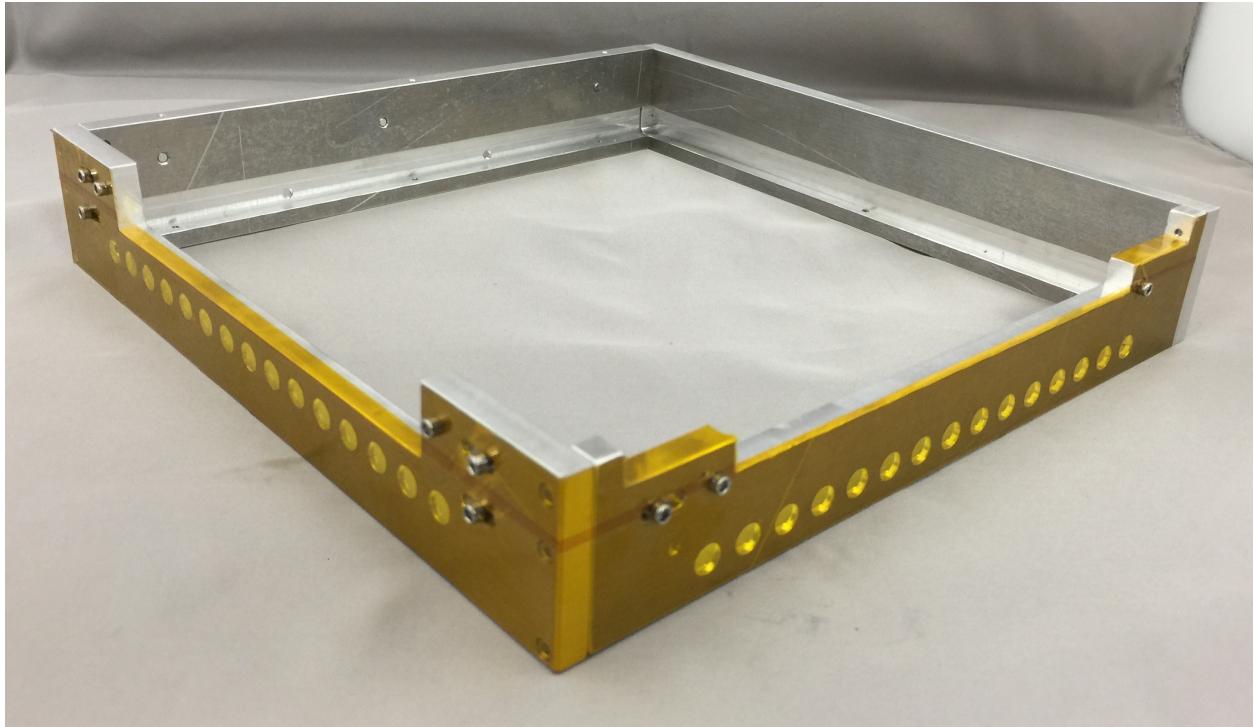


Figure 3.2: Empty tracker frame showing slots for the scintillating plane and MPPC sensors.

3.2 Scintillating Detector Planes

The scintillating detector planes used in The Enterprise house 30, round, single-clad, 2 mm, WSF (15 top and 15 bottom) provided by Saint-Gobain (ref. Fig.3.3). The WSFs are embedded in an orthogonal pattern on the top and bottom of the plane to make up the X and Y axis. By using WSFs the wavelength of the light generated by the PVT material is shifted to approximately 494 nm [9]. 494 nm is approximately the peak sensitivity wavelength of the Hamamatsu SI0362-13-050C MPPC (440 nm [8]). Constructing the planes started with a large piece of PVT material. Using a subtractive process the PVT material was milled down to a plate 30 cm wide by 30 cm long. The first of the scintillating planes starts with a thickness of 1 cm and will be changed in later studies to find the optimal thickness.

During the milling process, 30, 2 mm, grooves with a pitch of 1 cm centered in the middle of the plane was milled using a Radius Cutter End Mill. Using a Radius Cutter End Mill allows for the rounded fiber to sit in the grooves tightly, producing a superior contact with the PVT material. To embed the WSF into the plane, optical epoxy with a transmittance value greater than 98 percent [10] was used. After a curing period of 24 hours, the planes were then milled to the final dimensions of 20 cm by 20 cm.

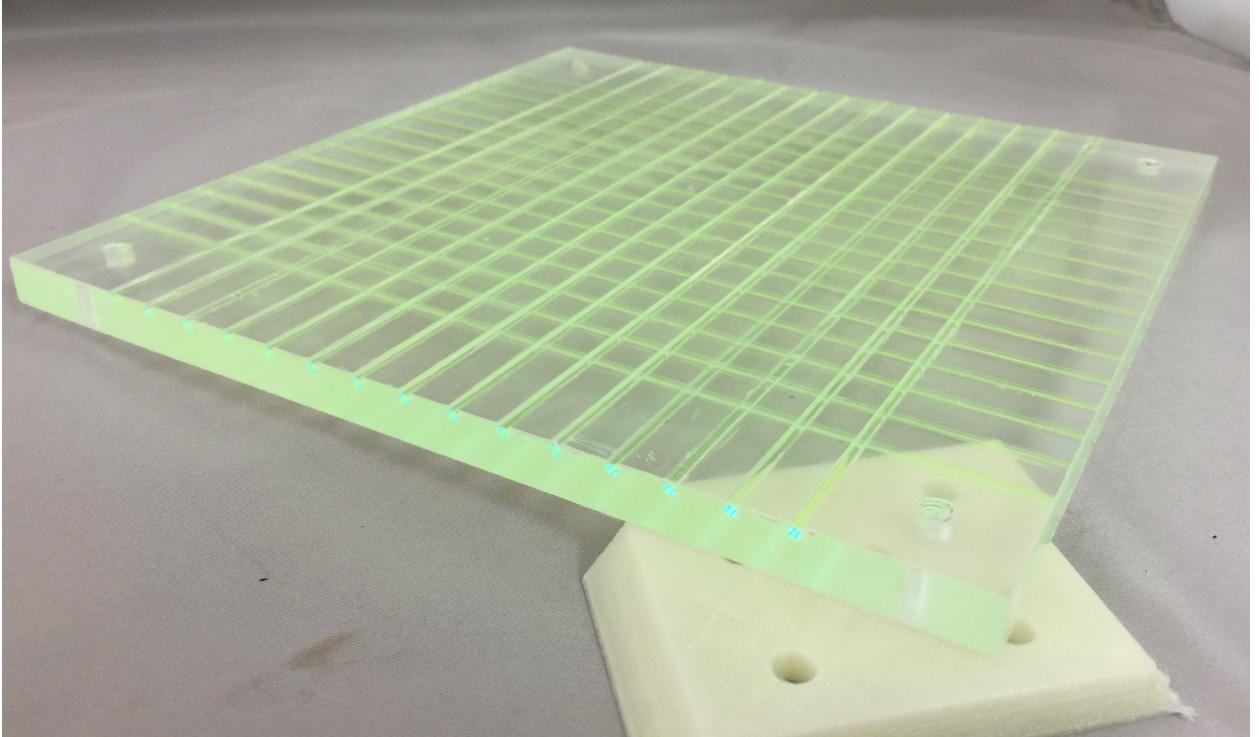


Figure 3.3: Photograph of the scintillating plane used for the tracker in the HMB.

3.3 Hamamatsu MPPC

The Hamamatsu, Multi-Pixel Photon Counter (MPPC) is a silicon photomultiplier made up of many silicon PN junctions. Unlike conventional vacuum photomultipliers tubes, the MPPC is a small solid state device grown on monolithic silicon crystals capable of detecting single photon intensity. The MPPCs are designed to operate in Geiger-mode, which uses avalanche effects in the PN junctions to produce a gain to increase the magnitude of the original photoelectric signal. The amount of gain is proportional to the over-voltage seen at the junction of the MPPC. If biased, correctly the MPPC can achieve gains on the order of several 100k, making the MPPC capable of detecting single photon events.

Traditionally, the output current from the MPPC is converted to an electrical pulse using Operational Amplifiers (OpAmp). But for the purposes of the BMD and tracker planes, the current from the MPPC will be converted using the RC gain circuit (ref. Fig.3.8). Although the Next Gen DCs can house many variations of the MPPCs, the Hamamatsu SI0362-13-050C MPPC (ref. Fig.3.4a) could be quickly implemented and was used for initial testing. The Hamamatsu SI0362-13-050C MPPC is an array of 667 pixels connected in parallel. Each pixel is $50\text{ }\mu\text{m}$ by $50\text{ }\mu\text{m}$ in size, and arranged in a 26 by 26 pixel array (ref. Fig.3.4b) [8]. It's spectral response is in-between 300 nm and 900 nm and peaks at 500 nm [8]. In the BMD and the tracker planes the HV bias for the MPPCs are provided by Advance Energy's UltraVolt XS series (coarse HV adjustments) and Analog Devices AD5391BSTZ-3 DACs (fine HV adjustments).

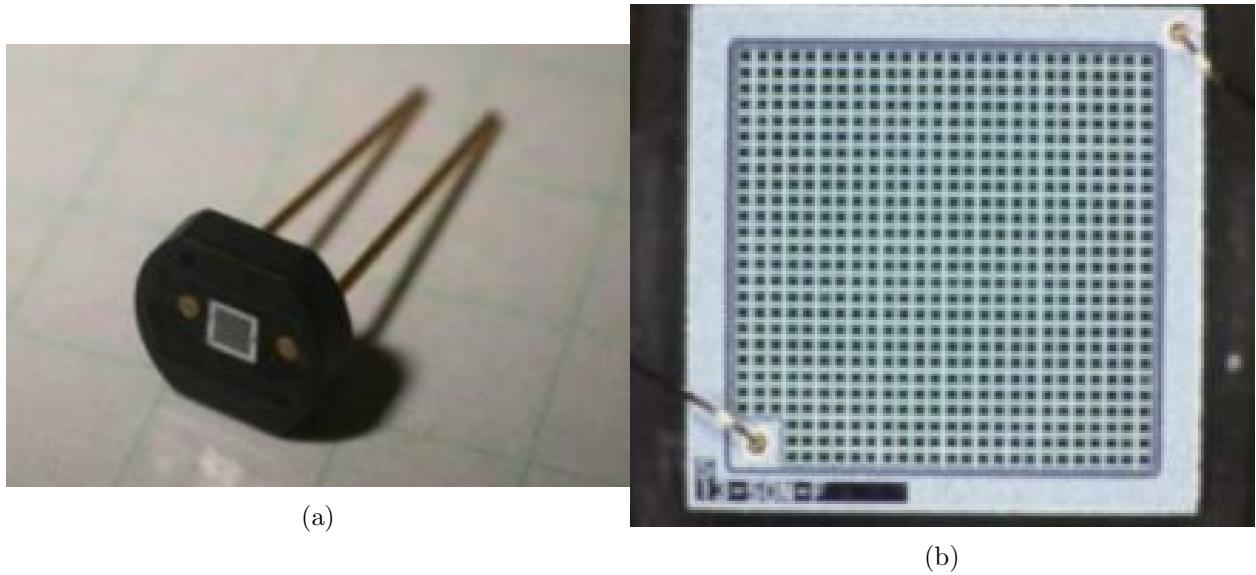


Figure 3.4: (a)Photograph of Hamamatsu SI0362-13-050C MPPC and (b) close up of 26 by 26 counter array.

3.4 Daughter Card (DC) Design

Many features from the 1st Gen DCs were modified or eliminated to fit the detector into a 17.78 cm (7 in) borehole. This section will give a detailed description of the major differences between the 1st Gen DC and the Next Gen DC.

The large amounts of CAT5 cables used to connect the MPPC sensors to the TARGETX ASIC in 1st Gen (ref. Fig.2.6a) needed to be eliminated from the design. CAT5 cable elimination was achieved by merging the TARGETX ASIC, Spartan 6 LX9 FPGA, SRAM memory, FLASH memory, temperature sensor, trim DACs, and HV supply with the MPPC sensors on to one PCB. In merging, special care was taken to isolate heat produced by the readout electronics from the MPPCs. To minimize heat transfer between readout electronics and the MPPCs, perforated holes were placed between the readout electronics and the MPPCs, along with electronically isolating the internal copper planes of the MPPC and area containing the readout electronics. From the heat simulation results done by Julien Cercillieux, it is suggested that the majority of the heat is kept away from the MPPCs with the isolation features (ref. Fig.3.5).

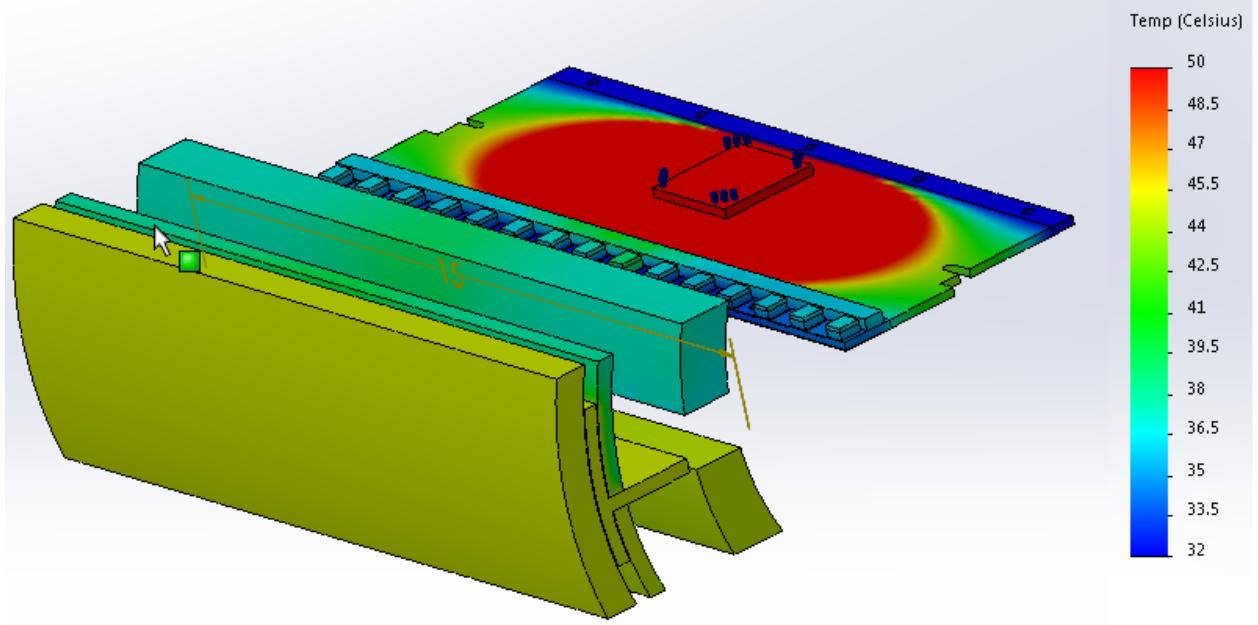


Figure 3.5: Thermal simulation done on Solidworks, show the thermal gradient of the 2nd generation BMD DC done by Julien Cercillieux.

In the 1st Gen BMD, all DCs were connected to the SCROD directly. The direct connection enabled commands to be issued directly to each ASIC, keeping the communication time to a minimum, but direct connection to each DC made the motherboard too large for placement inside the 17.78 cm borehole (ref. Fig.2.2). For the Next Gen readout electronics to fit in the cylindrical

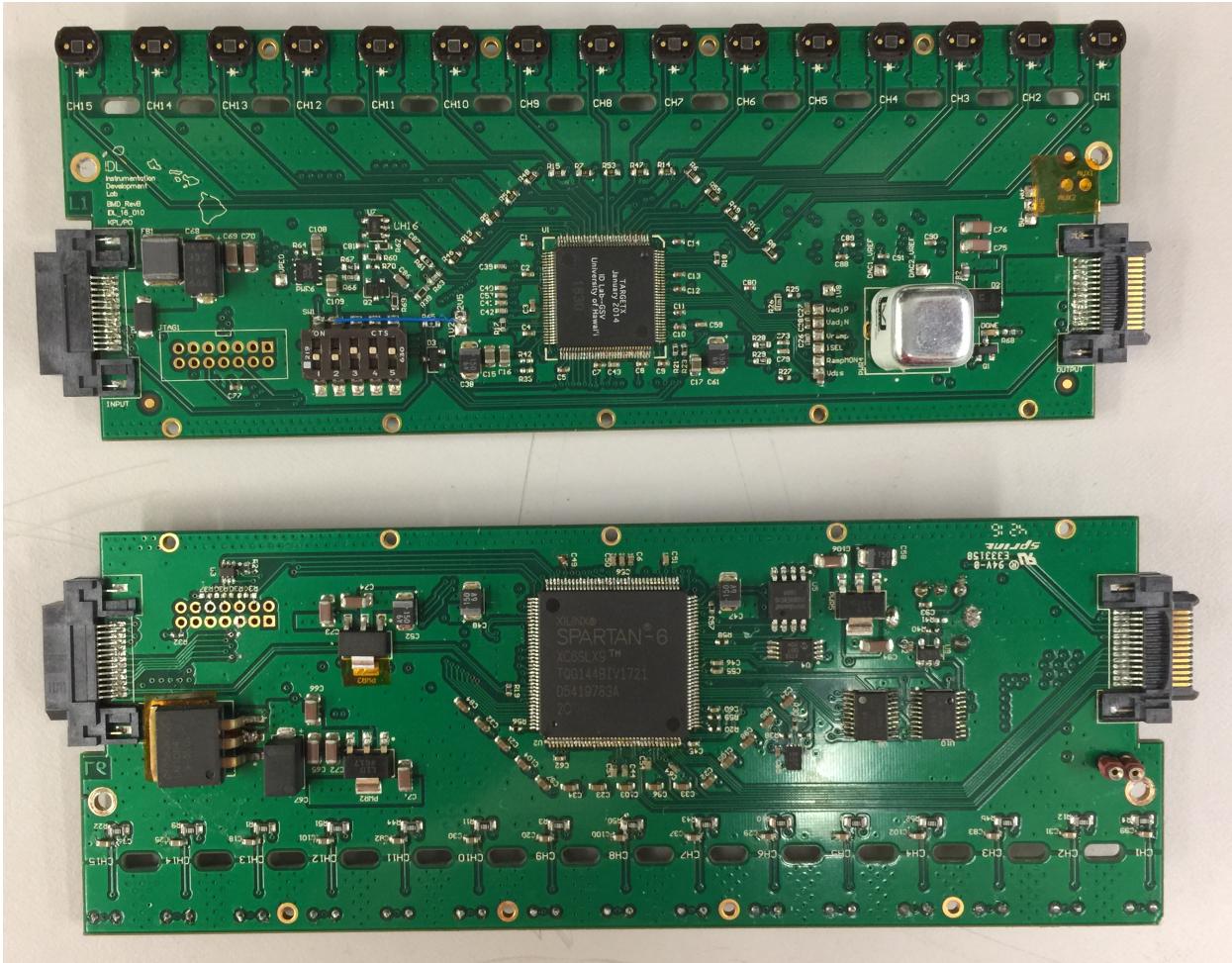


Figure 3.6: Photograph of top (top) and bottom (bottom) of fully populated 2nd gen BMD center DC.

shape, DCs were placed in series. Each card contains a settable hardware address that is used as the DC identification number. Placing DC's in series lengthened communication time, but was a reasonable trade-off against the elimination of the CAT5 cables.

Placing the DCs in series eliminated direct communication between the SCROD and each ASIC, limited DC size, and reduced pin availability. Subsequently, in the Next Gen DCs each DC has a dedicated set of readout electronics to include the following: Spartan 6 LX9 FPGA, Flash memory, SRAM memory, Temperature sensor, 16 12-bit DACS, HV module, and the TARGETX ASIC (ref. Fig.3.7). A photograph of the fully assembled Next Gen DC can be seen in Figure 3.6.

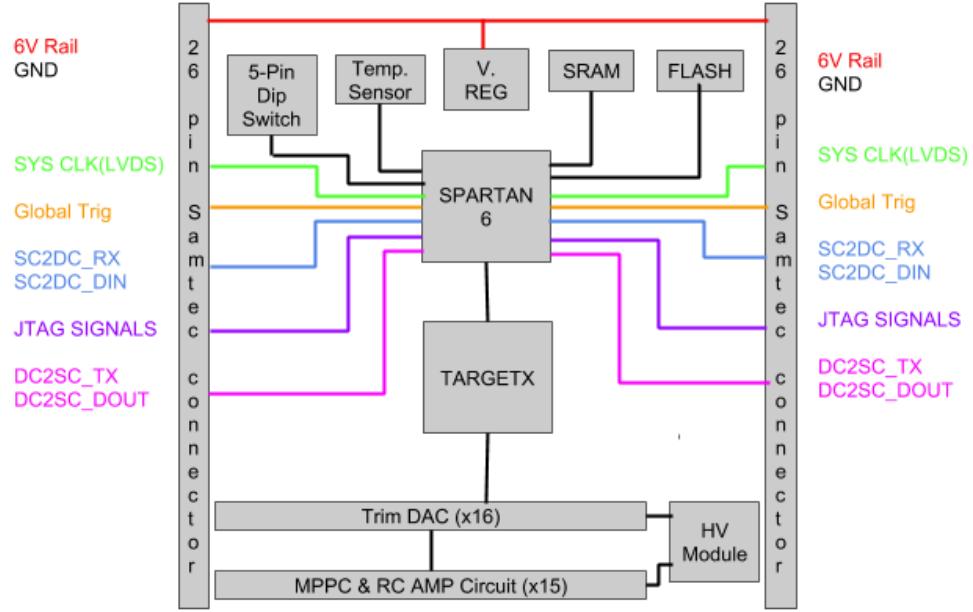


Figure 3.7: Block diagram of major components and connector pin layout of the Next Gen BMD DC.

Directly programming the DCs can be done by using standard JTAG protocol or indirectly using the on-board flash memory. The JTAG signals on each DC is configured to provide a present signal when a DC is inserted to the end of the chain. With the addition of this feature the chain of DCs can be easily programmed from one end of the detector rather than having to program each DC individually.

In the Next Gen DC, the pre-amplifier gain stage for each channel was originally planned to be omitted to decrease power consumption of the entire system. The pre-amplifiers were replaced with a RC gain circuit (ref. Fig.3.8) to provide the needed gain to the MPPC signal. The gain can be adjusted by changing the value of the resistor, R8. Using Equations 3.1, 3.2, and values of 1k for R, 5 ns for rise time, and 0.75M for the gain of the MPPC [8] the expected single PE MPPC signal is ~ 40 ADC counts.

$$dI = \frac{dQ}{dT} = \frac{\text{gain} * \#pe}{\text{RiseTime}} \quad (3.1)$$

$$\text{ADCcount} = \frac{dI * R}{V_{percount}} \quad (3.2)$$

Replacing the amplifiers with this circuit kept the rising edge of the Next Gen's MPPC signal relatively the same as 1st Gen's, however, the falling edge of the signal was increased to 10 ms. The increase is attributed to the RC time constant from R8 and C24. The increase of the falling edge could possibly shift the baseline for sequential events. Future testing is needed to find the optimal values for R8 and C24, to prevent the falling edge of the MPPC pulses from colliding with the rising edge of the following pulses. Optimization may help to verify that the amplification of from the circuit will result in a MPPC signal large enough to be differentiated from noise.

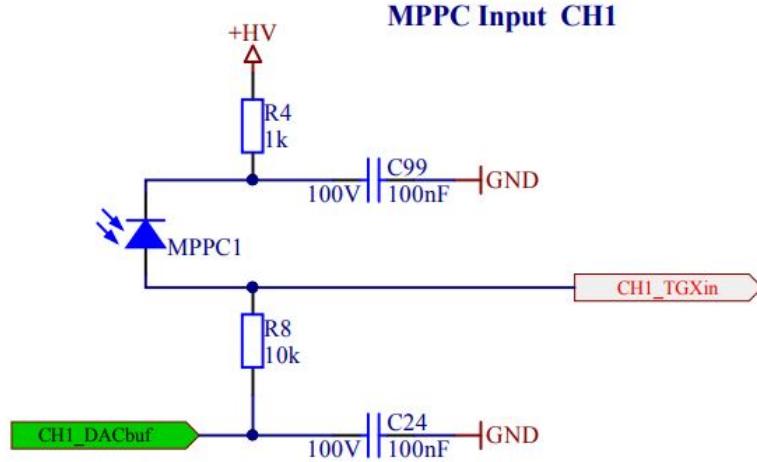


Figure 3.8: RC gain Circuit being tested in the 2nd gen BMD DC, which will replace the pre-stage amplifiers.

3.5 TARGETX ASIC

The TARGETX ASIC is a waveform digitizing ASIC, functioning as an advanced Analog to Digital Converter (ADC). The ASIC has 16 channels, each with 512 windows of 32 sample cells per window, and 12 bit per sample. The ASIC is capable of sampling Radio Frequency (RF) signals at 1 Giga-Samples Per Second (1GSPS) [6]. At maximum speed, the TARGETX ASIC is able to store up to $16.3 \mu\text{s}$, which equates to 1 ns per sample. The ASIC also offers self-triggering and settable threshold values. These compartmental features make the TARGETX ideal for use in semiconductor photon detectors such as muon and neutrino detectors (ref. Table 3.1).

Table 3.1: TARGETX ASIC specification [6].

Parameter	Value
Channels per ASIC	16
Sampling rate	1GSPS
Sampling array	2x32
Starge array	512x32
Input Noise	1-2 mV
DC RMS dynamic range	11 bits effective
Signal Voltage range	1.9V
LVDS sampling clock speed	16 MHz
LVDS digitization and Readout clock	64 MHz
Signal sampling resolution bits	10 - 12

The TARGETX ASIC, designed at the IDLab by Dr. Gary Varner [6], was fabricated in TSMC 250 nm CMOS process, and belongs to a family of chips intended for detectors with sampling rates of 0.5 – 1.2 GSPS (ref. Fig.3.9a). The ASIC is driven by an external FPGA, which provides all necessary clocks and readout instruction to the chip once a trigger is detected. The digital readout of the chip is done serially for all channels simultaneously, digitization is initiated by enabling the readout enable pins, setting the desired memory address, and providing the Wilkinson ADC converters with a clock (ref. Fig.3.9b).

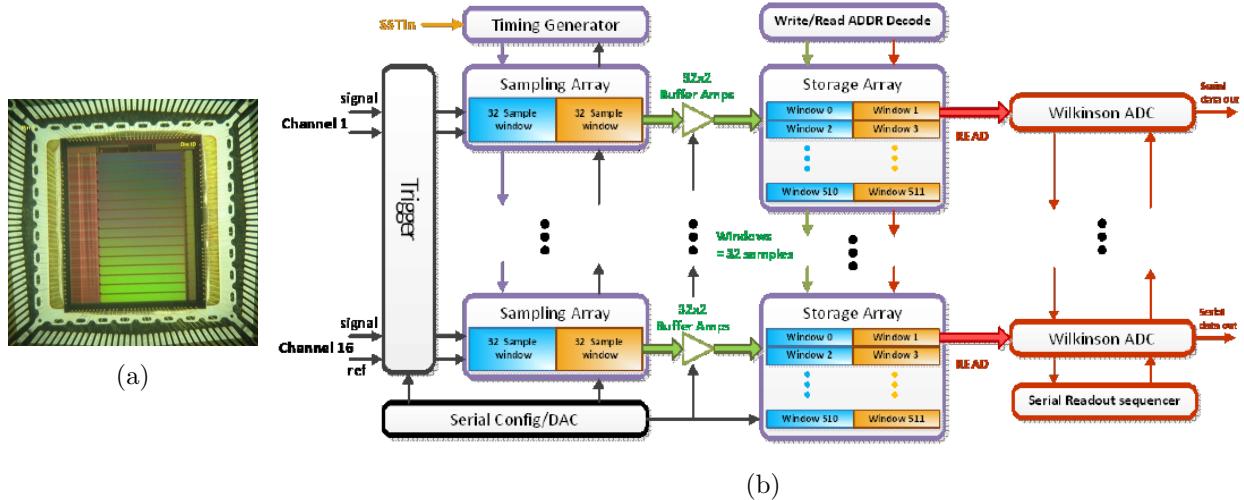


Figure 3.9: (a) Photograph of the TARGETX Waveform Digitizing ASIC [6] and (b) Block Diagram of TARGETX ASIC [6].

3.6 SCROD Rev A5

The Standard Controls and Read Out Device (SCROD), a development board designed by Xi-aowen Shi at the IDLAB at UHM, uses a Xilinx Spartan 6 XC6SLX150T FPGA. The SCROD can be programmed directly with the standard JTAG protocols or indirectly via on-board Flash memory. It has a fiber transceiver for communication with a PC and two Ethernet ports that can be repurposed for a variety of functions [11]. The SCROD A5 (ref. Fig.3.10) acts as the master FPGA in the BMD system, bridging the gap between the PC and BMD DCs via BMD communication firmware and gigabit ethernet. As the master unit, the SCROD is responsible for distributing commands sent by the PC, multiplexing the digital data from the DCs, and distributing the system clock to the detector.

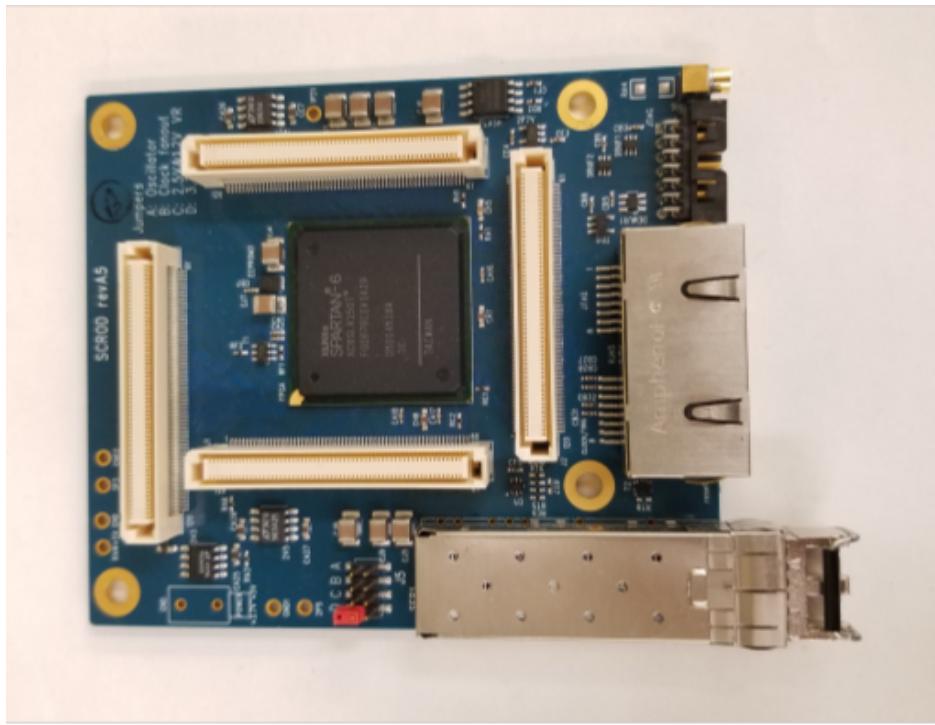


Figure 3.10: Photograph of the SCROD A5.

3.7 Connector Boards

New interconnect boards were designed (ref. Fig.3.11) to enable the connection between the SCROD and the DC chain on the top and bottom planes around the corners of the tracker frame. The first boards links the SCROD to the DC chains on the tracker frame (ref. Fig.3.11a). This card acts as a hub for all signals from the detector to pass through. The JTAG connection to each DC chain was moved to the interconnect board for easy access. The second interconnect boards connects all the DCs on each frame in a serial chain, over a ribbon cable (ref. Fig.3.11b). Adding the connector boards complete The Enterprise allowing for firmware and software testing.

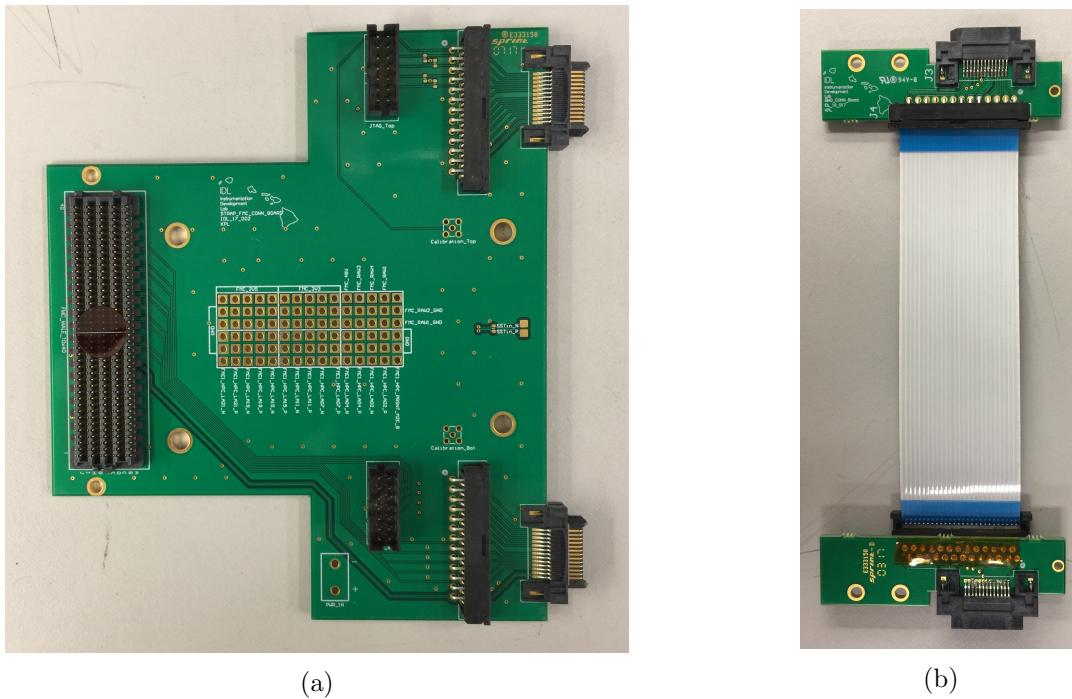


Figure 3.11: (a) Photograph of interconnect board designed to link the SCROD and Next Gen BMD DC around the HMB tracker frame and (b) interconnect board designed to link DCs together in a serial chain.

CHAPTER 4

FIRMWARE AND SOFTWARE

Directly connecting all 1st Gen BMD DCs to the SCROD enabled the SCROD to communicate with each ASIC directly. Making TARGETX register programming and readout very fast. The drawback to this configuration was that it made it impossible to place readout electronics, MPPC sensors, and scintillating planes inside a small borehole. The Next Gen BMD solves this issue by placing the SCROD at the top of a serial chain of new BMD DCs. Each of the new DCs has its own dedicated set of readout electronics and MPPC sensors, allowing the DCs to readout the TARGETX ASIC independently from the SCROD and other DCs in the system. This feature allows the Next Gen BMD to be scalable. Placing the DCs and SCROD in this configuration however, comes at the cost of communication speed. Due to these changes, new firmware and software had to be developed to enable a new communication protocol, event triggering protocol, and readout process. This section will go over in detail the major changes between the two generations of firmware and software.

4.1 System communication

With the limited space inside the hollow area of the new scintillating planes of the Next Gen BMD, routing large amounts of cables through the detector for communication was not feasible. For that reason the DCs of the Next Gen BMD are placed in a daisy-chain configuration. In this configuration the SCROD will only be directly connected to one DC from each plane, making direct communication from SCROD to each DC no longer possible. A new communication protocol was developed to enable the SCROD to command with each DC in the chain individually. Due to size constraints and pin limitations of the selected connector, each DC now has a Spartan 6 LX9 FPGA added to issue all local commands. The DCs also contain a settable hardware address that are the DCs identification numbers. With the addition of an FPGA on each DC the complexity of communicating commands to each ASIC increased. But in exchange, adding the FPGA decreased the required pin count necessary to readout 10 ASICs from 500 pins (50 pins per TARGETX) to 5 pins.

Since all DCs are now linked together in a daisy-chain, communication to the DCs is done serially. When a command is sent, each DC buffers all commands and redistributes it to the next DC in the chain. Each DC then checks all commands sent from the SCROD and will only parse commands that contain a matching address or the global address. The new communication protocol will work much like a standard serial peripheral interface (SPI) such that the communication requires a dedicated clock (25 MHz), receive signal (RX), transmit signal (TX), and two data lines. Commands will be sent in 32 bit words that will contain the DC address along with command type

and command data (ref. Table 4.2). When commands are sent through the system they are held in internal First-In First-Out (FIFO) memories inside the DC FPGAs until they are parsed and placed in to control registers (ref. Table 4.1).

Changing the communication to this proprietary protocol gives the Next Gen BMD the ability to be modified to have any number of DCs. In addition, readout of all TARGETX ASICs, can be done simultaneously via DC FPGA. But since communication will be done serially, the time required to complete readouts from ASIC to PC will be highly dominated by the speed that the serial communication can achieve. From the testes done in chapter 5, the Next Gen BMD can achieve a readout rate of ~ 60 Hz.

Table 4.1: List of control registers for SCROD and DC.

Register	SCROD Function	DC Function
0	Resets all SM(0)	Resets all state machines(0) Enables calibration CH(4)
1	SCROD ID(0)	1/2 TX register data(6-0)
2	Not used	2/2 TX register data(11-0)
3	Not used	TX load period
4	Not used	TC latch period
5	Software Trigger(0)	Software Trigger(0)
6	Trigger Mode(3-0)	Trigger Mode(3-0)
7	DC enable mask(3-0)	DC enable mask(3-0)
8	Output Mode(3-0)	SCROD acknowledgment wait(15-0) Offset window direction(15) number of windows to offset(8-0)
9	Not used	Number of windows to readout(8-0)
10	Not used	Not used
11	Not used	Enable fixed window readout(15)
12	Enable fixed window readout(15) Start window for readout(8-0)	Start window for readout(8-0) Ped cal enable(15)
13	Not used	Number of average for ped cal(3-0)
14	Not used	Reset sample window counter(15)
15	Not used	Timing reset parameter for sampling logic(1-0) Wait period for digitization ramp
16	Not used	Trim DAC address(4-0)
17	Not used	Trim DAC value(11-0)
18	Maximum trigger count	Maximum trigger count
19	Trigger count enable(0)	Trigger count enable(0)
69	1/2 trigger scalar count	1/2 trigger scalar count
96	2/2 trigger scalar count	2/2 trigger scalar count

Table 4.2: Break down of command word used for Next Gen BMD.

Command Type	SCROD Function	DC Function
A	Start DC Readout	Readout TARGETX
B	Not Used	Write TARGETX Register
C	Not Used	Program Trim DAC
D	Register Readback	Register Readback
E	Wait	Wait
F	Program Control Register	Program Control Register

Command Word (32 bit): DC# (4 bits) + cmd type(4 bits) + reg#(8 bits) + register value(16 bits)

BMD readout software was also redeveloped as a direct result of changing the readout firmware from a single FPGA to multiple FPGAs. In the 1st Gen the PC only communicated with one FPGA containing one set of control registers. The Next Gen BMD's PC now must communicate with and program as many FPGAs as there are DCs, in addition to the SCROD (ref. Fig.4.1). As well as preventing crosstalk between DCs when the serial data link is in use.

Using Python and a virtual machine running Ubuntu, the PC communicates with the SCROD via standard fiber optic Ethernet link. The SCROD will act as a master FPGA, route commands from the PC to the most relevant path, and issuing data readout commands to selected DCs once an event trigger is detected. Data coming to the PC is in hexadecimal and is converted to binary before being passed through parsing scripts written by Chris Ketter. The parsing script extracts the readout packet information, raw ASIC data, and saves it to a text file for future analysis.

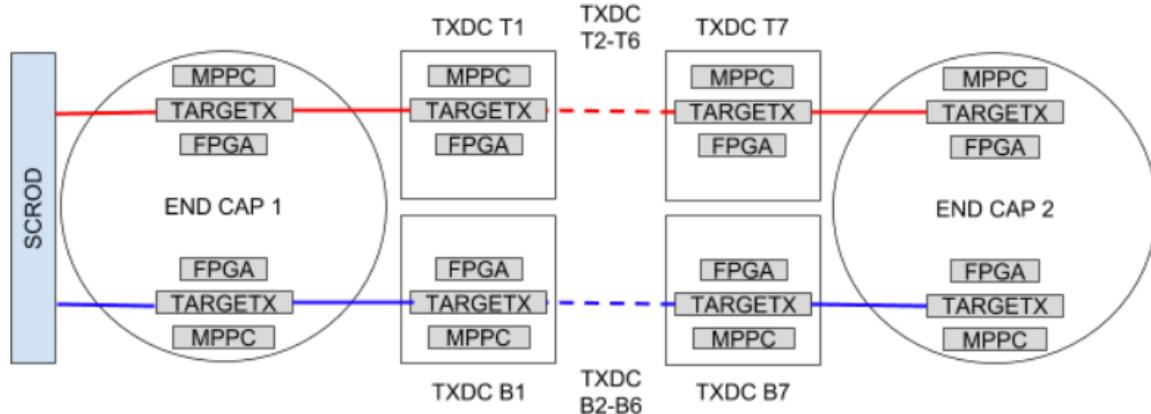


Figure 4.1: Block overview of 2nd gen BMD system from SCROD to last end-cap DC.

4.2 Event Trigger Protocol

The readout process starts with the event trigger protocol. In the 1st Gen BMD trigger bits from all TARGETX ASICs were routed directly to the SCROD, where the firmware made trigger decisions based on coincidences of enabled ASICs. Alternatively in the Next Gen the trigger logic is divided into two types and is propagated through the serial chain using two INOUT pins. One pin is designated for up-streaming coincidence triggers and receiving acknowledgments and the other for down-streaming the acknowledgments and receiving triggers from down stream DCs.

The first type of trigger is a coincidence trigger between any center and end-cap DC on the same plane. The protocol is executed by first ORing all trigger bits from the local TARGETX ASICs. The end-cap DC then sends its ORed result to the center DCs. The center DCs propagate the end-cap trigger through the serial chain, while monitoring its own local ORed trigger. When the ORed trigger of any center and end-cap DC on the same plane is active for greater than 32 ns, the event is considered to be a coincidence trigger for that plane. When a coincidence trigger for the plane is detected, the center DC that issued the trigger will hold its up-streaming trigger pin high for 80 ns. At the end of 80 ns, the DC waits for a settable amount of time for an acknowledgment from the SCROD to be issued on the same pin. If no acknowledgment is received within the wait period the trigger state machines will reset back to idle.

The second type of trigger is an event trigger done at the SCROD level. When the coincidence triggers from both planes are active for longer than 8 ns, it is considered a possible muon event. Once the SCROD detects an event trigger, the SCROD issues an acknowledgment to all DCs and sends a trigger packet to the PC. At which time, the DCs readout its local TARGETX and saves the data to a local Block Random Access Memory (BRAM). Once the PC receives the trigger packet, it issues an acknowledgment to the SCROD, along with directions for which DCs to readout.

To filter out false triggers from thermal discharges and lower data rates, the Next Gen requires coincidence triggers from both planes in the detector before issuing an event trigger and starting the readout process. Executing the trigger decision in this manner will cut the number of required pins for triggering of 10 ASICs from 50 pins (5 pins per ASIC) to just 2 pins (1 for up-stream and 1 for down-stream). A clear flow chart of the trigger logic can be seen in Figure 4.2.

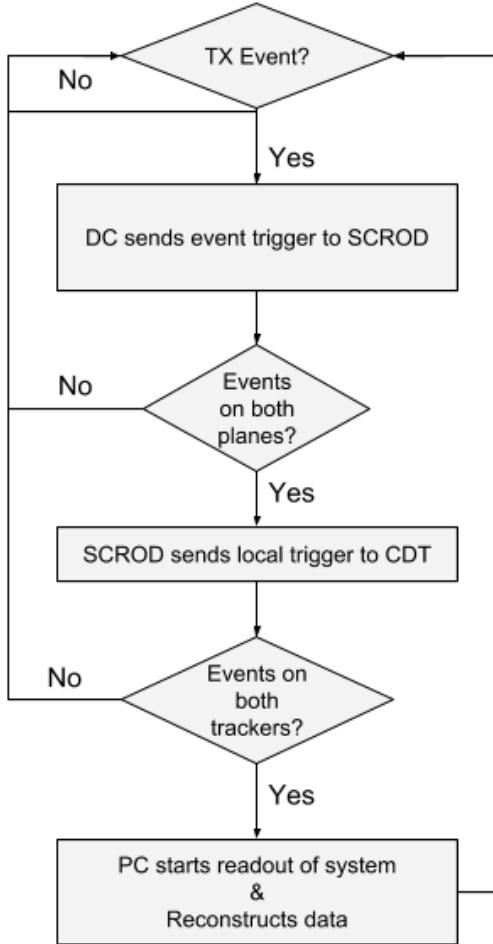


Figure 4.2: Logical flow chart of the trigger decision process for the 2nd gen BMD.

4.3 Readout Process

Although the underlying steps of reading out the TARGETX are the same for both generations, the actual readout process in the Next Gen comes with an extra difficulty of an intermediate data transfer process from the DC to the SCROD before being delivered to the PC. Since each DC now has its own FPGA, responsible for all local operations, the firmware for the Next Gen BMD is divided into two levels. The first level is at the SCROD; at the first level coincidence triggers between scintillating planes are monitored, along with issuing readout commands, repackaging data from DCs, implementing pedestal subtraction, and clock distribution. At the second level, each DC is responsible for all operations of the TARGETX ASIC and supporting ICs, pedestal calculation, buffering and syncing communication signals to data clock, and redistributing system clock and commands from the SCROD to down stream DCs.

The readout of the TARGETX is done in blocks of 4 windows. Each window containing 32 samples at 12 bits per sample. Once an acknowledgment is received, the FPGA starts the readout process by setting the read address in the TARGETX and initiates the digitization process. Digitization of the TARGETX ASIC memory is done one window at a time. During digitization, data for all channels is digitized at the same time. When digitization is complete, the Readout Control State Machine reads out the data for all channels simultaneously and save the data into a BRAM. This process is repeated until the readout process has read out the desired number of windows. Once all windows are read out, the DC waits for the SCROD to issue the data transfer signal.

When the transfer signal is received, the DC will readout the BRAM and package two samples of data into a 32-bit word and shift the data into a First-In, First-Out (FIFO) memory block. The data is then sent to the SCROD through the serial chain via the new communication protocol. The SCROD repackages the data by extracting each sample of data, placing the sample into another 32-bit word that contains window and sample number. The SCROD then either does pedestal subtraction, or sends back raw data to the PC (ref. Fig. 4.3).

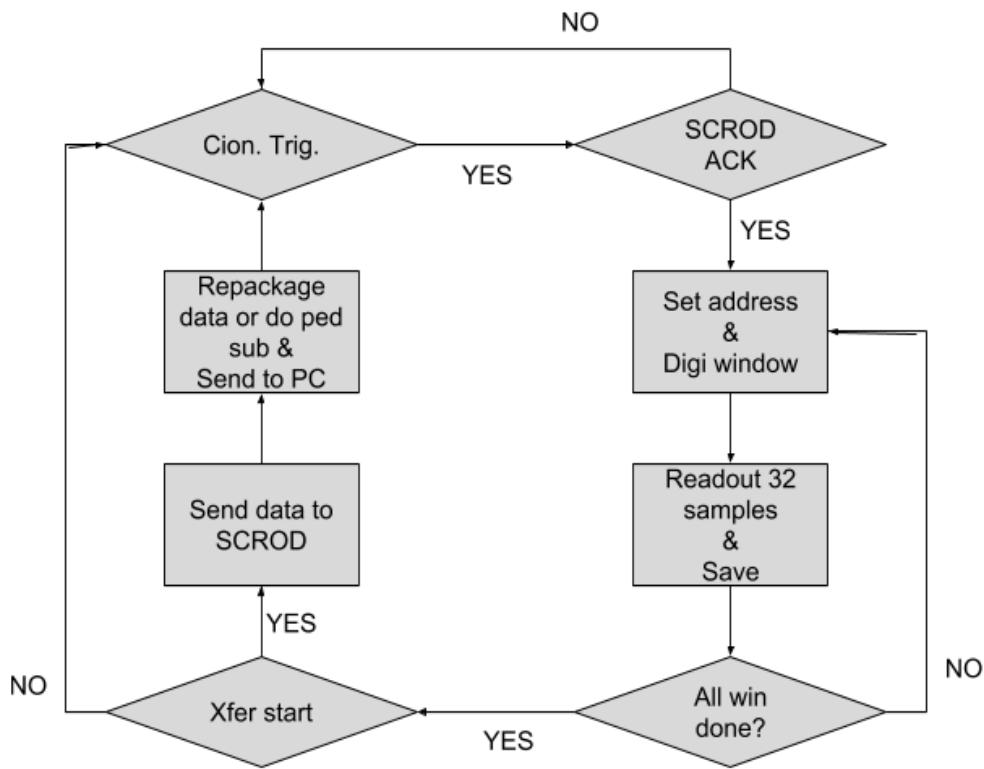


Figure 4.3: Logical flow chart of the readout process of one DC for the 2nd gen BMD.

CHAPTER 5

CALIBRATION AND RESULTS

With the completion of the Next Gen center DC, scintillating plates, firmware, software, tracker frame, cover plates, and standoff legs, The Enterprise was assembled and placed into a temporary dark box (box with no light leakage) for functionality testing. Once reliable communication, data readout, and pedestal subtraction can be achieved it will mark the end of stage one and the start of stage two of prototyping. In stage two, data sets and simulation will be done to estimate the optimal scintillating plane thickness. The calibration process began by placing the assembled tracker into a dark box, (ref. Fig.5.1) the first stage of calibration programed all DCs using the JTAG connectors in the SCROD to DC interconnect Board (ref. Fig.3.11a). Then a functionality and accuracy test for all supporting ICs on each DC, followed by implementation of threshold and trim DAC scans. The sections below describe the steps taken to calibrate the tracker planes and the results from the pedestal subtraction, injected sine wave reconstruction, LED pulser, and results from initial data sets.

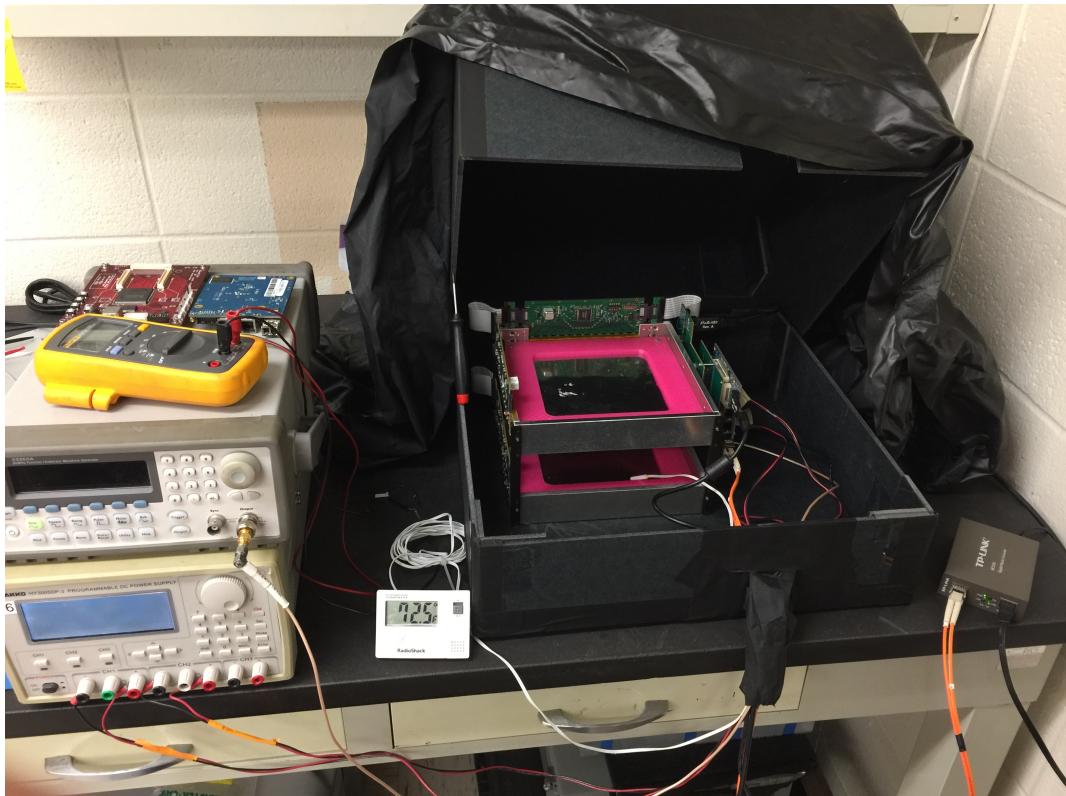


Figure 5.1: The fully assembled tracker with all connections placed inside the temporary dark box.

5.1 Threshold and Trim DAC Scans

Threshold and Trim DAC scans sought to find a region of operation where the TARGETX and MPPC sensors are sensitive to single photon events. New software and firmware was developed to scan over trigger thresholds and MPPC HV bias (the difference in voltage between the HV module and trim DAC), while counting the number of triggers from the TARGETX for 16,777,216 clock cycles at a clock rate of 62.5 MHz (~ 0.25 seconds). These values were then used to calculate the trigger rate of each MPPC in kilo-Hertz. By comparing trigger rates to threshold values, a region of operation can be chosen where single pixel events are distinguished from multi-pixel events.

Similar to the 1st Gen the HV module provides the coarse adjustments and the trim DAC provides the fine adjustments for the MPPC HV bias. Due to the omission of the pre-amplifier stage in the Next Gen DC, the trim DACs in the new DCs also provides the Voltage Pedestal (VPed) offset for the TARGETX. Requiring a new threshold baseline scan to be done for every trim DAC increment. The threshold scan is broken into three stages: (1) Baseline Scan, (2) Fine Scan, and (3) Offset Scan. Thresholds in the TARGETX is changed by programming dedicated internal registers for each channel, each register is 12-bits long with each bit equating to ~ 0.6 mV. A flow chart of the scan can be seen in Figure 5.2.

The script starts by setting the MPPC HV bias and TARGETX thresholds on all channels to minimum (trim DACs to max and threshold registers to zero) and the HV module to the selected value. Over the entire scan the voltage at the HV module will be left unchanged, while the trim DACs will be scanned over the range of 2V to 1V in increments of 0.1V. With each increment of the trim DAC, the script will step through the three stages of threshold scans.

The Baseline Scan is done to the same channel on all DCs simultaneously to optimize time. The upper and lower threshold range is set to ± 256 DAC counts from the current trim DAC value and increments 4 DAC counts for each step. A trigger count is then calculated with each increment. The value that yields the highest trigger count is considered to be the coarse baseline. The Fine Scan is performed individually on each channel in the detector. The scan starts 30 DAC counts below the coarse baseline and increments by 1 DAC count until no triggers are present. Similar to the coarse scan, the triggers are counted and the values are saved into a file with each increment. The threshold value that gives the highest trigger count is then the fine baseline. For the last stage of the scan, a final trigger count with an offset of 10 DAC counts from the fine baseline, is taken and saved into a text file as the final baseline for the current DAC value. Trigger counts from this stage will be out of the input noise and have a high probability of being a muon event.

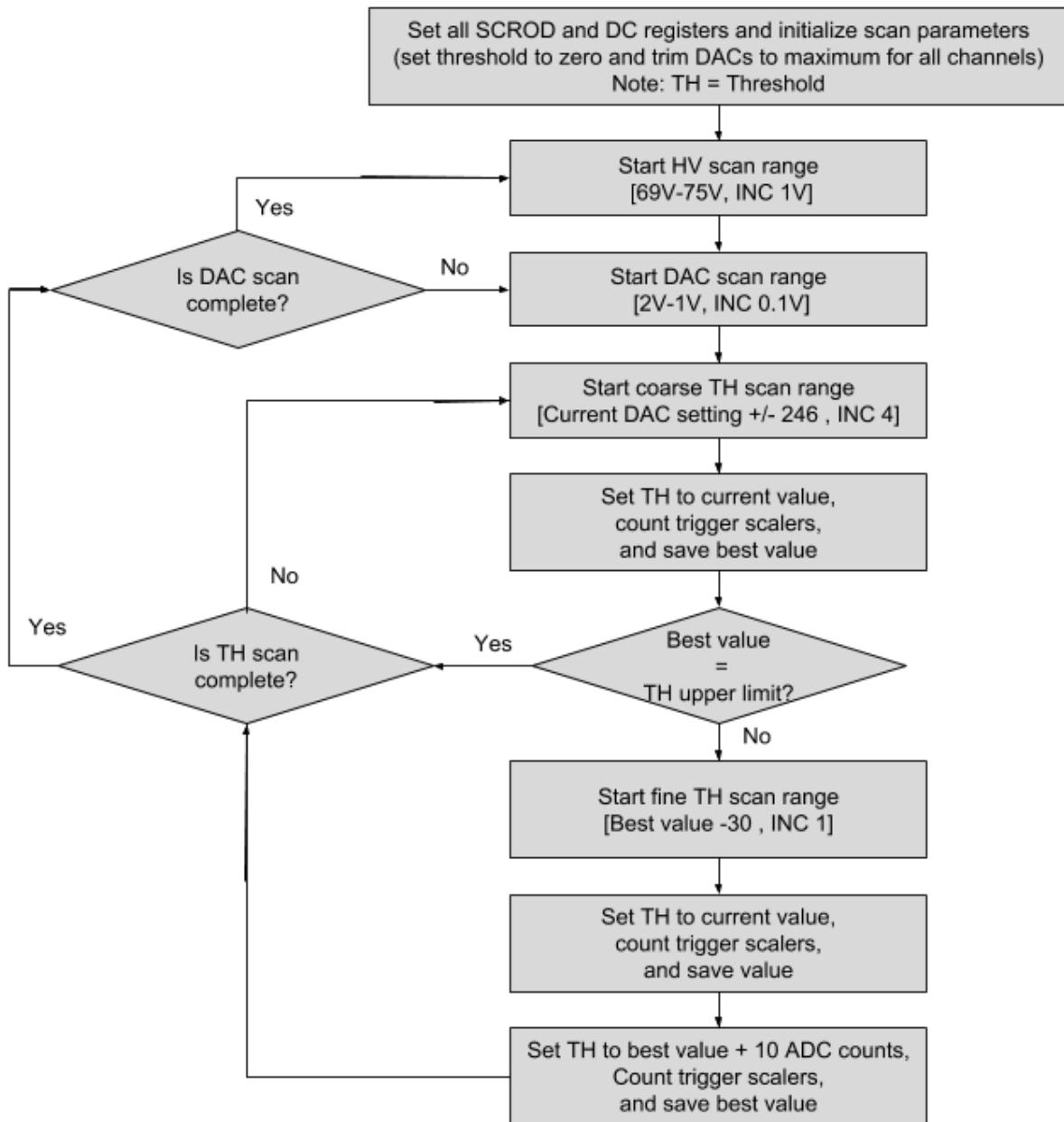


Figure 5.2: Flow chart of threshold and trim DAC scan.

Once a region of operation is defined where the MPPC sensors are sensitive to single photon events, the script will start an event trigger scan that counts coincidence triggers from all DCs rather than counting triggers from individual DCs. The event trigger scan is done over a span of one second, so that trigger rates in the hertz can be counted. In this scan, the goal is to find a threshold offset from the final baseline that yields an approximate event trigger rate roughly the

expected trigger rate for muons at sea-level. The expected event rate is proportional to the active area of the detector and the allowable angle of incident. Using Equation 5.1, assuming that the allowable incident angle is 180 degrees, and 0.04 m^2 for the active area of one tracker plane (20 cm by 20 cm). The expected muon event rate should be roughly about 17.6 Hz. Using 17.6 Hz as an ideal rate the secondary scan will start at the baseline found from the first two stages and add increments of 1 ADC count to all baseline values for every channel in the system until a event trigger rate closes to the ideal rate is found.

$$Area * 2 * \pi * 70 * \oint_{\phi}^0 \sin(\phi) \cos(\phi)^2 d\phi \quad (5.1)$$

5.2 Pedestal Subtraction

The ability to perform pedestal subtraction is vital to achieving a system that is sensitive to single PE events. Since arbitrary differences are present in each sampling capacitor, input buffer, component routing, and digitization ramp linearity, each sample is slightly offset from one another, making the raw data non-ideal (ref. Fig.5.4a). To account for these offsets, pedestal data is calculated and subtracted from corresponding samples in the raw data. The result is an accurate representation of the signals at the analog inputs of the TARGETX ASIC. Pedestal data is obtained by reading out the entire memory of the TARGETX multiple times and averaging each sample by the number of repetitions.

Pedestal calculation in the Next Gen BMD and tracker planes were performed either via firmware (ref. Fig.5.3a) or software (ref. Fig.5.3b) and can be saved either in the SRAM on the SCROD or on the memory of the PC, by setting the calculation mode register in the BMD Read Control script. In firmware mode, the script sets necessary control register and does software triggered readouts of the same set of 4 widows for a selected-able number of repetitions. With each readout, the new data is summed to the previous values. At the end of the pedestal calculation, the firmware averages the values over the number of repetitions. The averaged values for each sample of the set of 4 windows is sent back to the PC, parsed, and saved into a text file. This process will continue over the entire 512 window memory of the TARGETX.

In software mode, the script will readout the entire 512 window memory of the TARGETX in blocks of 4 windows for a select-able number of repetitions. With each readout in software mode the script will save readout data into a text file until the last repetition is complete. The script then parses the data and sums each sample of the memory to the corresponding sample of each repetition. At the last repetition, the script will average and save the pedestal data into a text file.

Pedestal subtraction can also be done either via firmware or software by setting control registers in the script. In firmware mode, the SCROD extracts the correct range of samples for the readout from the SRAM on the SCROD and does the subtraction to the corresponding sample during the

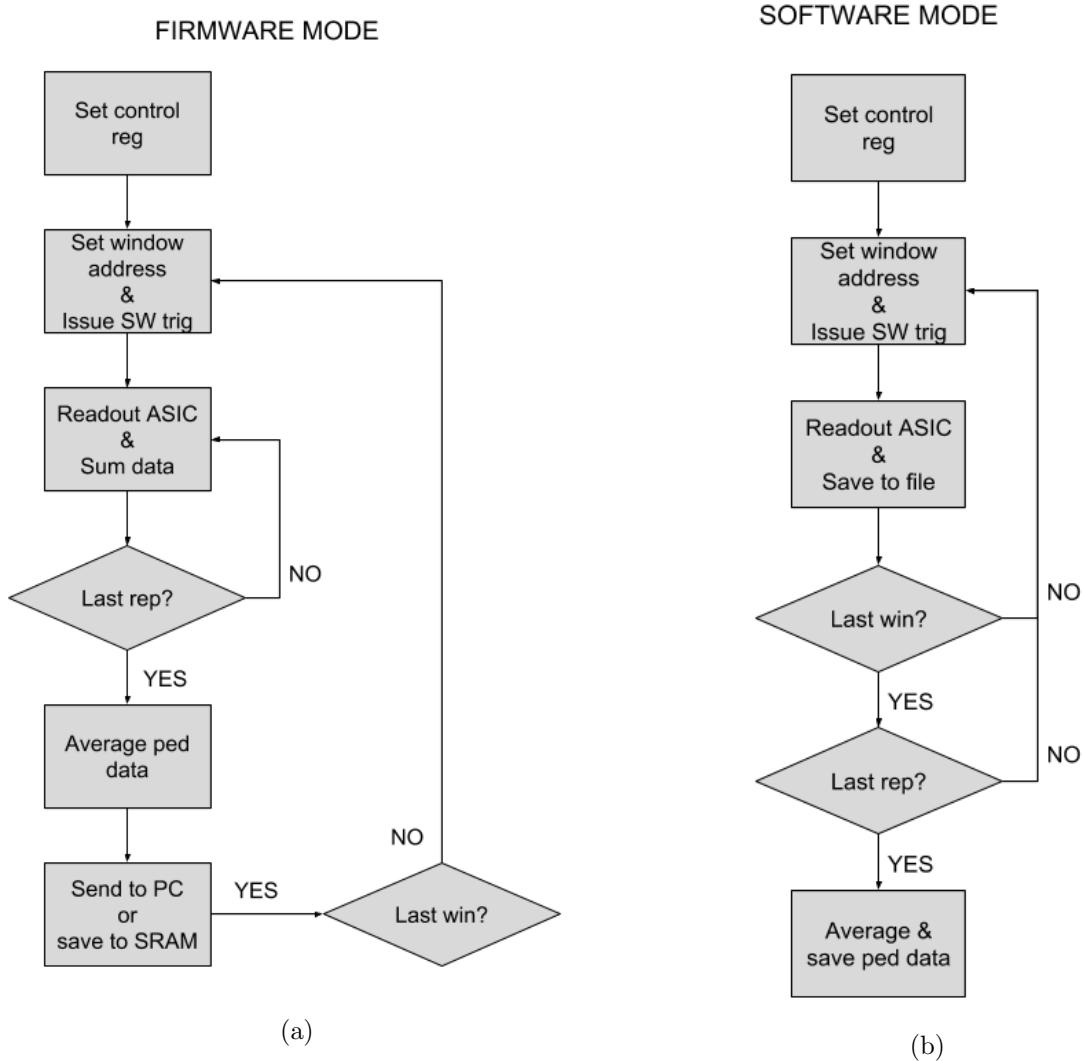


Figure 5.3: Flow chart for pedestal calculation in (a) firmware mode and (b) software mode.

repackaging period. In software mode, the raw data is read out and saved in the memory of the PC, pedestal subtraction takes place during the post-parsing stage and is done in a similar method as the firmware mode.

To illustrate the effectiveness of pedestal subtraction, a comparison of non-pedestal subtracted readout (ref. Fig.5.4a) versus pedestal subtracted readout (ref. Fig.5.4b) can be seen in Figure 5.4. Pedestal data used in Figure 5.4 was done in software mode by taking 100 successive readouts of the entire memory of the TARGETX and averaging each sample cell. A histogram of raw (ref. Fig.5.4c) and pedestal subtracted data (ref. Fig.5.4d) from 4 windows is also shown in Figure 5.4. Comparing the histogram distribution from both data sets, it can be seen that after pedestal subtraction the Standard Deviation (STD) σ of the data is reduced from 25.54 to 1.22, leaving a

noise level of approximately 1.22 ADC counts with a mean of -1.52. The negative mean value could be a product of the drift in temperature from when pedestal were taken versus readout. Another contributing factor is the fluctuation in HV over the span of time it took to collect the pedestal data. Since the pedestal data is taken over a span of 5 seconds and normal software trigger readouts are done in milliseconds. The instantaneous value of the HV could be slightly higher or lower than that of the average HV over the 5 seconds. This could result in a mean that is slightly above or below zero.

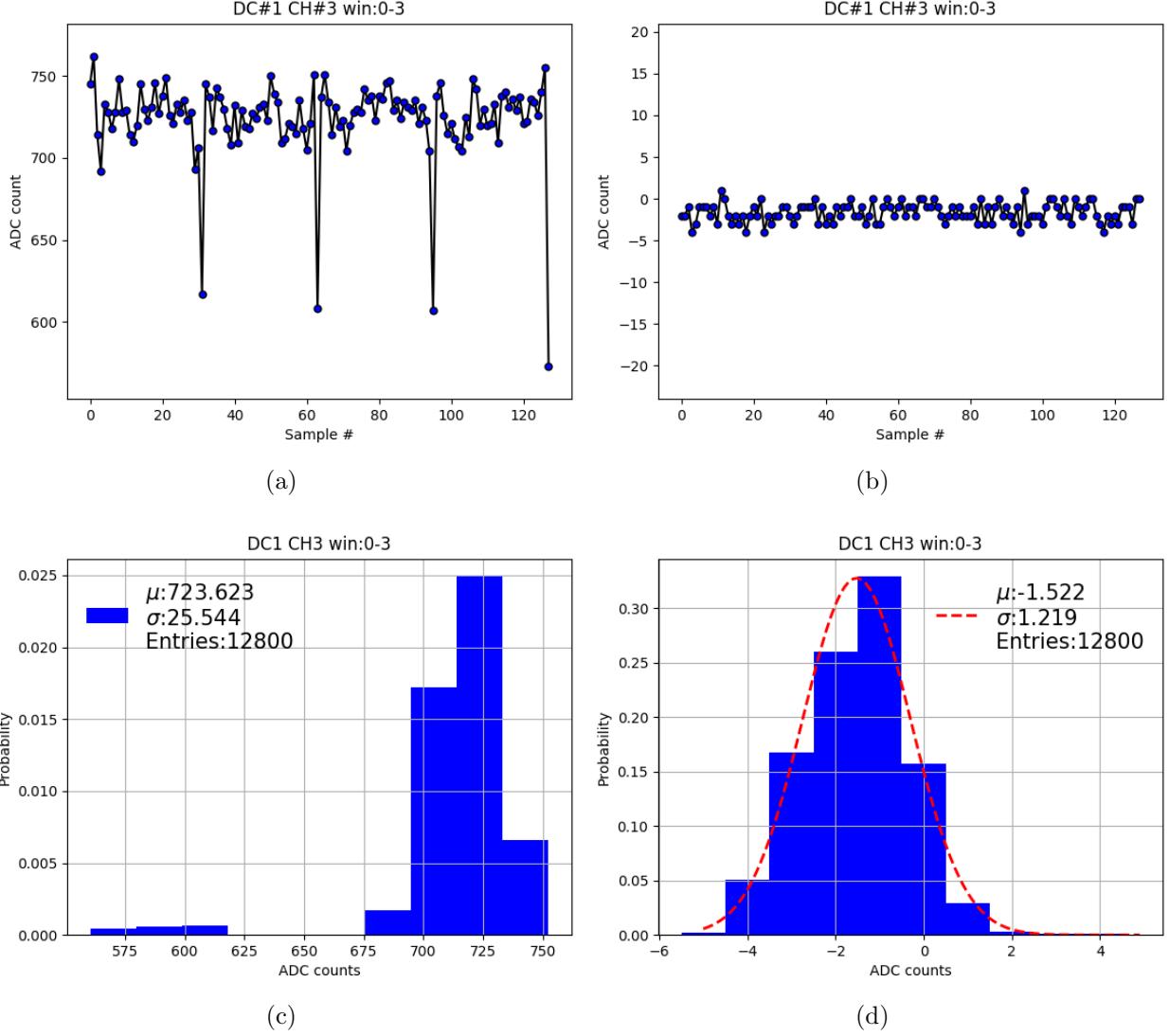


Figure 5.4: Comparison of single event (a) non-pedestal subtracted readout vs. (b) pedestal subtracted readout from TARGETX and histogram distribution of (c) non-pedestal subtracted data vs. (d) pedestal subtracted data from 100 events.

5.3 Sine Wave Reconstruction and LED pulser

Before taking actual triggered event readouts, a sine wave reconstruction test was completed to ensure that the pedestal subtraction process was functioning properly for the entire memory of the TARGETX. For the sine wave reconstruction, a 20 MHz sine wave with an amplitude of 500 mV peak to peak, was injected into the system directly to channel 16 (ref. Fig.5.5). Further tuning of the TARGETXs Wbias registers was complete to scale the TARGETX data as close as possible to the equivalent values for an equivalent 12 bit ADC ($\sim 0.6\text{mV}$ per ADC count).

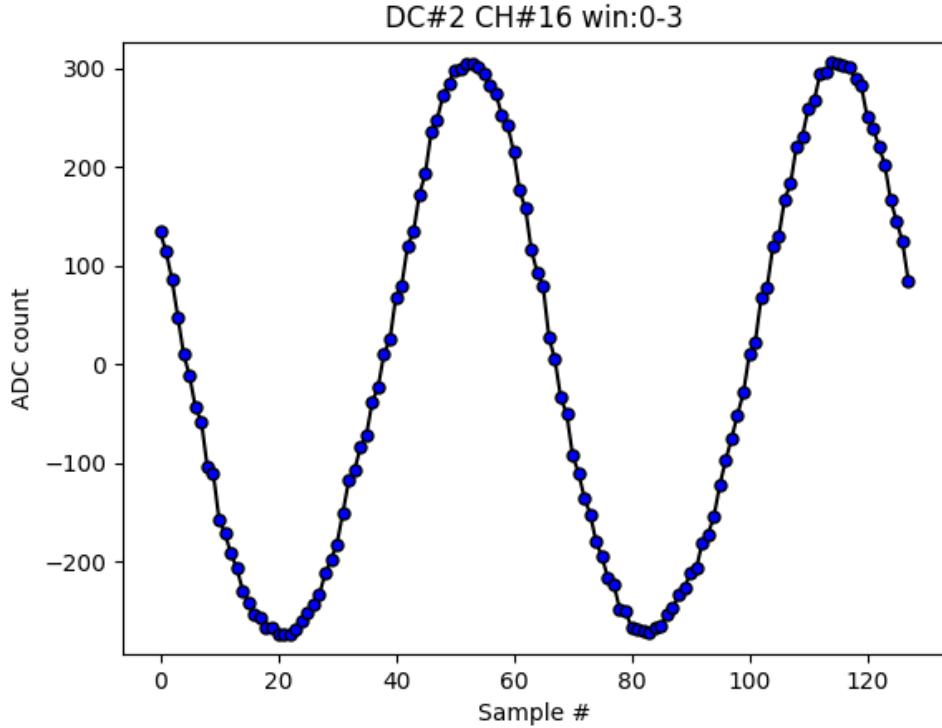


Figure 5.5: Results of sine wave reconstruction test with a 500 mV peak to peak 20 MHz sine wave.

Along with the sine wave reconstruction, an LED pulser Test was also done to find the look-back-window parameter. This parameter is used when the detector is operating in self-trigger mode as a compensation for the time between trigger and readout start. As the TARGETX issues a event trigger the current window that is being written to inside the TARGETX memory is recorded. The look-back-window parameter is then subtracted from that window number. By subtracting the look back window parameter the windows being readout will contain the event data (ref. Fig.5.6).

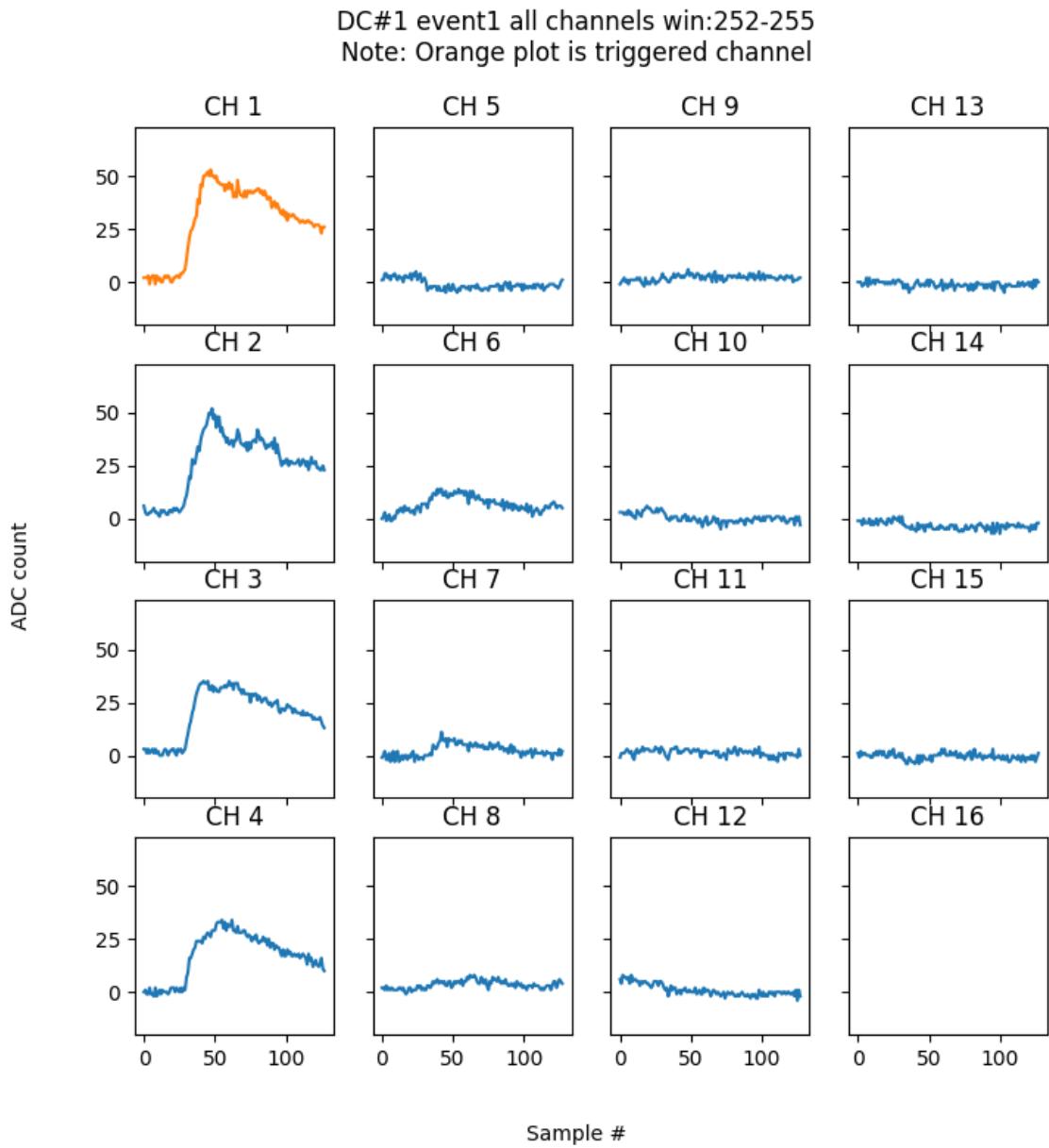


Figure 5.6: Results of LED pulser test with the detector placed in self-triggering mode.

5.4 Event Readout

The final piece of the readout process was an event trigger system that gathered triggers from individual TARGETXs, and compares their timing to demand a coincidence trigger from multiple DCs. In requiring coincidence triggers the effective event rate of the system will greatly increase. The trigger system of the Next Gen BMD and tracker planes have two modes: (1) uses two wires connected to each DC and routes trigger information back to the SCROD and (2) routes the

triggers through the DC chain using the event trigger protocol described in chapter 4. As the SCROD receives triggers from the DCs, it will require a coincidence trigger from top and bottom planes before issuing a event trigger back to the PC and starting the system readout. Figure 5.7 shows a possible muon trigger event using the self-triggering protocol.

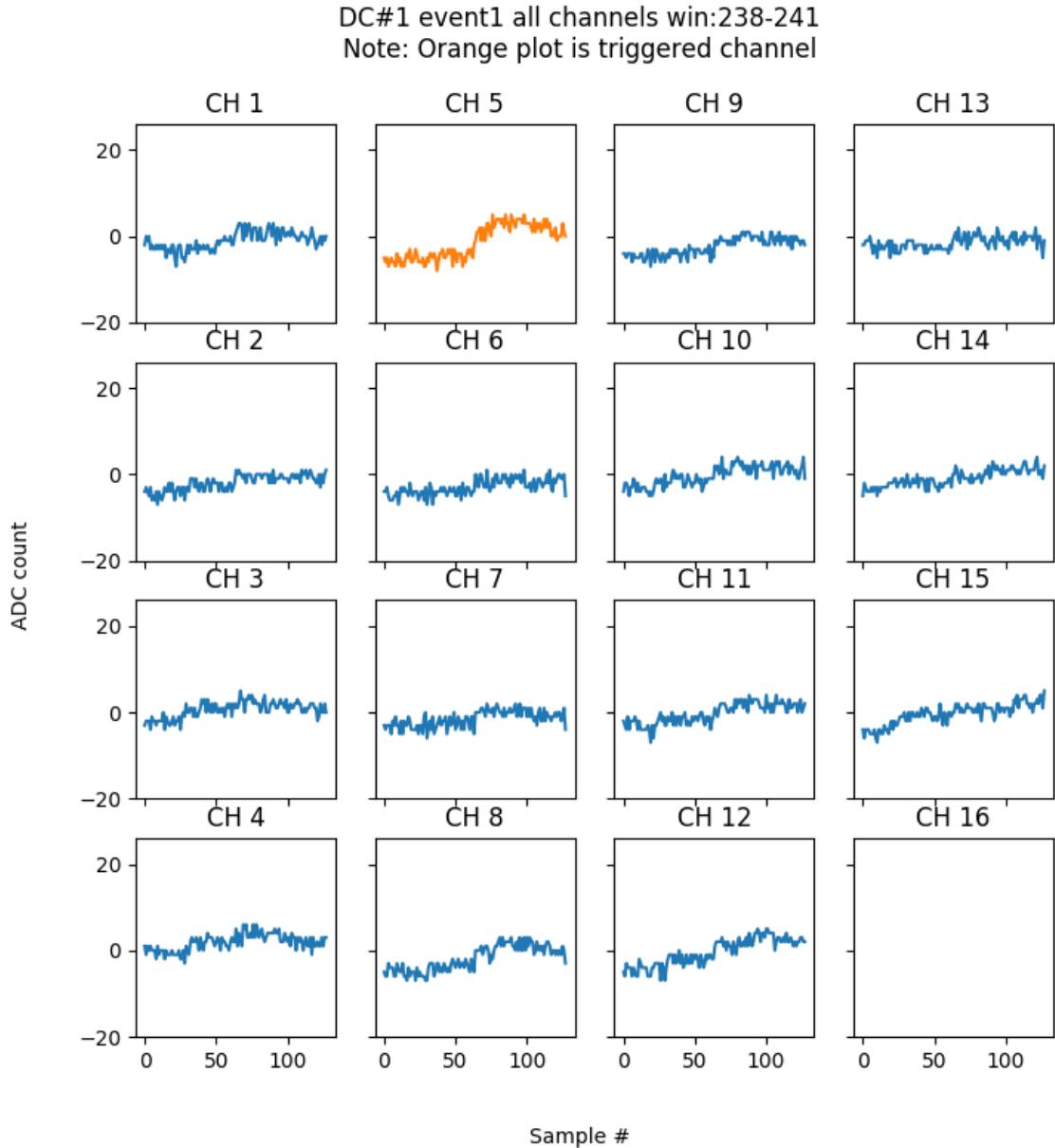


Figure 5.7: Plot of possible muon triggered event.

5.5 RC Gain Circuit Evaluation

A simple Trigger Rate versus Threshold Value Test was done to evaluate the resolution that can be achieved with the RC gain circuit. In this test, the ideal result may be a distribution that resembles steps. Each step represents a different amount of pixels activated at the same time (ref. Fig.5.8d).

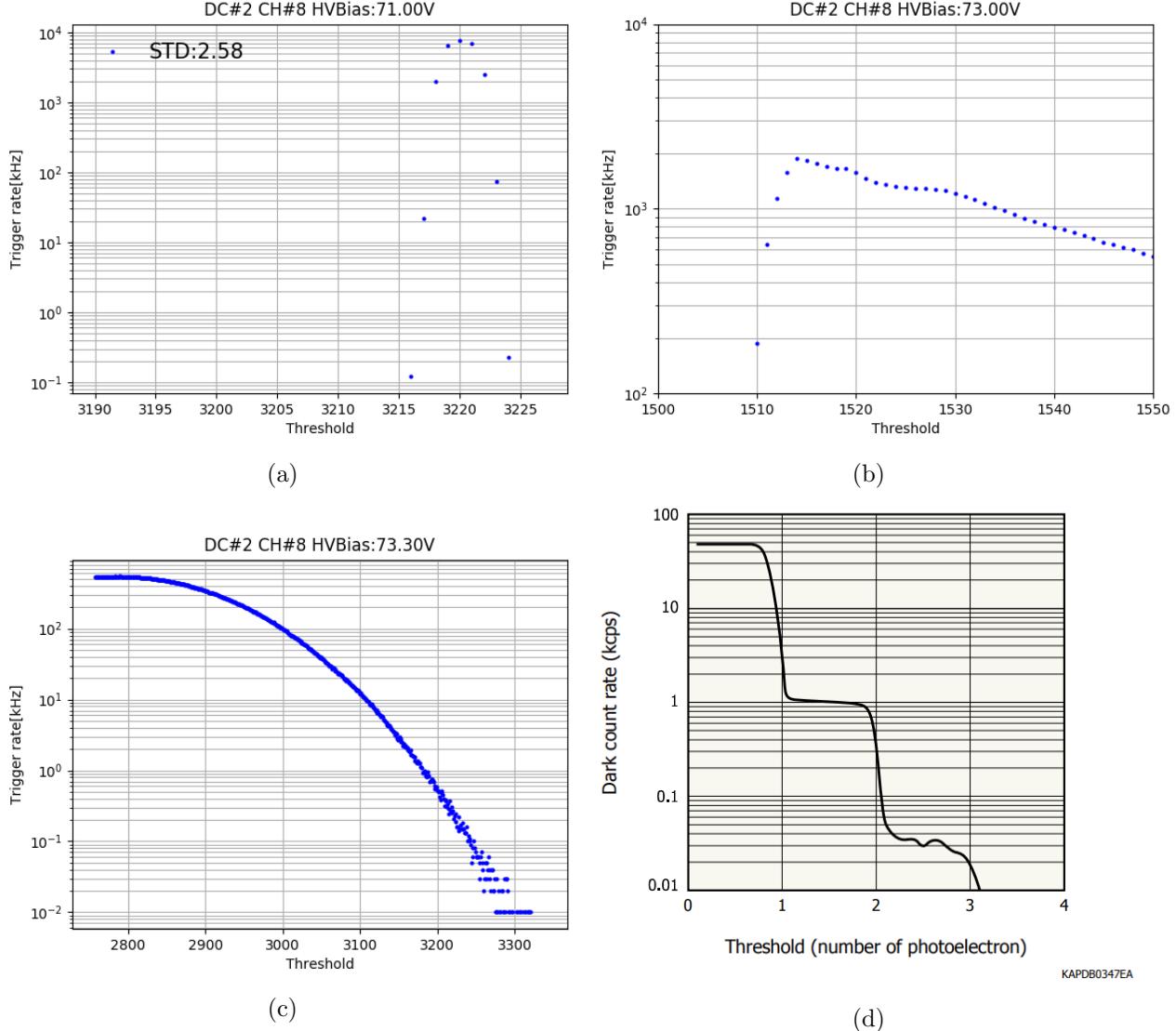


Figure 5.8: Trigger rate Vs threshold plots for HV bias set at (a) 71V, (b) 73.3V, (c) 73V, (d) ideal distribution [8].

The results of this test are shown in Figure 5.8, in the Figure, the HV bias was set to 71V, 73V, and 73.3V respectively. A resistor value of 5k was used for R8 in the RC gain circuit. Although the HV bias in the three plots is much greater than the normal operating voltage of 70V [8], no distinguishable steps were detected until the HV bias was at 73V—with the average steps being approximately 5 ADC counts. As the HV bias increases, the steps quickly became indistinguishable. Operating the MPPC in this region will result in a much higher probability of crosstalk. Crosstalk occurs when a photon incident on a single pixel, on the MPPC, can trigger avalanche effects from neighboring pixels. This effect must be identified and removed from any data sets before analysis. An estimation of crosstalk probability can be calculated using the ratio between the width of a step versus the difference in trigger rates between two steps. From Figure 5.8b the crosstalk probability between the two distinguishable step is \sim 40 percent, which is not ideal, since this will effectively reduce the event efficiency by 40 percent even before any further analysis.

In comparing the STD from Figure 5.8a against the width of an average step from Figure 5.8b, the approximate Signal to Noise Ratio (SNR) was less than 2. With a SNR this low, distinguishing single PE events using the RC gain circuit will be challenging even after pedestal subtraction. Detecting single PE events is a major facet to the accurate calibration of any MPPC/SiPM-based detector, for that reason a second revision of the Next Gen center DCs will be designed that will replace the RC gain circuit with low power amplifiers.

5.6 Future Works

Based on the results from the RC gain circuit evaluation, a second revision of the center DCs needs to be designed to include low power amplifiers on each channel in the detector. Once the second prototype is fabricated, assembled, and tested, Stage Two of testing can begin. In this stage, the tracker planes will be placed into the HMB enclosure to take initial data needed for Monte Carlo simulations at various thicknesses of PVT scintillating plates. From the results of the simulations a second PVT scintillating plate can be made and compared with the initial 1 cm thick plate. Once the optimal scintillating plate thickness is found the end-cap DC, power boards, supporting structure, and final cylindrical scintillating planes of the Next Gen BMD can be designed, fabricated, and assembled. At that point, electrical and functionality testing of the entire BMD system has to be done. If all electrical and functions test pass, then the calibration, pedestal subtraction, sine wave reconstruction, and LED pulser tests need to be done to ensure full operations of the Next Gen BMD before field deployment. The final step of the BMD is to develop software that will handle the analysis of the data to reconstruct muon path and relevant information.

CHAPTER 6

CONCLUSION

Using the 1st Gen of the BMD as a foundation, the Next Gen BMD has made steps towards the true goal of the BMD project, which is to design a deployable, low-power detector that will fit entirely inside a 17.78 cm (7 in) borehole. With the completion of the center DC and the results from the event readout, pedestal subtraction, LED pulsar, sine wave reconstruction tests the functionality of the firmware and software is at a operational level. Although from the RC gain circuit evaluation, it is clear that an amplifier stage is needed to amplify the signal from the MPPC so that the pluses are distinguishable from the intrinsic noise of the electronics.

With the lessons learned from testing the first prototype of the center DC and the new scintillating plates, moving forward into the next stages of the Next Gen BMD as mentioned in the future works section a fully deployable detector is not far off.

BIBLIOGRAPHY

- [1] John Perry. Advanced applications of cosmic-ray muon radiography, 2013.
- [2] Hiroyuki K.M. Tanaka, Toshiyuki Nakano, Satoru Takahashi, Jyunya Yoshida, Minoru Takeo, Jun Oikawa, Takao Ohminato, Yosuke Aoki, Etsuro Koyama, Hiroshi Tsuji, and Kimio Niwa. High resolution imaging in the inhomogeneous crust with cosmic-ray muon radiography: The density structure below the volcanic crater floor of mt. asama, japan. *Earth and Planetary Science Letters*, 263(1):104 – 113, 2007.
- [3] H. Tanaka, K. Nagamine, N. Kawamura, S. N. Nakamura, K. Ishida, and K. Shimomura. Development of the cosmic-ray muon detection system for probing internal-structure of a volcano. *Hyperfine Interactions*, 138(1):521–526, Dec 2001.
- [4] N. Lesparre, D. Gibert, J. Marteau, Y. Dclais, D. Carbone, and E. Galichet. Geophysical muon imaging: feasibility and limits. *Geophysical Journal International*, 183(3):1348–1361, 2010.
- [5] Alain Bonneville, Richard T. Kouzes, Jared Yamaoka, Charlotte Rowe, Elena Guardincerri, J. Matthew Durham, Christopher L. Morris, Daniel C. Poulson, Kenie Plaud-Ramos, Deborah J. Morley, Jeffrey D. Bacon, James Bynes, Julien Cercillieux, Chris Ketter, Khanh Le, Isar Mostafanezhad, Gary Varner, Joshua Flygare, and Azaree T. Lintereur. A novel muon detector for borehole density tomography. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 851:108 – 117, 2017.
- [6] S. Funk, D. Jankowsky, H. Katagiri, M. Kraus, A. Okumura, H. Schoorlemmer, A. Shigenaka, H. Tajima, L. Tibaldo, G. Varner, A. Zink, J. Zorn, and for the CTA consortium. Target: A digitizing and trigger asic for the cherenkov telescope array. *AIP Conference Proceedings*, 1792(1):080012, 2017.
- [7] Many muons: Imaging the underground with help from the cosmos, Dec 2016.
- [8] Hamamatsu Photonics K.K. Mppc s13360-1350cs, 2016.
- [9] SaintGobain. Plastic scintillating fibers, 2017.
- [10] SaintGobain. Bc-600 optical cement, 2016.
- [11] M. Andrew, C. Lim, K. Nishimura, L. Ridley, and G. Varner. 128 channels of multi-gigasample-per-second waveform sampling and digitization in a 10 cm x 10 cm x 8 cm package. In *2012 18th IEEE-NPSS Real Time Conference*, pages 1–5, June 2012.