Nathan Godwin

nathanrgodwin@gmail.com | (530) 470-3328 | www.nathanrgodwin.com
github.com/nathanrgodwin | linkedin.com/in/nathanrgodwin

Education

Electrical Engineering, MS, UC San Diego (Expected December 2018)
Area of Focus: Machine Learning, Digital Logic Design
Electrical Engineering, BS, UC San Diego (June 2017), GPA 3.6
Area of Focus: Signal and Image Processing, Circuit Design

Experience

Cymer **FPGA Intern**
San Diego, CA **6/2016-Present**

- Developed an automated design verification system in Python for timing and energy monitoring FPGAs for extreme-ultraviolet laser systems.
- Reduced the on-bench hardware testing time from eight hours to one hour.
- Created a self-checking SystemVerilog verification system for timing and energy FPGA system.

Digital Acoustics **Independent Contractor**
Grass Valley, CA **2/2013-9/2015**

- Designed a script for automated FIR filter generation and correction in VHDL and MATLAB.
- Performed analysis of frequency shift keyed and minimum shift keyed signals.
- Created VHDL systems for data pipelining and system control on FPGAs.
- Developed systems for projects such as the JJY atomic clock timing transmitter, the ITER fusion experiment, and very-low-frequency submarine transmitters.

Intern
10/2012-1/2013

- Performed bench-testing for jitter on fiber-optic systems.
- Generated verification test benches and simulations for FPGA systems.
- Developed data transfer systems in VHDL for transmitter control systems.

Projects

Laser Cutter

- A CNC laser cutter system constructed from two CD drives and supporting circuitry. The GUI and control system was designed in Java and the motor controller was designed in C++.

8-bit NAND Computer

- An 8-bit general purpose computer built primarily from NAND gate chips. Custom instruction set and micro-architecture with a focus on gate minimization. SystemVerilog, Python, Eagle for PCB design, and Assembly were used in this project for design and testing.

Autonomous Line-Following Car

- Designed motor driver, PCB, and control software for a small autonomous car with a team. Received 3rd place at UCSD's GrandPrIEEE and 4th at UC Davis' NATCAR competitions.

SVM Classifier

- A Support Vector Machine design in MATLAB. Converts training set to dual problem with appropriate offset, employs kernel trick for non-linear datasets, and classifies test set.

Skills

- MATLAB, C, Java, VHDL, Verilog, SystemVerilog, SPICE simulation, Python, Assembly, and C++.
- Analog and digital circuit design, digital IC design and verification, computer architecture, and FPGA programming.
- Digital filter design for finite- and infinite-impulse response filters.

Leadership

- UCSD IEEE Quarterly Projects Chair: 1/2016 – 6/2016
  - Managed ten teams for ten-week-long projects.
  - Developed technical workshops and provided programming and circuit design assistance.