Nathan Godwin

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Education

Electrical Engineering, MS, University of California, San Diego (Expected December 2018)
Electrical Engineering, BS, University of California, San Diego (Expected June 2017), GPA 3.63
Natural Science, AA, Sierra College (June 2013), GPA 3.84
Area of Focus: Signal and Image Processing, Circuit Design

Experience

Cymer **FPGA Intern**
San Diego, CA **6/2016-9/2016**

- Developed an automated design verification system in Python for timing and energy monitoring FPGAs for extreme-ultraviolet laser systems.
- Reduced the on-bench hardware testing time from eight hours to one hour.

Digital Acoustics **Independent Contractor**
Grass Valley, CA **2/2013-9/2015**

- Designed and implemented a system for automated FIR filter generation and correction in VHDL and MATLAB.
- Performed analysis of frequency shift keyed and minimum shift keyed signals.
- Created VHDL systems for data pipelining and system control on FPGAs.
- Contributed to projects such as the JJY atomic clock timing transmitter, the ITER fusion experiment, and very-low-frequency submarine transmitter systems.

Intern
10/2012-1/2013

- Performed bench-testing for jitter on fiber-optic systems.
- Generated simulations for FPGA systems.
- Developed data transfer systems in VHDL for transmitter control systems.
- Created block diagrams and documentation for transmitter control systems.

Personal Projects

Laser Cutter

- A CNC laser cutter system constructed from two CD drives and supporting circuitry. The GUI and control system was designed in Java and the motor controller was designed in C++.

8-bit Signed Multiplier Integrated Circuit

- A SystemVerilog RTL design of an 8-bit multiplier using a carry-save array and a radix-4 booth multiplier. The netlist was created with Synopsys Design Vision, and Place and Route and appropriate optimization was performed with Cadence Innovus.

Autonomous Line-Following Car

- Designed a motor driver and overall system architecture for a $1/12^{th}$ scale autonomous car.

Skills

- MATLAB, C, Java, VHDL, Verilog, SystemVerilog, SPICE simulation, Python, Assembly, and C++.
- Analog and digital circuit design and analysis including digital IC design, RTL verification, computer architecture, and FPGA programming.
- Digital filter design for finite- and infinite-impulse response filters.

Leadership

- UCSD IEEE Quarterly Projects Chair: 1/2016 – 6/2016
  - Managed ten teams for ten-week, fast-paced projects.
  - Developed two technical workshops and provided programming and circuit design assistance.