	cycle	instruction retitred	reason
	1	-	
	2	-	
	3	-	
	4	-	
	5	lbi r0	
	6	lbi r5	
	7	lbi r6	
	8	lbi r7	
	9	ld r1 r0 0	
	10	nop	*st r5 r1 0* is stalled until *ld r1 r0 0* can write r1, avoid RAW hazard, st instr begins decoding at cycle 10
	11	nop	st instr begins executing at cycle 11
	12	nop	st instruction begins memory stage at cycle 12
	13	st r5 r1 0	st instruction retired after inserted nops
	14	ld r1 r0 2	
	15	nop	*st r6 r1 1* is stalled until *ld r1 r0 2* can write r1, avoid RAW hazard, st instr begins decode stage at cycle 15
	16	nop	st instr begins execute stage at cycle 16
	17	nop	st instruction begins memory stage at cycle 17
	18	st r6 r1 1	st instruction retired after inserted nops
	19	ld r1 r0 4	
	20	nop	*st 75 r1 1* is stalled until *ld r1 r0 4* can write r1, avoid RAW hazard, st instr begins decoding at cycle 20
	21	nop	st instr begins execute stage at cycle 21
	22	nop	st instruction begins memory stage at cycle 22
	23	st r7 r1 1	st instruction retired after inserted nops
	24	halt	
	25	nop	wait until last instruction retired before dumbing memory
	26	nop	wait until last instruction retired before dumbing memory
	27	nop	wait until last instruction retired before dumbing memory
	actual cycles in processor: 27		