CMOS Project Report
Delay Measurement Device

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1 Introduction

1.1 Specifications

The goal of this project is to design and simulate a delay measurement device using components available through the AMS C35 0.35 µm CMOS process. In order to measure the length of a long cable, a voltage pulse is applied to one end of the cable and the length is deduced from the time it takes to reach the other end.

The output of the device must scale with the delay between two voltage pulses, which can range between 10 ns and 500 ns. The pulses themselves are chosen to be 10 ns long, and the device must be able to drive a 10 pF capacitive load.

1.2 Basic Block Diagram

To achieve this, the device is organized as shown in figure 1.

Figure 1: Block diagram overview.

At the core is the block `rampgen` which generates a rising ramp on its analog output *measure* when the digital input *charge* is HI , maintains its output when *charge* is LO , and resets it to ground when the digital input *start* is HI .

It is the controlled by the first block, `logic` , which controls *charge* based on the succession of pulses on its digital inputs *start* and *stop* and some internal logic.

The output of `rampgen` is buffered by the output stage `buffer` which is able to drive the specified load of 10 pF.

In the next three sections, the design of each of these blocks is reviewed. Then, in the last section, the operation curves of the whole are presented.