

Nathan J. Zhang

natjiazhan@gmail.com

natjiazhan.github.io // github.com/natjiazhan

PROFILE	Electrical engineering student at Arizona State University with a strong foundation in digital design, signal processing, and HDL programming. Experienced in FPGA development (SystemVerilog, Quartus Prime), circuit analysis.	
EDUCATION	B.S. Electrical Engineering , Arizona State University - Barrett Honors M.S. Electrical Engineering Arizona State University GPA: 3.8/4.0 Relevant Coursework <ul style="list-style-type: none">HDL, Digital Design, Circuits I & II, Signals and Systems, Random Signal Analysis, Programming Principles, Electromagnetics	Expected May 2027 Expected May 2027
EXPERIENCE	ASU Bioinformatics Research Group - Research Assistant <ul style="list-style-type: none">Assembled FED-3 behavioral feeder for rodent-based experiments; integrated Arduino control scripts for behavioral conditioning (Pavlovian, exponential, incremental).Authored a technical guide and presentation on device implementation in field settings. Qubit by Qubit Quantum Computing Program - Student Researcher <ul style="list-style-type: none">Developed quantum algorithms using Qiskit, including Grover's Search and VQE simulations for molecular modeling.Implemented quantum key distribution protocols and linked foundational quantum mechanics with programming techniques in Python.Conducted experiments on IBM's real quantum hardware via cloud access. HarvardX/edX - Data Science Program <ul style="list-style-type: none">Completed modules on R programming, data visualization, probability, inference, and productivity tools as part of Harvard's professional data science certificate series.Certificate IDs: R Basics, Visualization, Probability, Inference and Modeling, Productivity Tools	2022 2022 2022
PROJECTS	FPGA-Based Digital Systems - DE0-CV Board (Altera Cyclone V) <ul style="list-style-type: none">Used SystemVerilog and Quartus Prime to design, simulate, and implement digital systems on the DE0-CV FPGA. Projects included a 2x1 multiplexer and 7-segment decoder, a mod-100 up/down counter with adjustable timing via FSM control, and a configurable 24-hour alarm clock with LED-based alerts and debug modes.Designed and implemented a custom microprocessor with an instruction set supporting arithmetic, jumps, and immediate loads, including a register file, ALU, and instruction memory.Used VGA signal generation to display an animated game, demonstrating pixel timing and raster synchronization. Club Leadership: Led events and managed organizational logistics for over 100+ Chinese American Student Association members as club president	
SKILLS	Technical SystemVerilog, Quartus Prime, FPGA Design, Linux, Digital Logic, Python, Java, Circuit Analysis, Arduino, Qiskit, SPICE, MATLAB (basic), L ^A T _E X Tools Oscilloscope, Multimeter, SEM, TEM, XPS, FIB, AES, Function Generator Languages English (native), Mandarin (fluent) Interests Semiconductors, Machine Learning, Embedded Systems, Computer Architecture, Quantum Computing	