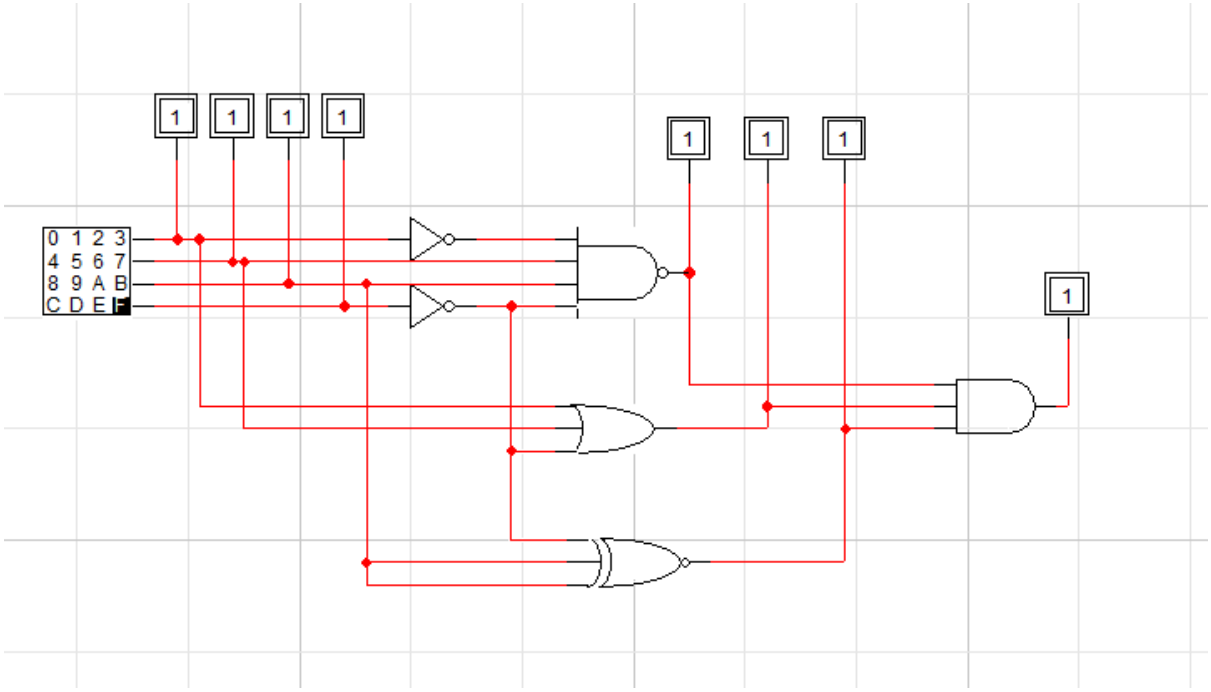
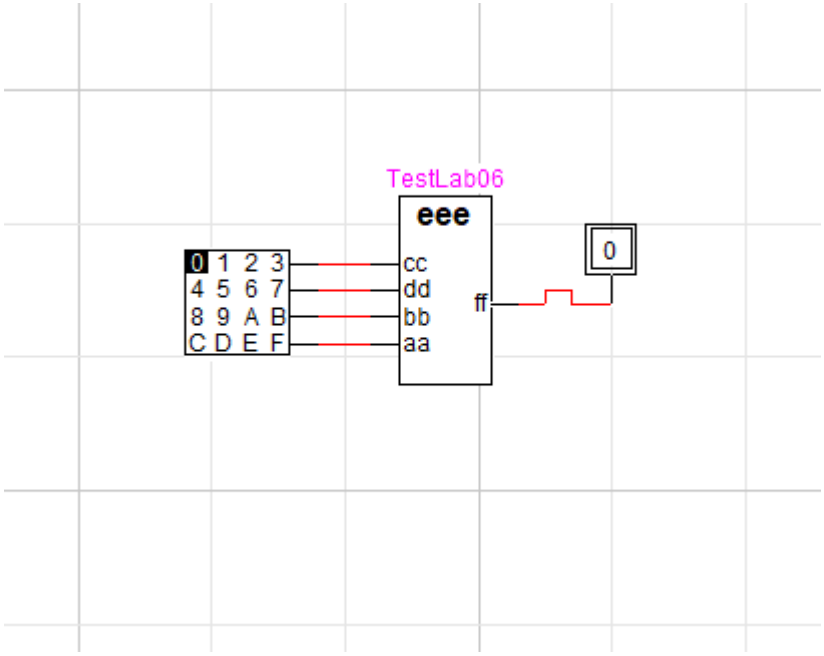
printOut_2/3



printout_3/3




```
library IEEE;
use IEEE.std_logic_1164.all;
entity eee is
 port(
                aa      : in    std_logic;
                bb      : in    std_logic;
                dd      : in    std_logic;
                cc      : in    std_logic;
                ff      : out   std_logic
        );
end eee;
architecture arch1 of eee is
begin
ff <= (not bb and not aa)or(not cc and not aa)or(dd and bb and not aa)after 10ns;
  -- Your VHDL code defining the model goes here
end arch1;
```