Chapter 1

VLSI Fabrication Technology

INTRODUCTION

During the first half of 20th century, electronic circuits used large, expensive, power hungry and unreliable vacuum tubes. In 1948, John Bardeen and Walter Brattain built the first functioning point contact transistor at Bell Laboratories. It was nearly classified as a military secret, but Bell Labs publicly announced the device in the following year.

In 1958, Jack Kilby at Texas Instruments realized the potential for miniaturization if multiple transistors could be built on a single piece of silicon.

The invention of the transistor earned the Nobel Prize in Physics in 1956 for Bardeen, Brattain and their co-worker. Kilby received the Nobel Prize in Physics for the invention of the integrated circuit. Soon after the point contact transistor, Bell Labs developed the bipolar junction transistor. Bipolar transistors were more reliable, less noisy and more power-efficient. Early Integrated Circuits primarily used bipolar transistors. Transistors can be viewed as electrically controlled switches with a control terminal and two other terminals that are connected or disconnected depending on the voltage applied to the control. Bipolar transistors require a small current into the control (base) terminal to switch much larger currents between the other two (emitter and collector) terminals. The power dissipated by these base currents limits the maximum number of transistors that can be integrated onto a single die.

Metal Oxide Semiconductor Field Effect Transistor (MOSFETs) offers the advantage that they draw almost zero control current while idle. They come in two flavors: nMOS and pMOS, using n-type and p-type dopants, respectively.

Frank Warilass at Fairchild described the first logic gates using MOSFETs in 1963. His gates used both nMOS and pM0S transistors, earning the Complementary Metal Oxide Semiconductor (CMOS). The circuits used discrete transistors but consumed only nanowatts of power.

With the development of the silicon planar process MOS integrated circuits became attractive for their low cost; because each transistor occupied less area and the fabrication process was simpler. Early processes used only pMOS transistors and suffered from poor performance, yield and reliability. Processes using nMOS transistors became dominant in 1970s. While the nMOS process was less expensive than CMOS, nMOS logic gates still consumed power when it is in idle. Power consumption became a major issue in 1980's as thousands of transistors were integrated onto a single die. CMOS processes were widely adopted and have essentially replaced nMOS and bipolar processes for nearly all digital logic applications.

Gorden Moore observed in 1965 that plotting the number of transistors that can be made economically fabricated on a chip gives a straight line on a semi logarithmic scale. He found transistor count doubling every 18 months. This observation has been called Moore's Law.

The evolution of IC technology is measured by the number of components integrated on a single chip. The IC industry has gone through the milestones of small scale integration (SSI), medium scale integration (MSI), large scale integration (LSI), and very large scale integration (VLSI).

The following table shows the approximate number of transistors available on a single chip in each of these periods.

Integration Scale	Number of components	Examples
SSI	< 10 transistors	Logic gates
MSI	10 - 1,000 transistors	Adders, counters
LSI	1,000 - 10,000 transistors	8 bit Microprocessors
VLSI	> 10,000 transistors	Advanced Microprocessors

In this chapter, the fabrication issues of the CMOS technologies were discussed.

Process technologies used in today's design Environment

The mainstream process technology used in today's chip design/manufacturing environment is Complementary Metal Oxide Semiconductor (CMOS) technology. Other technologies include bipolar, BiCMOS, Silicon on Insulator (SU) and Gallium Arsenide (GaAs. The majority of integrated circuits manufactured are CMOS circuits. This is due to three characteristics of CMOS devices:

- High noise immunity,
- Low static power and
- High density.

The CMOS process has consistently advanced to smaller feature sizes over the years allowing more circuitry to be packed in one chip as described by Moore's law.

VLSI chips are manufactured on semiconductor material whose electrical conductivity lies between that of an insulator and a conductor. The electrical properties of semiconductors can he modified by introducing impurities through a process known as doping. The ability to control conductivity in small and well defined regions of semiconductor material has led to the development of semiconductor devices. Combined with simple passive components (resistors. capacitors and inductors) they are used to create a variety of electronic devices. The electronic circuits are gradually, created on a wafer of pure semiconductor material such as silicon in a step by step manner. Let us discuss main processing steps in detail in this chapter.

1. WAFER MANUFACTURE

Silicon is the second most abundant element in the earth's crust, however, it occurs exclusively in compounds. The most common is silica (impure SiO_2). Modern ICs must be fabricated on ultrapure defect free slices of single-crystalline silicon, called wafers. A wafer is the circular silicon base upon which chips are

manufactured. It is made from an ingot, which is a cylindrical single crystal semiconductor typically resulting from the Czochralski crystal growth process.

Wafer production requires three general processes:

- Silicon refinement,
- Crystal growth and
- Wafer formation

Silicon Refinement

Metallurgical Grade Silicon (MGS)

Silicon refinement begins with the reduction of silica in an arc furnace at roughly 2000°C with a carbon source. The carbon effectively "pulls" the oxygen from the SiO_2 molecules, thus chemically reducing the oxide to roughly 98% pure silicon, referred to as Metallurgical Grade Silicon (MGS). The overall reduction is governed by the following equation

SiO_2 (solid) + SiC (solid) → Si (solid) + SiO (gas) + CO (gas) (1)

Electronic Grade Silicon (EGS)

MGS is not pure enough for microelectronic device applications because the electronic properties of a semiconductor such as silicon are extremely sensitive to impurity concentrations. It is, therefore, necessary to further purify the MGS into Electronic-Grade Silicon (EGS). Silicon is pulverized and treated with hydrogen chloride (HCl) to form trichloro silane ($SiHC1_3$). The overall reduction is governed by the following equation;

$SiHCl_3 + H_2 \rightarrow$ Si (solid) + 3HCI (gas)

A Si rod is used to nucleate the reduced Si obtained from the silane gas, as shown in figure 1. During the conversion of silicon to trichlorosilane impurities are removed and process can be cycled to increase purity of the formed Si. The final material obtained is the EGS. This is a polycrystalline form of Si, like MGS, but has much smaller impurity levels, closer to what is desired in the final single crystal wafer. EGS is still polycrystalline and needs to be converted into a single crystal Si ingot for producing the wafers.

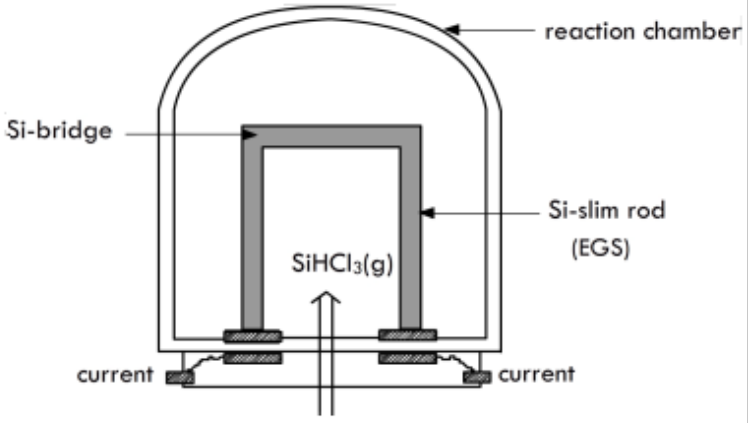

FIGURE 1 Deposition Reactor

Single crystal Si manufacture

There are two main techniques for converting polycrystalline EGS into a single crystal ingot, which are used to obtain the final wafers.

1. Czochralski technique (CZ) - this is the dominant technique for manufacturing single crystals. It is especially suited for the large wafers that are currently used in IC fabrication.

2. Float zone technique - this is mainly used for small sized wafers. The float zone technique is used for producing specialty wafers that have low oxygen impurity concentration.

Crystal Growth

The Czochralski Technique

1. The Czochralski technique uses an apparatus known as crystal puller as shown in Fig.2. In the crystal growth process EGS is placed in the crucible and the furnace is heated above the melting temperature of the silicon.

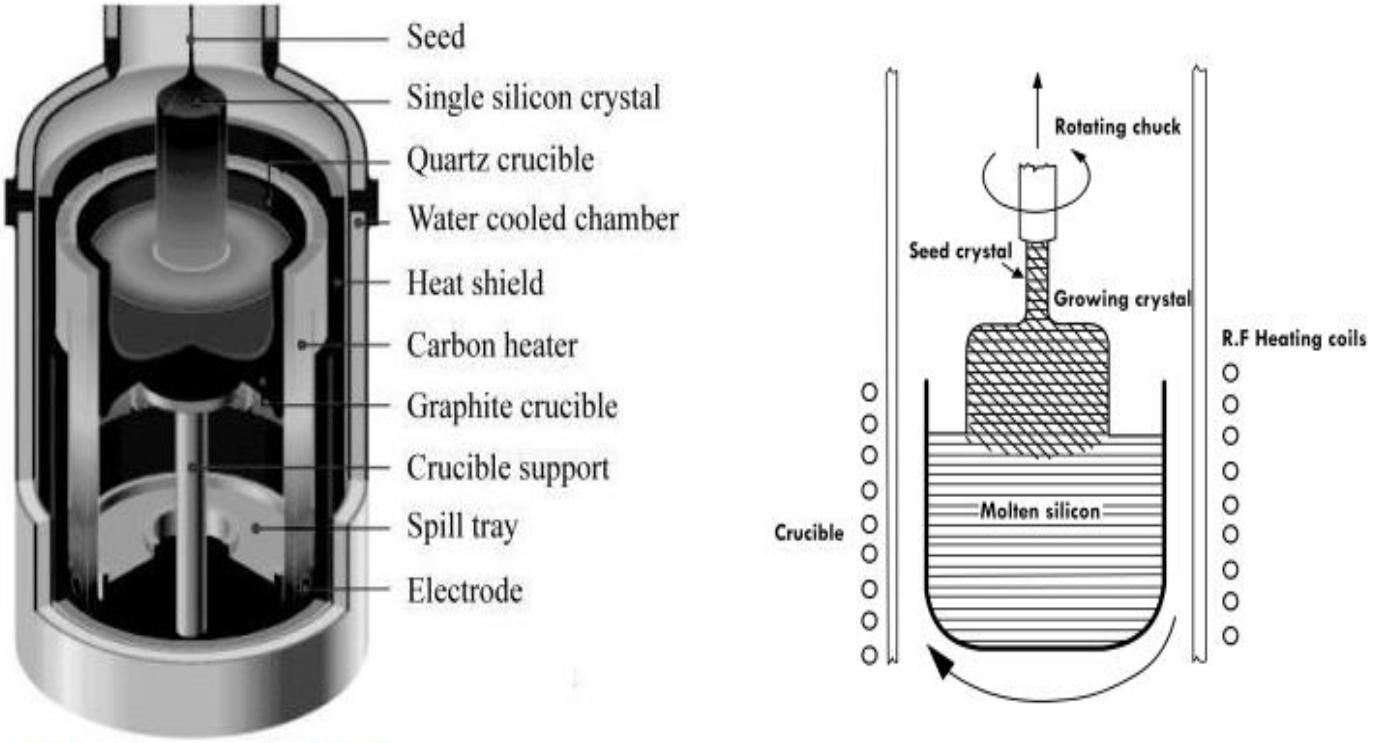

Fig 2 Czochralski Crystal puller

2. Dopant impurity atoms such as boron or phosphorus may be added to the molten intrinsic silicon to dope the silicon, thus changing it into n-type or p-type extrinsic silicon. This influences the electrical conductivity of the silicon.
3. A seed crystal mounted on a rod is dipped into the molten silicon. This seed crystal rod is continuously pulled upwards and rotated at the same time.
4. By controlling the temperature, the rate of pulling, and the speed of rotation, a large single crystal, cylindrical ingot can be extracted from the melt. This process is normally performed in an inert atmosphere (such as argon) and in the chamber made of an inert material (such as quartz).

Float zone technique

The float zone technique is suited for small wafer production, with low oxygen impurity. The schematic of the process is shown in figure 2a. A polycrystalline EGS rod is fused with the single crystal seed of desired orientation. This is taken in an inert gas furnace and then melted along the length of the rod by a traveling radio frequency (RF) coil. The RF coil starts from the fused region, containing the seed, and travels up, as shown in figure 2a. When the molten region solidifies, it has the same orientation as the seed. The furnace is filled with an inert gas like argon to reduce gaseous impurities.

Also, since no crucible is needed it can be used to produce oxygen 'free' Si wafers. The difficulty is to extend this technique for large wafers, since the process produces large number of dislocations. It is used for small specialty applications requiring low oxygen content wafers.

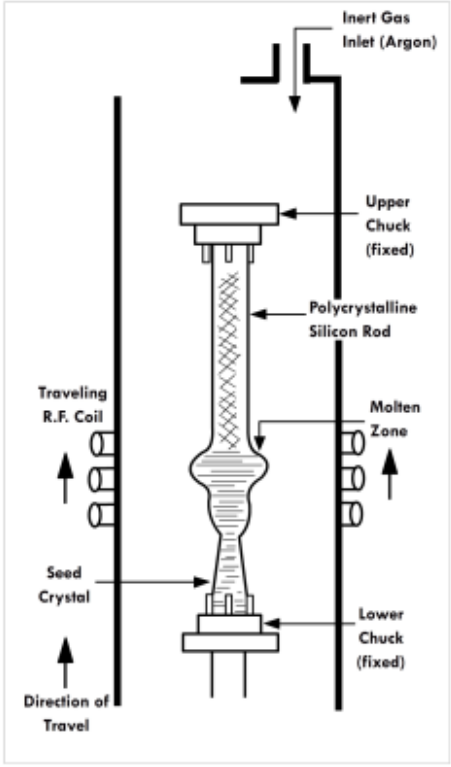

Figure 2a Schematic of the oat zone technique

Wafer Formation

Using high precision diamond saws or diamond wires the ingot is first shaped and then sliced into wafers with thicknesses on the order of 0.5 mm. This wafer fabrication process includes the steps of cutting, grinding, polishing, and cleaning to transform a single crystal rod into many circular wafers for manufacture into semiconductor devices. A wafer is measured by its diameter: 4 inches, 6 inches, 8 inches, or 12 inches.

Inside a wafer, as shown in Fig 2b, there are many small blocks it cells. These individual cells arc called dies or chips. A die is a small piece of silicon material upon which a given circuit is fabricated. The resultant wafer is then cut into pieces, each containing one copy of the desired integrated circuit. Each one of these pieces is a die. Fig 2b shows a wafer with dies.

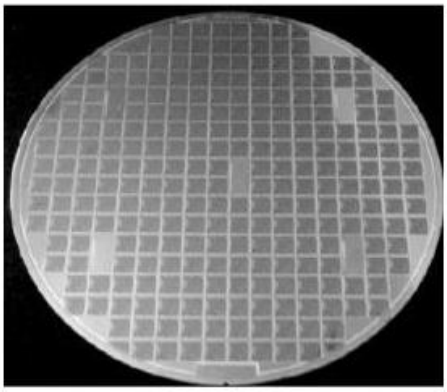

FIG 2b A Wafer with dies

2. WAFER CLEANING

Cleaning will be done in two steps as follows

Wet cleaning steps:

1. Cleaning in ammonia peroxide solution removes organic contamination and particles.
2. Cleaning in hydrogen chloride and hydrogen peroxide mixture removes metallic impurities.
3. Sulphuric acid and hydrogen peroxide mixture removes organics.
4. Hydrogen fluoride removes native oxide from silicon surface.

Dry cleaning steps:

1. Oxygen and Argon plasma treatments to remove unwanted surface layers, or hydrogen bake at elevated temperature to remove native oxide before epitaxy.

3. DOPING OF IMPURITIES

In order to fabricate semiconductor devices, a controlled amount of impurities has to be introduced (doped) selectively into the single crystal wafers. There are three basic methods used for controlled doping of a semiconductor. They are

- Epitaxy
- Diffusion and
- Ion implantation

Epitaxy

The term epitaxy literally means ¯arranged upon". In this process, a thin layer of single crystal semiconductor (typically a few nanometers to a few microns) is grown on an already existing crystalline substrate such that the grown film has same lattice structure as the substrate.

There are basically two types of epitaxy:

a) Homo Epitaxy: in which the same material as that of substrate is grown. Example is growing Si on silicon substrate.
b) Hetero Epitaxy: in which a different layer is grown over the substrate. Example is growing AlGaAs on GaAs.

Epitaxy is further classified into

- Vapor phase epitaxy (VPE),
- Liquid phase epitaxy (LPE),
- Molecular beam epitaxy (MBE),

Diffusion

Epitaxial growth takes place throughout the surface that is, it is non-selective. In order to achieve selective doping, the technique most commonly used in silicon processing is called as diffusion. The basic principle underlying this process is that the dopant atoms migrate from a region of high concentration to the region of low concentration. In simple, diffusion is the process of introducing controlled amounts of dopants into the semiconductors. The unwanted regions of diffusion are covered by the masking material while others are left unprotected. Now if the semiconductor is held in an ambience of high dopant concentration and temperature is raised dopant atoms migrate into the unprotected regions of the semiconductor while many semiconductor atoms move out of their regular lattice sites.

A high concentration of dopant atoms are introduced at the silicon surface by a vapor that contains the dopant at a temperature of about 1000°C. At the temperature of l000°C, silicon atoms move out of their lattice

sites creating a high density of vacancies and breaking the bond with the neighboring atoms. The second step is drive in process, used to drive the impurities deeper into the surface without adding any more impurities. Common dopants are boron for P-type layers and phosphorus, antimony, and arsenic for N-type layers.

A typical arrangement of the process of diffusion is shown in Figure 3a. The wafers are placed in a quartz furnace tube that is heated by resistance heaters surrounding it. So that the wafers may be inserted and removed easily from the furnace, they are placed in a slotted quartz carrier known as a boat. To introduce a phosphorus dopant, as an example, Phosphorus Oxychloride.

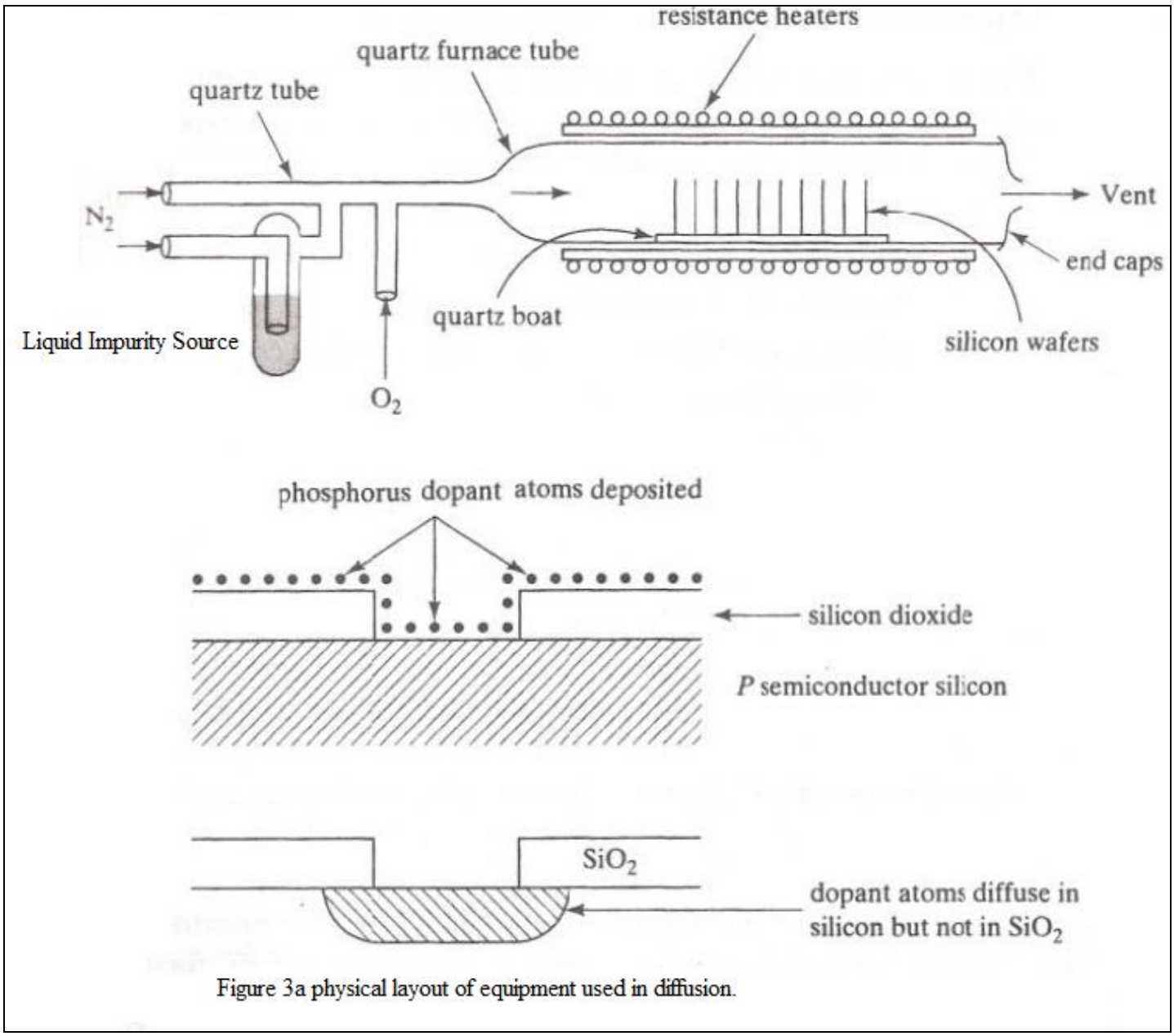

Figure 3a physical layout of equipment used in diffusion.

Phosphorus Oxychloride is placed in a container either inside the quartz tube, in a region of relatively low temperature, or in a container outside the furnace at a temperature that helps maintain its liquid form.

Nitrogen and oxygen gas are made to pass over the container. These gases carry the dopant vapor into the furnace, where the gases are deposited on the surface of the wafers. These gases react with the silicon,

forming a layer on the surface of the wafer that contains silicon, oxygen, and phosphorus. At the high temperature of the furnace, phosphorus diffuses easily into the silicon. Diffusion depth is controlled by the time and temperature of the drive in process.

By precise control of the time and temperature, accurate junction depths of fraction of a micron can be obtained.

Three kinds of situations arise in the process of the diffusion.

- Substitutional diffusion
- Interstitial diffusion

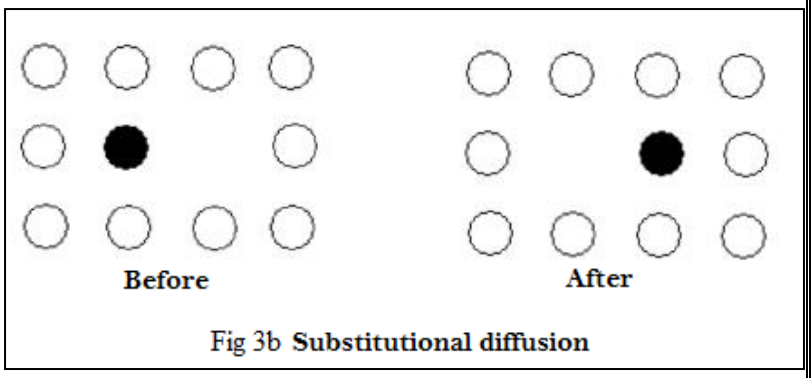

Fig 3b **Substitutional diffusion**

Substitutional diffusion:

An impurity atom wanders through the crystal by jumping from one lattice site to the next, thus substituting for the original host atom. However, it is necessary that this adjacent site be vacant, i.e. vacancies must be present to allow substitutional diffusion to occur. Due to high temperature, silicon atoms get removed from its lattice position in the crystal and the impurity atom takes its place. (Fig.3b)

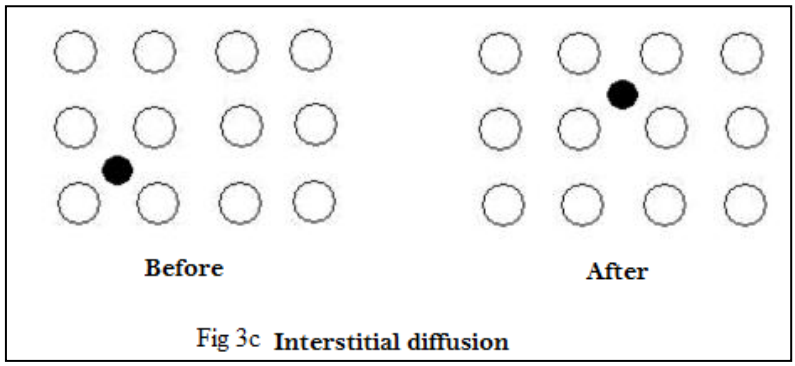

Fig 3c **Interstitial diffusion**

Interstitial diffusion:

An impurity atom moves through the crystal lattice by jumping one interstitial site to the next. Interstitial diffusion requires that jump motion occurring from one interstitial site to another adjacent interstitial state. This process is relatively fast because of large number of vacant interstitial place in the semiconductor crystal

Ion Implantation:

Ion implantation is the other technique used to introduce impurities into a silicon wafer. In this process, silicon wafers are placed in a vacuum chamber and are scanned by a beam of high energy dopant ions as shown in Fig.6. These ions are accelerated by energies between 20 kV to 250 kV. As the ions strike the silicon wafers, they penetrate some small distance into the wafer. The depth of penetration of any particular type of ion increases with increasing accelerating voltage.

Even though ion implantation offers a lot of advantages over diffusion, the process of ion implantation causes lot of damages in the implanted region. This is termed as crystallographic damage and can be thermally annealed in order to make doped regions electronically active.

Annealing can be carried out in a conventional furnace at a temperature range of 800-1000^{O}C for 20 to 30 minutes. This alters the doping profile considerably by driving the dopants inside the silicon substrate. Rapid thermal annealing (RTA) is an alternative technique in which the substrate temperature is suddenly raised to a high value quickly, held constant for a brief period and then cooled down fast. The entire annealing process takes a few seconds to few minutes and the doping profile remains unaltered, RTA is therefore preferred as an annealing technique in present day VLSI technology over conventional furnace annealing.

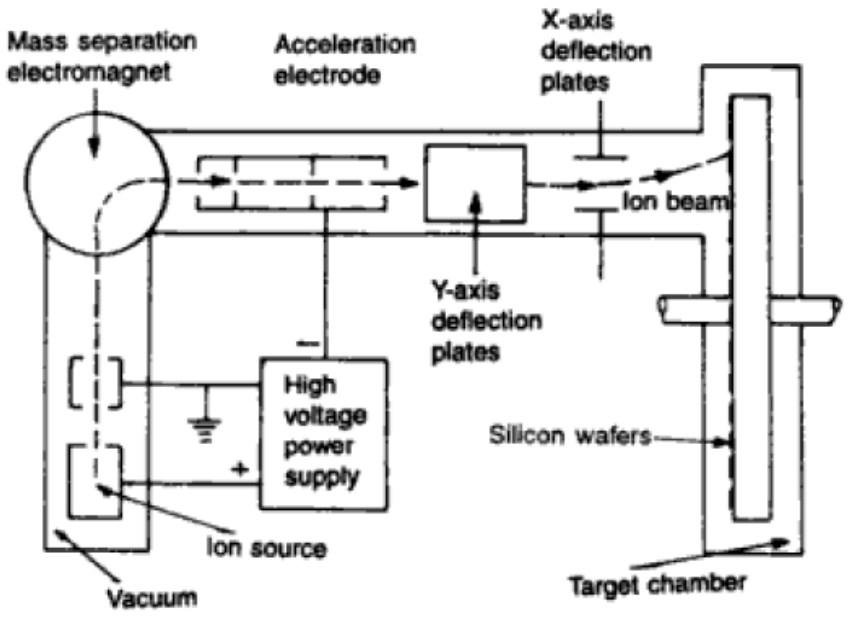

Fig 4 Ion Implantation

Advantages of Ion Implantation:

- Doping levels can be precisely controlled since the incident ion beam can be accurately measured as an electric current.
- The depth of the dopant can be easily regulated by control of the incident ion velocity. It is capable of very shallow penetrations.
- Extreme purity of the dopant is guaranteed.
- The doping uniformity across the surface can be accurately controlled.
- Because the ions enter the solid as a directed beam, there is very little spread of the beam, thus the doping area can be clearly defined.
- Since this is a low temperature process, the movement of impurities is minimized.

Comparison of Diffusion and Ion Implantation

- Diffusion is a cheaper and more simplistic method, but can only be performed from the surface of the wafers. Dopants also diffuse unevenly, and interact with each other altering the diffusion rate.
- Ion implantation is more expensive and complex. It does not require high temperatures and also allows for greater control of dopant concentration and profile. It is an anisotropic process and therefore does not spread the dopant implant as much as diffusion. This aids in the manufacture of self aligned structures which greatly improve the performance of MOS transistors**.**

4. Oxidation

SiO_2 has the property of preventing the diffusion of almost all impurities through it. It serves two very important purposes.

1. SiO_2 is an extremely hard protective coating and is unaffected by almost all reagents except hydrofluoric acid. Thus it stands against any contamination.

2. By selective etching of SiO_2, diffusion of impurities through carefully defined windows in the SiO_2 can be accomplished to fabricate various components.

The silicon wafers are stacked up in a quartz boat and then inserted into quartz furnace tube. The Si wafers are raised to a high temperature in the range of 950 to 1115°C and at the same time, exposed to a gas containing O_2 or H_2O or both.

The chemical reaction is

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

This oxidation process is called thermal oxidation because high temperature is used to grow the oxide layer. The thickness of the film is governed by time, temperature and the moisture content. The thickness of oxide layer is usually in the order of 0.02 to 2 μm.

5. LITHOGRAPHY

Lithography is a process of drawing patterns on a silicon wafer. It involves two processes,

- Making of a photographic mask
- Photo etching

Photomask

The Photomask contains the detailed blueprint of the designed circuit. Using the Photomask, specific images of detailed devices are transferred onto the surface of the silicon wafers by means of photolithography. A Photomask is used just like the negative in photography that captures specific images for later reproduction. A Photomask produces duplicate images or patterns onto the silicon wafers. A single Photomask plate produces identical images on thousands of wafers.

Procedure for pattern transfer:

It consists of the following basic steps:

Preparation of wafer

The wafer is initially heated to a temperature which is sufficient to remove any moisture that may be present on the wafer surface.

Photoresist application

Photoresist, a viscous liquid polymer, is applied to the top surface of the oxidized wafer. The application typically occurs by dropping (or spraying) a small volume of photoresist onto a rapidly rotating wafer, yielding a uniformly thin film on the surface. Following spinning the coated wafer is soft baked on a hot plate, which dries

out most solvents from the photoresist and improves adhesion to the underlying substrate. This is known as pre baking.

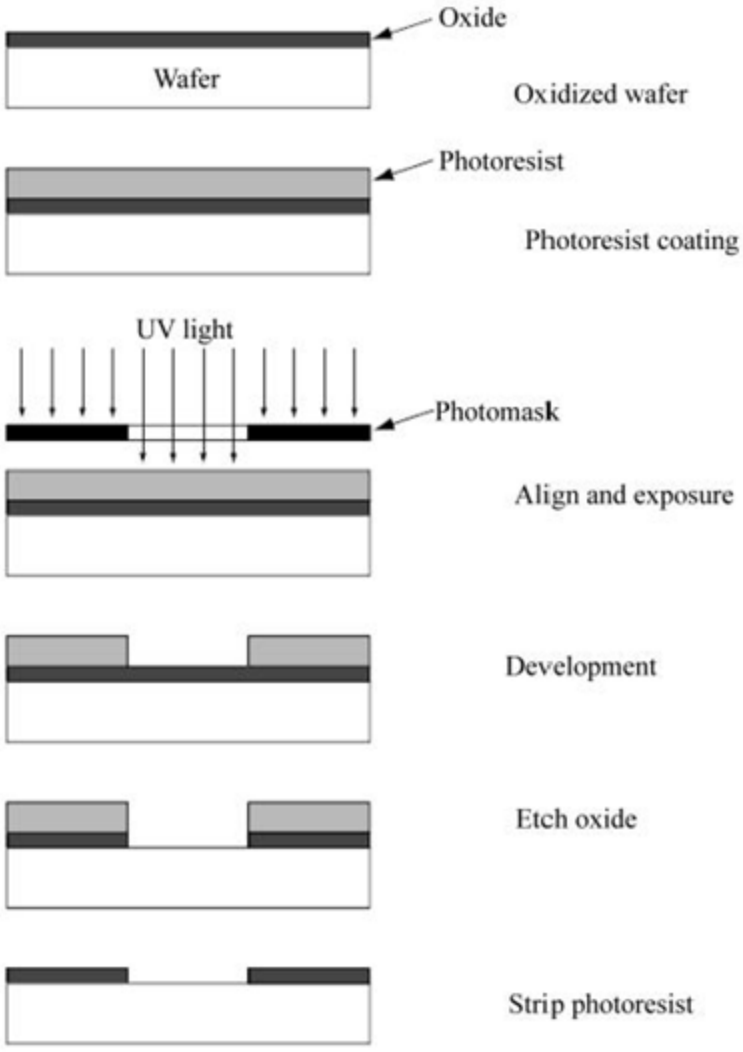

Fig 5 **Steps for photolithography**

Exposing

The wafers are exposed to ultraviolet light through a mask that contains the layout patterns as shown in the Fig.5. After exposure the photoresist absorbs the radiation in the exposed areas from the UV beam and changes its chemical structure. It breaks long chain hands and become soluble in the developer solution.

Developing

A developer solution is a mixture of deionized water and KOH (potassium hydroxide pellets). The wafer is dipped in the developer solution so that the exposed resist areas on the substrate dissolve in the developer solution. This process is called as development.

Baking

The resulting wafer is then "hard-baked", typically at 120 to 180^{O}C, which solidifies the remaining photoresist.

Etching

In the etching step a liquid (wet etching) or plasma (dry etching) chemical agent removes the uppermost laver of the substrate in the areas that are not protected by photoresist.

Photoresist removal

After a photoresist is no longer needed, it must be removed from the substrate. This usually requires a liquid "resist stripper", which chemically alters the resist so that it no longer adheres to the substrate. Alternatively, photoresist may be removed by a plasma containing oxygen, which oxidizes it. This process is called ashing, and resembles dry etching.

6. ETCHING

Etching is the process of removal of the substrate from the unmasked regions so that the desired pattern is transferred on to it. Etching is generally done after lithography. Etching is of two types:

- Wet chemical etching and

- Dry etching

Wet Chemical Etching

It is used extensively in semiconductor processing. Chemical etchants are used for lapping and polishing an optically flat, damage free surface.

Dry Etching

In this type of etching, no wet chemicals are used instead plasma is used hence it can be called as plasma etching. Plasma is ionized gas composed of equal numbers of positive and negative charges and a different number of unionized molecules. It is produced when electric field is applied to a gas, causing gas to break down and become ionized. The process is initiated by free electrons that gain kinetic energy from electric field, collide with gas molecules, and lose energy. The energy transferred causes the gas molecules to be ionized. Free electrons gain kinetic energy from the field, and the process continues. Plasma etching involves chemical reaction combined with physical ion bombardment. Oxygen plasma is generally used for dry etching in semiconductor device fabrication.

7. METALLIZATION

The purpose of this process is to produce a thin metal film layer that will serve to make interconnections of the various components on the chip. Aluminium is usually used for the metallization of most ICs as it offers several advantages

- It is relatively a good conductor.
- It is easy to deposit aluminium films using vacuum deposition.
- Aluminium makes good mechanical bonds with silicon.

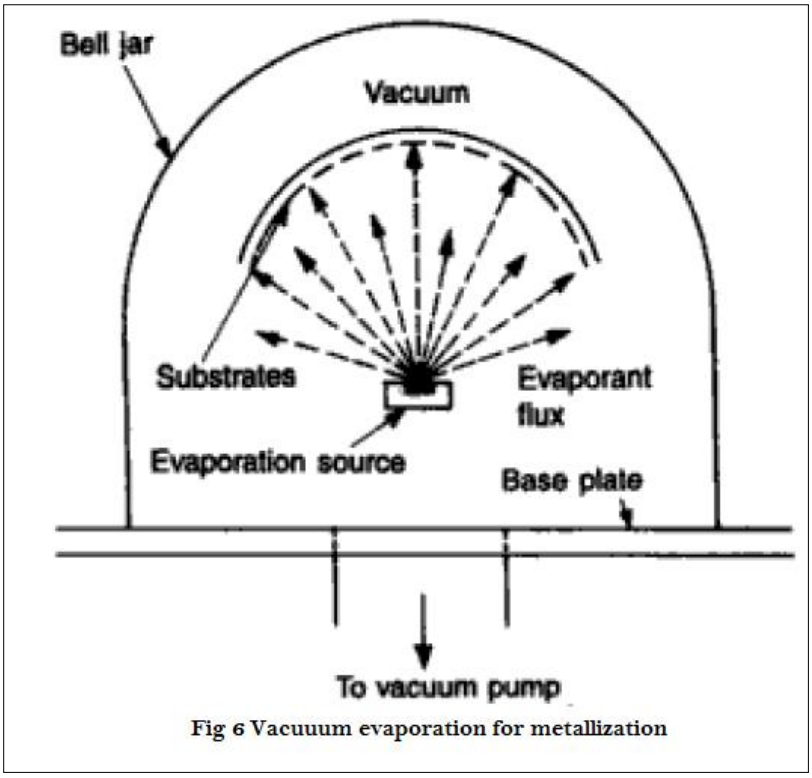

Fig 6 Vacuuum evaporation for metallization

The process takes place in a vacuum evaporation chamber as shown in Fig 6. The pressure in the chamber is reduced to the range of about 10^{-6} to 10^{-7} torr (1 atmosphere = 760 torr = 760 mm Hg). The material to be evaporated is placed in a resistance heated tungsten coil or basket. A very high power density electron beam is focused at the surface of the material to be evaporated. This heats up the material to very high temperature and it starts vaporizing. These vapors travel in straight line paths. The evaporated molecules hit the substrate and condense there to form a thin film coating.

Aluminium is etched away from unwanted places by using etchants like phosphoric acid (H_3PO_4).

8. ASSEMBLY PROCESSING AND PACKAGING

Each of the wafers processed contains several hundred chips, each being a complete circuit. So these chips must be separated and individually packaged. A common method called scribing and cleaving used for separation makes use of a diamond tipped tool to cut lines into the surface of the wafer along the rectangular grid separating the individual chips. Then the wafer is fractured along the scribe lines and the individual chips are physically separated. Each chip is then mounted on a ceramic wafer and attached to a suitable package.

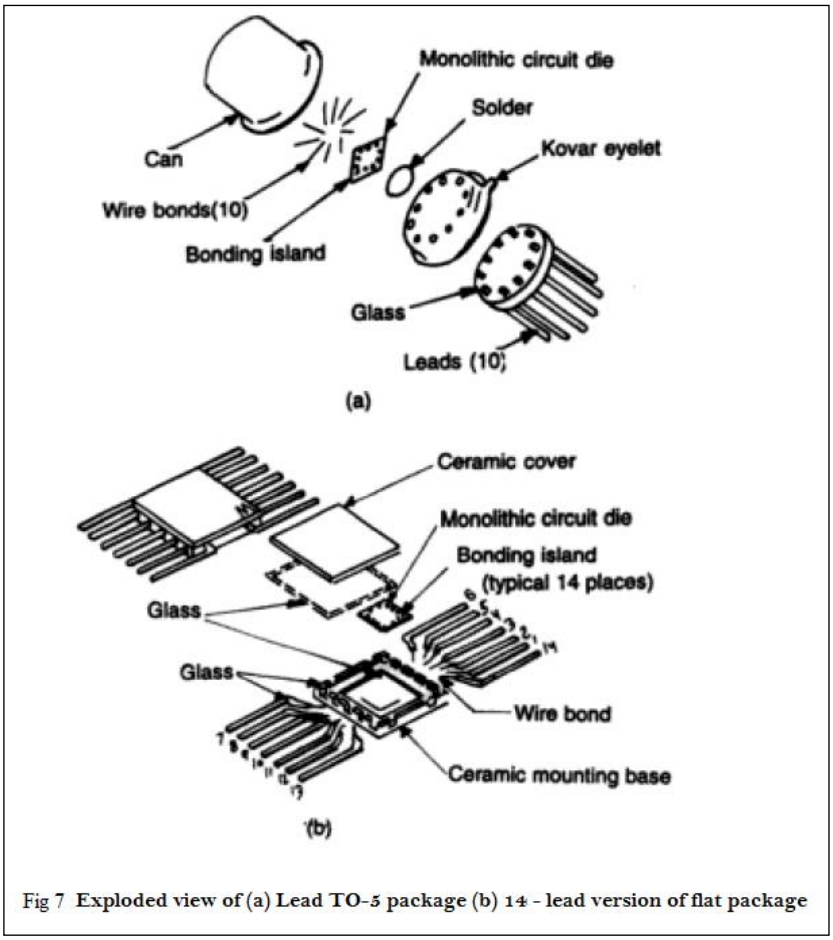

Fig 7 Exploded view of (a) Lead TO-5 package (b) 14 - lead version of flat package

There are three different package configurations available.

- TO-5 glass metal package
- Ceramic flat package
- Dual-in-line (ceramic or plastic type)

TO-5 packages are available in 8, 10 or 12 leads, whereas the flat or dual-in-line package is commonly available in 8, 14 or 16 leads, but even 24 or 36 or 42 leads are also available for special circuits. Ceramic packages, whether of flat type or dual-in-line are costly due to fabrication process, but have the advantage of best hermetic sealing. Most of the general purpose ICs are dual-in-line plastic packages due to economy. Fig7 shows the exploded view of TO-5 and flat package.

FABRICATION OF PASSIVE COMPONENTS

Resistors

Resistors have been available for use in ICs for many years. Some of these are made in silicon, so they are directly integrated with the rest of the IC processes. Usually, resistors in ICs are characterized in terms of their sheet resistance rather than their absolute resistance value. Sheet resistance, R_{sheet} is defined as the resistance of a resistive strip with equal length and width so that

$$R_{sheet} = \frac{\rho}{t}$$

Where p is the material resistivity (Ωm) and t its thickness (m). Once R_{sheet} value is given, the resulting resistor value is obtained by multiplying the number of squares that can be accommodated in the strip.

The resistor may be fabricated at a number of stages during the IC process giving rise to different resistors with different characteristics. Some of the most common are discussed below.

Diffused Resistors:

These can be formed during either the base or emitter diffusion of a bipolar process. For an NPN process the base diffusion resistor is a p-type of moderate sheet resistivity typically in the range of 100-200 Ωm. This can provide resistors in 10-50 kΩ range. The heavily doped n^+ emitter diffusion will produce an n^+ type resistor with low sheet resistivity of 2-10 Ωm. This can provide resistors with low values in 1-100 Ω range.

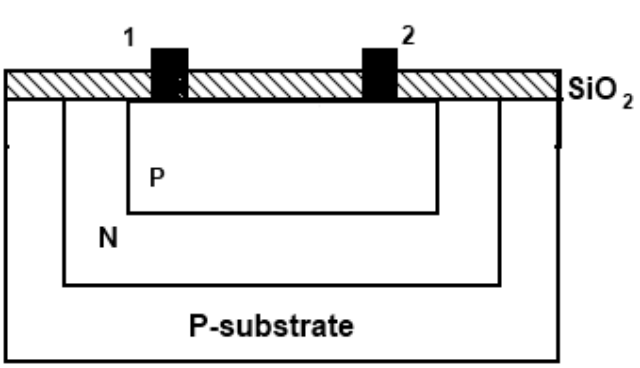

Fig 8 Diffused Resistor

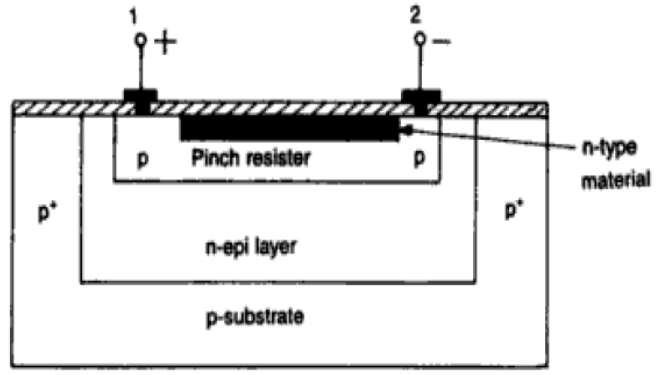

Fig 9 Pinched Resistor

Pinched Resistor:

The sheet resistance offered by the diffusion regions can be increased by narrowing down its cross-sectional area. This type of resistance is normally achieved in the base region. Figure 9 shows a pinched base diffused resistor. It can offer resistance of the order of mega ohms in a comparatively smaller area. In the structure shown, no current can flow in the N-type material since the diode realized at contact 2 is biased in reversed direction. Only very small reverse saturation current can flow in conduction path for the current has been reduced or pinched. Therefore, the resistance between the contact 1 and 2 increases as the width narrows down and hence it acts as a pinched resistor.

Thin Film Resistor:

Vapour thin film deposition techniques can also be used for the fabrication of IC resistors. In this, a very thin metallic film usually of Nichrome (NiCr) of thickness less than 1 μm is vapour deposited on the SiO_2 layer. Using masked etching, desired geometry of this thin film is achieved to obtain suitable values of resistors.

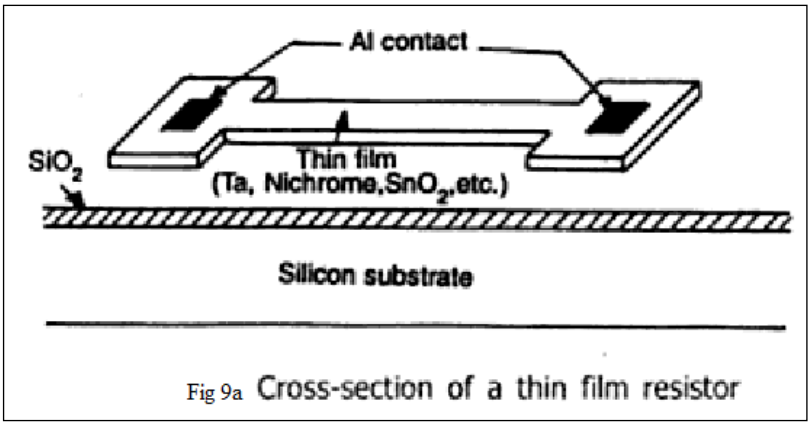

Fig 9a Cross-section of a thin film resistor

These thin film resistors have three distinct advantages over the diffused resistors.

1. Thin film resistors have lesser and smaller parasitic components and hence their high frequency behavior is better.

2. The values of thin-film resistors can be easily adjusted even after fabrication by cutting a part of the resistor with a laser beam (Laser trimming).

3. Thin film resistors have low temperature coefficient, thereby making them more stable.

Higher values of thin film resistors have been obtained by depositing Tantalum over SiO_2 layer. The main disadvantage of thin film resistors is the additional process steps required in their fabrication.

Capacitors:

Most integrated capacitors are either junction capacitors or MOS capacitors.

Junction Capacitors:

A junction capacitor is formed when a pn junction is reverse biased. This can be formed using the base-emitter, base-collector, or collector-substrate junctions of an NPN structure in bipolar ICs. Of course, the particular junction must be maintained in reverse bias to provide the desired capacitance. Since the capacitance arises from the parallel plate effect across the depletion region, whose thickness in turn is voltage-dependent, the capacitance is also voltage dependent decreasing with increased reverse bias. The capacitance depends on the reverse voltage. The base-emitter junction provides the highest capacitance per unit around 1000 pF/mm^2 with a low breakdown voltage (5V). The base-collector junction provides 100 pF/mm^2 with a higher breakdown voltage (40 V).

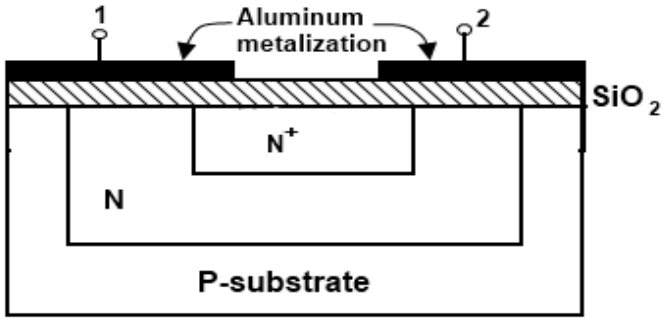

Fig10 Integrated MOS Capacitor

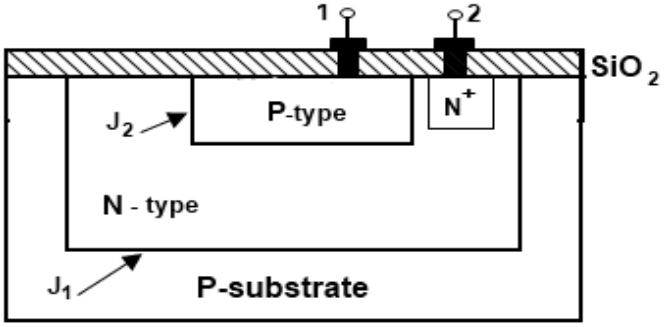

Fig 11 Integrated Junction Capacitor

MOS Capacitors:

MOS capacitors arc usually formed as parallel plate devices with a top metallization and heavily doped n region as the two plates with a thin oxide dielectric sandwiched in between. The oxide is usually a thin layer of SiO_2 with a relative dielectric constant ε_r of 3- 4 or Si_3N_4 with ε_r of 5-8. Since the capacitance obtained is $\varepsilon_o\varepsilon_r A/t_{oxide}$, the oxide thickness is critical. MOS capacitors can provide around 1000 pF/mm^2 with breakdown voltages up to 100 V. Unlike junction capacitors, MOS capacitors are voltage independent and can be biased either positively or negatively. Their breakdown, however, is destructive since the oxide fails permanently. Care should be taken to prevent overvoltage conditions.