

KSZ8863 Daughter Board Information Sheet

Abstract

The KSZ8863 Daughter Board (AC320004-7) enables Ethernet communication with a variety of Microchip starter kits. This information sheet provides an overview and a detailed schematic of the KSZ8863 Daughter Board.

This daughter board is designed specifically to be used with the PIC32 Ethernet Starter Kit II (DM320004-2) or the PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Starter Kit (DM320007); however, it can also be used with other Microchip development hardware.

For additional information about the KSZ8863 Daughter Board, visit Microchip web site: http://www.microchip.com.

1 Features

The KSZ8863 Daughter Board features a 22-pin header for connecting the board into compatible PIC32 starter kits. The board has a KSZ8863 Ethernet Physical Layer Chip, configured to use RMII. The KSZ8863 Daughter Board is suitable for use with the PIC32 Ethernet Starter Kit II and PIC32MZ EF Starter Kit.

The following are features of the KSZ8863 Daughter Board:

- · RMII interface with MDC/MDIO management interface for register configuration
- Fast start-up and link
- · Loopback modes for diagnostics
- Integrated 3-Port 10/100 Managed Switch with PHYs
- IEEE 802.1q VLAN Support
- · Optional SPI interface
- Compliant with IEEE 802.3u standard

2 Applications

- · VoIP Phone
- · Set-Top/Game Box
- Automotive
- · Industrial Control
- IPTV POF
- SOHO Residential Gateway
- Broadband Gateway/Firewall/VPN
- Integrated DSL/Cable Modem

- Wireless LAN Access Point + Gateway
- Standalone 10/100 Switch

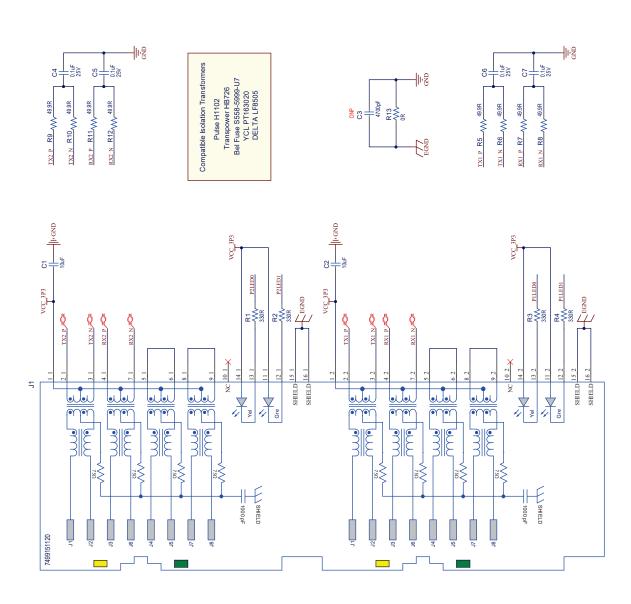
3 Additional Information

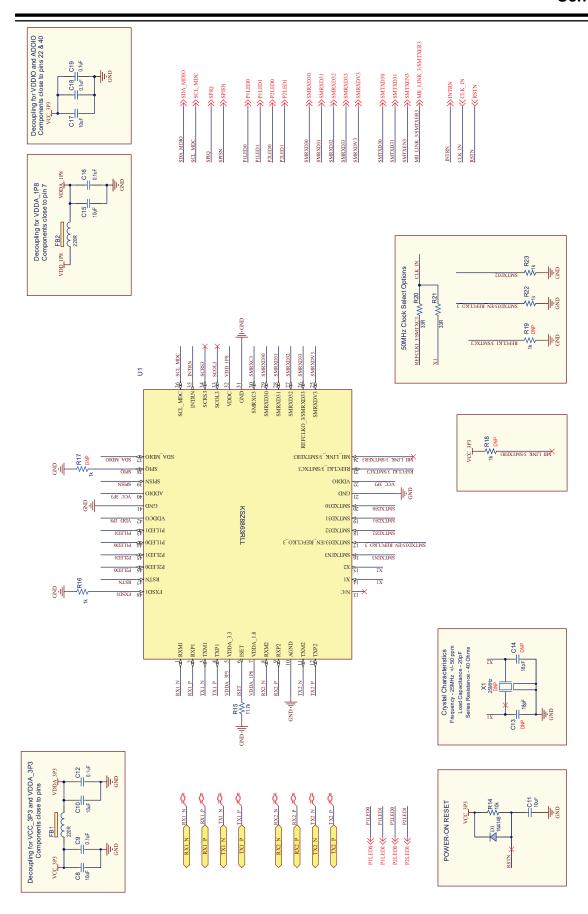
For additional information on drivers and examples, follow these links:

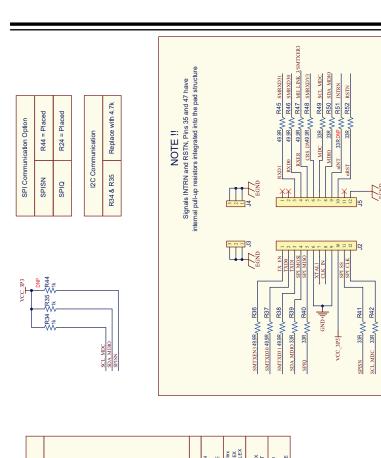
- https://www.microchip.com/wwwproducts/en/KSZ8863
- http://www.microchip.com/mplab/mplab-harmony

1. Schematics









Cle	충	Clock Source Configuration	iguration	
Pin 17 SMTXD33 Pin 18 SMTXD32 /EN_REFCLK0_3 Internal Pull-Up (For Rev A3)	ternal F or Rev	MXD32	Clock Source	Note
(use 1k Pull-Down) (use 1k Pull-Down)	0 e 1k P	ull-Down)	External 50MHz OSC input to SMTXC3/REFCLK[_3 and X1 pin directly	EN_REFCLK0_3 = 0 to Disable REFCLK0_3 for better EMI
1 0 (use 1k P	0 e 1k P	0 (use 1k Pull-Down)	50MHz on X1 pin is clock source. REFCLK0_3 Output is Feedback to REFCLKI_3 externally	EN_REFCLK0_3 = 1 to Ensable REFCLK0_3
1 1	+		25MHz on X1 pin is clock source. REFCLK0_3 Output is connected to REFCLK1_3 externally	EN_REFCLK0_3 = 1 to Ensable REFCLK0_3
0 0 0 0 0 0 1	0 00	_	25MHz on X1 pin, 50MHz RMII Clock goes to SMTXC3/ REFCLKI 3 internally REFCLKI 3 is unconnected	EN_REFCLK0_3 = 0 to Disable REFCLK0_3 for better BMI

Bus Communication Configuration	R29 DNP R29 DN	Serial Bus Configuration	I2C (master mode) EEPROM	I2C Slave Mode	SPI Slave Mode	SMI Mode
Bus Commu	0तत्रारत । तत्रारत	[P2LED1,P2LED0]	[Placed,Placed]	[Placed,DNP]	[DNP,Placed]	[DNP,DNP]

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	R30 DW	PORT 2 - OPTIONS	Force Flow DNP = EN Placed = D	Force Full/H DNP = FULI Placed= HAL	Force S DNP = 100 Placed = 1	Auto-Neg DNP = E Placed = E
Port Configuration Options	SMRXD30 F SMRXD31 F SMRXD33 F SMRXD33 F	PORT 2	SMRXD30	SMRXD31	SMRXD32	SMRXD33
nfigura						
Port Co	R24 ONF IR R25 ONF IR R25 ONF IR R25 ONF IR R27 ONF IR	PORT 1 - OPTIONS	Force Flow Control DNP = ENABLE Placed = DISABLE	Force Full/Half Duplex DNP = FULL DUPLEX Placed= HALF DUPLEX	Force Speed DNP = 100BaseTX Placed = 10BaseT	Auto-Negotiation DNP = ENABLE Placed = DISABLE
	SMRXDV3 PILEDI PILEDI	PORT 1	SPIQ	SMRXDV3	P1LED1	P1LED0

PILEDO

PILEDI

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PILEDO

P2LED1	SPIQ SPISN SDA MDIO SCL MDC	SMRXD30 SMRXD31 SMRXD32 SMRXD33 SMRXD33	SMTXD30 SMTXD31 SMTXEN3 MIL LINK 3/SMTXER3
P2LED1	SPIQ\\ SPA_MDIO\\ SCL_MDC\\	SMRXD31 >>	SMTXD30 >>> SMTXD31 >>> SMTXB13>>> MILLINK_3/SMTXER3 >>>

2. Revision History

Revision B - March 2019

The following changes were implemented for this release:

- Updated the schematics:
 - Added the property and notation DNP to the resistor R51
- · Updated document format

Revision A - June 2018

Initial release of this document.

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