Exp.No…9……. Name of the Experiment: Asynchronous Counter or Ripple Counter

Aim: Construct a 4 bit ripple counter using JK FF IC

Objectives: To study the design , Construction , and the working of various Counters.

Components: Bread board/ Kit , 7476,7408

Theory:

Asynchronous Counter or Ripple Counter

The counter in which external clock is only given to the first Flip-flop & the succeeding Flip-flops are clocked by the output of the preceding flip-flop is called asynchronous counter or ripple counter. The name ripple counter is because the clock signal ripples its way from the first stage of Flip-flops to the last stage

A binary ripple counter consists of series connection of complementing flip-flops with outputs of each flip-flop connected to the clock of the next higher order flip-flop. The flip-flop holding the least significant bit receives the incoming pulse. A complementing flip-flop can be obtained from a JK flip-flop with J & K inputs tied together or from a T flip-flop. The inputs of all flip-flops are connected to logic 1. This makes each flip-flop complement if the clock input goes through negative transition. IC 7476 consists of two JK flip-flops with PRESET & CLEAR.

The pin diagram is as shown in figure.

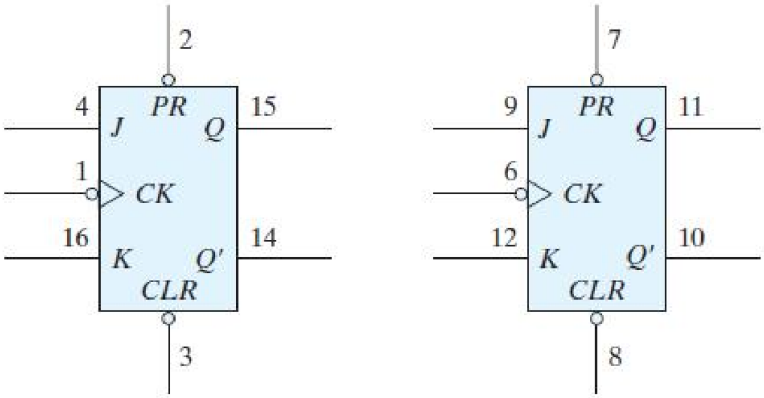
Synchronous counter, Construct a synchronous four-bit binary counter and check its operation. Use two 7476 ICs and one 7408 IC.

However, with the Synchronous Counter, the external clock signal is connected to the clock input of EVERY individual flip-flop within the Counter so that all of the flip-flops are clocked together simultaneously (in parallel) at the same time giving a fixed time relationship. In other words, changes in the output occur in "synchronisation" with the clock signal. The result of this synchronisation is that all the individual output bits changing state at exactly the same time in response to the common clock signal with no ripple effect and therefore, no propagation delay. Ripple up-counter starts counting from 0 and counts up to its maximum range. Its range depends on the number of flip-flop being used.

Ripple up-counter can be made using T-Flip flop and D-Flip flop.Designing of counters using flip-flops differs from each other with the type of flip-flop being used.

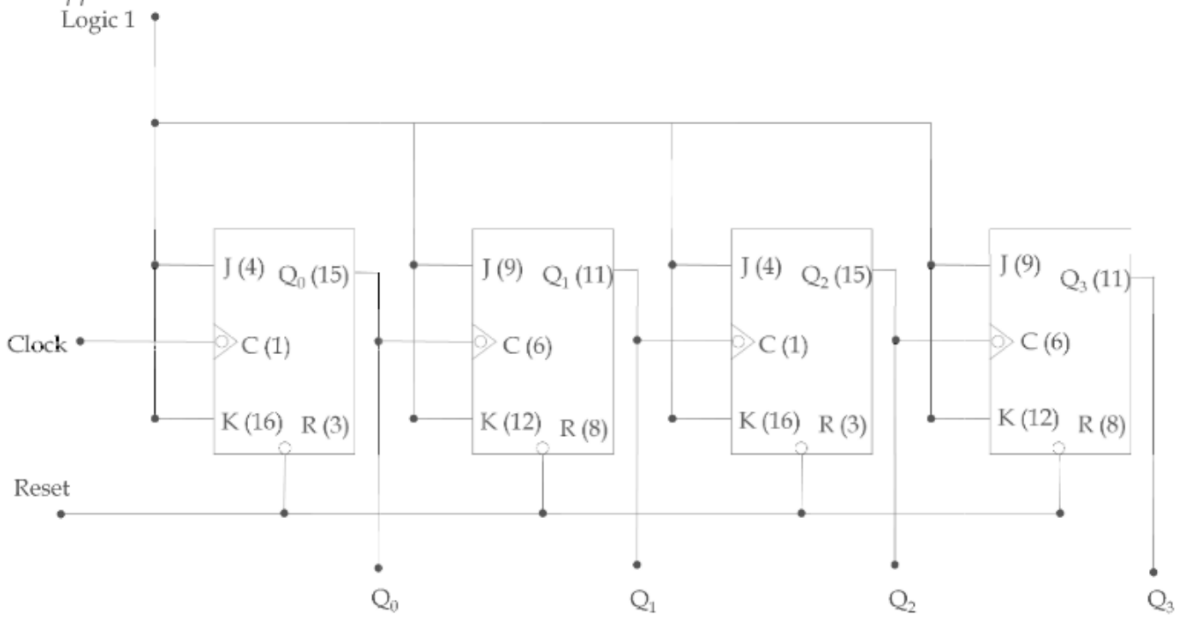
Consider a 3-bit counter with Q0, Q1, Q2 as the output of Flip-flops FF0, FF1, FF2 respectively. The state table for the 3-bit counter is given below:

State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1



V_{CC} = pin 5
GND = pin 13

4-bit Ripple Counter:



Procedure

1. Connections are made as per the circuit diagram

2. Switch on the power supply

3. Observe the outputs; compare the outputs with the truth tables

Result :