MODULE -4 : MICROPROCESSORS

Microprocessor is a single-chip CPU used in microcomputers. The Central Processing Unit (CPU) controls the operation of a computer system. CPU contains Arithmetic Logic Unit (ALU), Control Unit (CU) and registers. Thus microprocessor is a major component in the microcomputers which is responsible for controlling all the activity in the system.

Programs given to a computer is executed by CPU by performing the following three main activities:

1. Fetch an instruction from memory
2. Decode the instruction
3. Execute the instruction

History of microprocessors:

- The integrated circuit (IC) technology had wide acceptance during 1960s
- Many companies, such as Intel, Motorola, AMD, Zilog etc. are involved in developing microprocessors
- Intel was the dominant company among these
- Intel 4004 was the first microprocessor
- Microprocessors are categorized based on their word length (the number of bits it can process at a time), addressing capacity, clock speed etc.

Following table shows a brief history of Intel processors.

Processor	Year of release	Word length	Clock speed	Transistors used
4004	1971	4 bit	108 KHz	2300
8008	1972	8 bit	800 KHz	3500
8080	1974	8 bit	2MHz	4500
8085	1976	8 bit	3MHz	6500
8086	1978	16 bit	5MHz 8 MHz 10 MHz	29000
8088	1979	8bit External 16 bit internal	4.77 MHz 8 MHz	29000

The 8086 was the first 16 bit processor which gave rise to the x86 architecture. Later processors followed this x86 architecture which are called x86 family of processors. Some of them are :

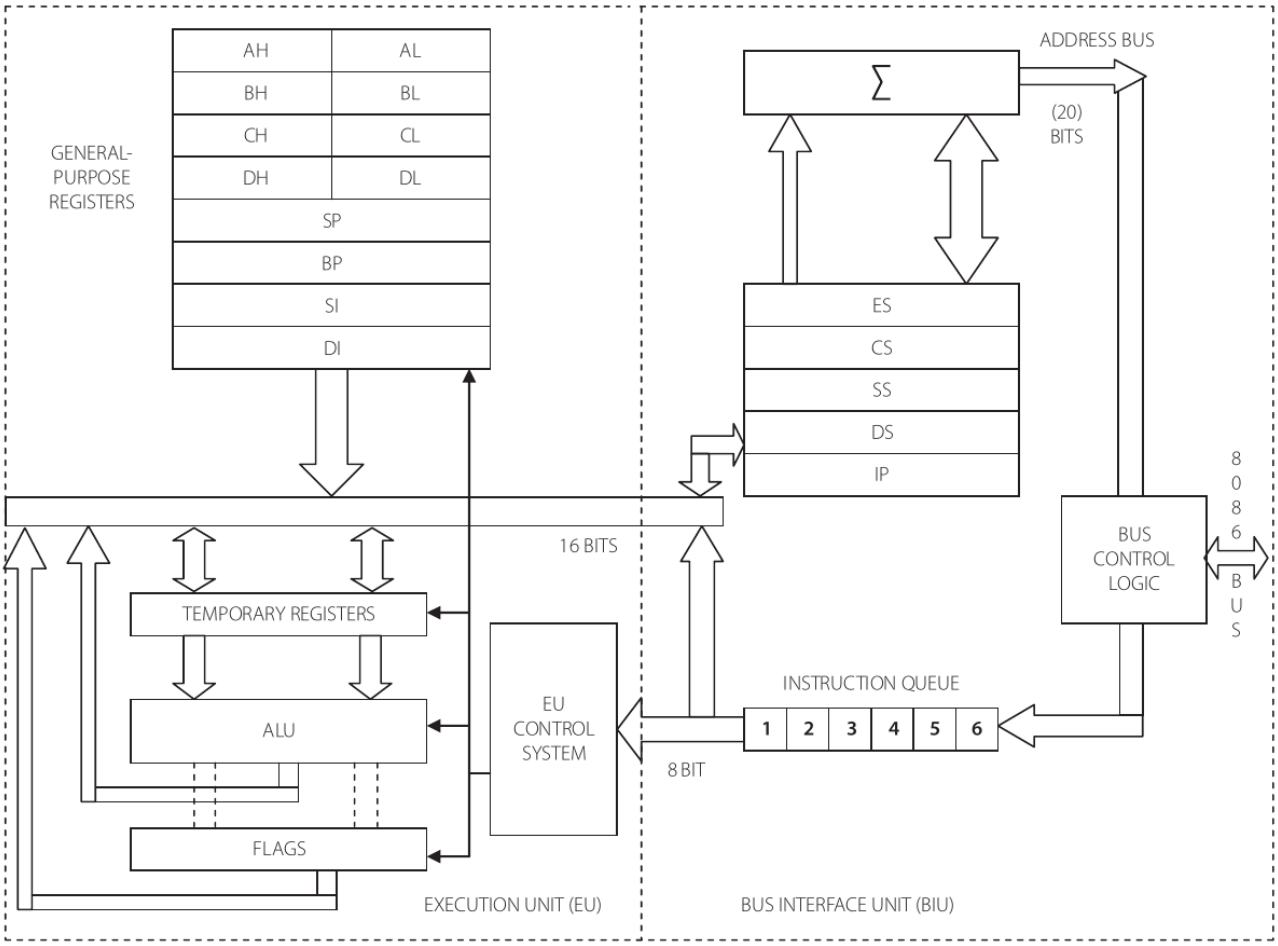
- 16 bit processors : 8086 (1978), 8088 (1979), 80186 (1982), 80286 (1982)
- 32 bit processors : 80386 (1985), 80486 (1989), Pentium (1993), Pentium Pro (1995), Pentium-2(1997), Pentium-3 (1999)
- 64 bit processors : Pentium Dual core, Core i3, Core i5, Core i7 etc.

Intel 8086 Microprocessor

Features of 8086:

- It is the first 16 bit processor
- It has 16 bit data bus. So it can read or write data either 8 bits or 16 bits.
- It has 20 bit address bus. So it can address a maximum of 2^{20} (1 MB) memory locations.
- It is available in three clock speeds : 5 MHz, 8 MHz and 10 MHz
- It operates in single processor and multiprocessor configuration
- It supports two stage pipelining.
- It can pre-fetches up to 6 instruction bytes from memory and queues them in order to speed up instruction execution.
- It has 256 vectored interrupts
- Its instruction set supports several addressing modes.
- It supports memory segmentation

Internal Block Diagram of 8086



The 8086 microprocessor is internally divided into two separate functional units to speed up processing. These are:

- Bus Interface Unit (BIU)
- Execution Unit (EU).

The Bus Interface Unit (BIU)

The BIU performs all external bus operations, such as:

- It calculates address to access memory or I/O
- It pre-fetches instructions from memory to instruction queue
- It writes or reads data to and from memory or I/O

To perform these above functions, the BIU has the following sections:

- Segment registers
- Instruction Pointer
- Instruction queue

Memory segments and Segment registers

The 1MB memory is divided into four segments of maximum 64KB size. These memory segments are called:

- Code segment
- Data segment
- Extra segment
- Stack segment.

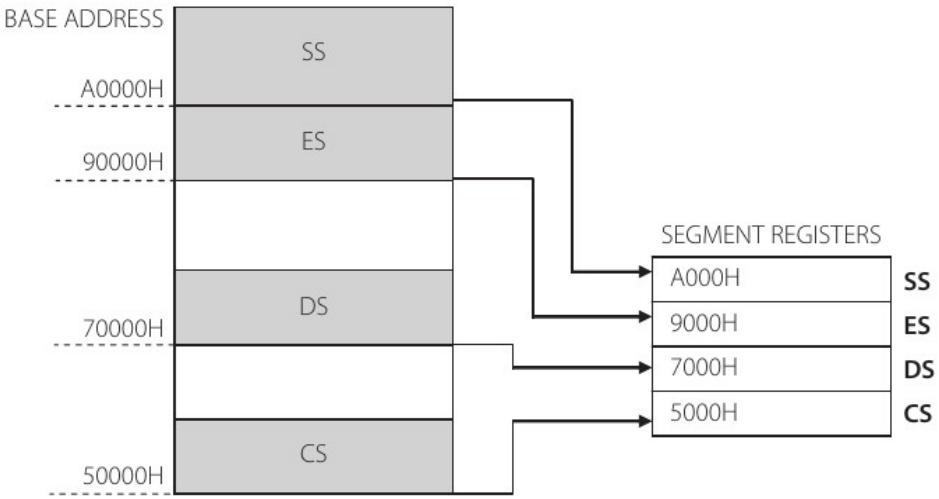
    - The code segment is used to store code (programs)
    - The data segment and extra segment are used to store data
    - The stack segment is used for stack.

There can be any number of these segments, but only four segments can be accessed at a time.
To access any location from a 1MB memory, we need 20 bit address.

There are four segment registers in the BIU. All are 16 bit size.

1. Code Segment register (CS)
2. Data Segment register (DS)
3. Extra Segment register (ES)
4. Stack Segment register (SS)

These segment registers contain the upper 16 bits of the base address of each memory segment which are active at a time. For example, the CS contain the upper 16 bits of the base address of Code segment. Following figure shows the relationship between segment registers and memory segments.



Calculating physical address:

The 20 bit address is called physical address. This 20 bit physical address is represented using two 16 bit numbers, which is called logical address. The logical address is written in *base address:offset* format. Physical address is generated by shifting the base address four times left and adding the offset to it. Shifting four times left creates four zeros in binary at the right most positions.

For example:

Let the logical address 2222H:0016H, then the physical address is calculated by shifting the 2222H four times left. It gives 22220H. Then add the offset as given below:

$$\begin{array}{rr} & 22220\text{H} \\ + & \underline{0016\text{H}} \\ & \underline{\mathbf{22236\text{H}}} \end{array}$$

So the 20 bit physical address is: 22236H

Instruction Pointer (IP)

IP is a 16 bit register which is similar to Program Counter register (PC). IP contains the offset. IP indicates the offset of the next instruction to be fetched from code segement of memory. The 20 bit physical address of next instruction is generated from CS:IP

Instruction Queue

It is 6 byte FIFO queue which is used to pre-fetch up to six instruction codes in advance. This method speed up program execution. The BIU fetches next instruction while executing the current instruction. This technique is called pipelining.